CY7C65221

Dual I²C Slave Bridge

Features

- Dual channel I²C slaves
  - 400 kHz I²C clock rate
  - 1 byte sub-addressing
  - 256 byte register space
  - Configurable slave port base address
  - Interrupt line only for I2C_B (INT_B)
- Clocking: Integrated 48 MHz clock oscillator
- Operating voltage: 1.71 to 5.5 V
- Operating temperature: –40 °C to 85 °C
- ESD protection: 2.2 kV HBM
- RoHS compliant package
- 24-pin QFN (4 mm × 4 mm, 0.5 mm pitch, 0.55 mm height)
- Ordering part number CY7C65221-24LTXI

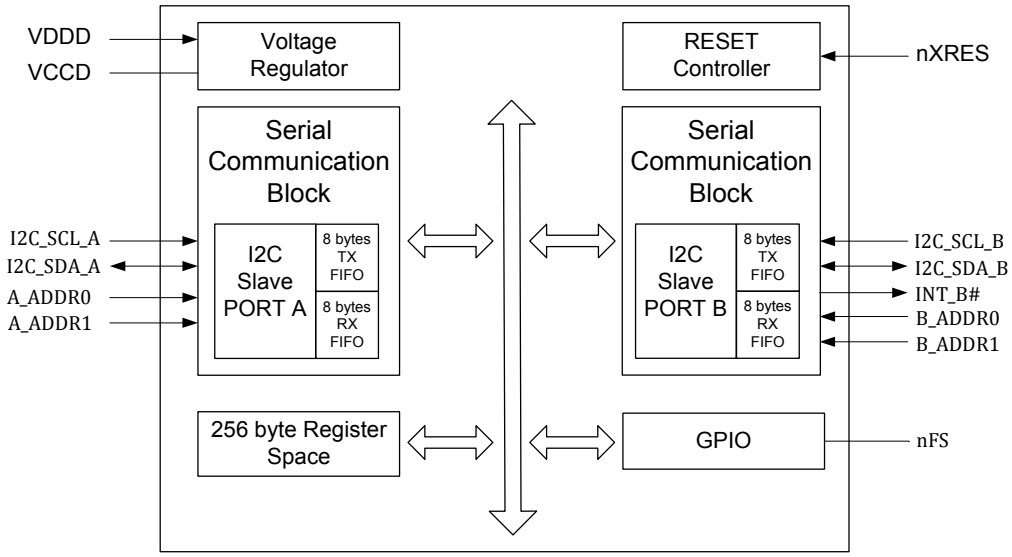
Applications

- Test and measurement systems
- Industrial

Functional Description

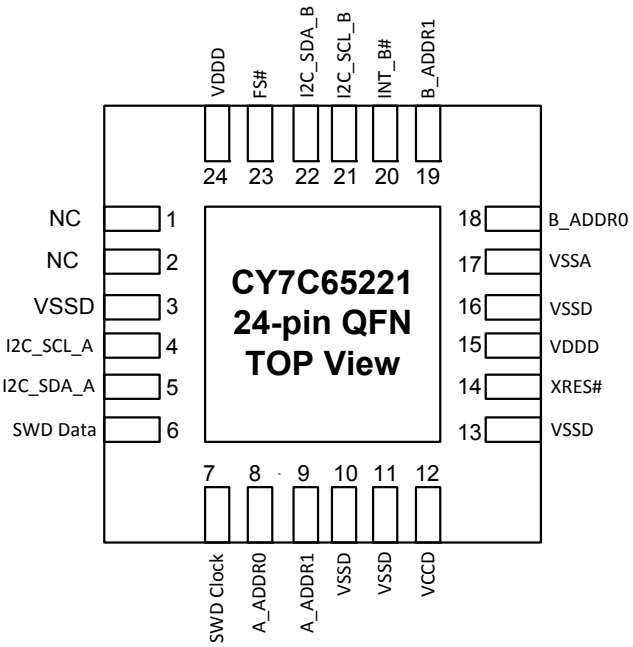
CY7C65221 is an I²C bus bridge. It functions as an I²C slave for two masters, allowing them exchange data. This bridge is to have a communication path between the Cypress FX3S RAID solution and the Dell board controller.

Block Diagram



Contents

Pin Configuration



Pin Description

Pin	Type	Name	Description
1	NC	NC	
2	NC	NC	
3	Power	VSSD	Digital Ground
4	Input	I2C_SCL_A	Port A I^2C Clock. 400 KHz max
5	Input / Output	I2C_SDA_A	Port A I^2C data
6	Input / Output	SWD Data	In-system serial programming and debug data
7	Input	SWD Clock	In-system serial programming and debug Clock
8	Input	A_ADDR0	Port A I^2C base address select, bit 0
9	Input	A_ADDR1	Port A I^2C base address select, bit 1
10	Power	VSSD	Digital Ground
11	Power	VSSD	Digital Ground
12	Power	VCCD	This pin is an output of an internal regulator and cannot drive external devices. Decouple this pin to ground using 1 µF capacitor when the VCCIO voltage is greater then 2 V. Connect this pin to VCCIO supply when the VCCIO voltage is less then 2 V.
13	Power	VSSD	Digital Ground
14	Input	XRES#	Chip reset, active low. Can be left unconnected or have a pull-up resistor connected to VCCIO supply.
15	Power	VDDD	Supply to the device core. 3.3 V to 5.5 V
16	Power	VSSD	Digital Ground
17	Power	VSSA	Analog Ground
18	Input	B_ADDR0	Port B I^2C base address select, bit 0
19	Input	B_ADDR1	Port B I^2C base address select, bit 0
20	Output	INT_B#	Port B I^2C interrupt request
21	Input	I2C_SCL_B	Port B I^2C Clock. 400 KHz max
22	Input / Output	I2C_SDA_B	Port B I^2C data
23	Input / Output	FS#	Fail safe Input
24	Power	VDDD	Supply to the device core and interface, 1.71 V to 5.5 V

Functional Overview

Bridge register space

The 256 byte address space is divided into three areas: BMC-FX3S register space, Bridge register space and Bridge buffer space. The legend used in the following register definitions are:

Table 1. Register Space Legend

Legend	Description
A	I2C_A (BMC) interface
B	I2C_B (FX3S) interface
Br	Bridge
RW	Read write access
RS	Read and Set only

BMC-FX3S register space

The BMC-FX3S register space occupies locations 0x00 to 0x5F. This space is maintained by FX3S (I2C_B) interface. The Bridge only provides the required field mask option for the data bytes and does not decode the writes to this address space except for two specific registers provided by the Bridge (I2C_A_WRITE_ADDR and I2C_A_WRITE_SIZE). Whenever there is a write operation from the BMC interface, the Bridge updates I2C_A_WRITE_ADDR and I2C_A_WRITE_SIZE registers and interrupts FX3S by asserting the INT_B line. The I2C_A interface shall be clock stretched until the FX3S de-asserts the INT_B line.

Bridge register space

The Bridge register space occupies locations 0x1E, 0x1F and 0x60-0x7F. This space is maintained by the Bridge and allows for configuration and operation of the Bridge. These are special registers which are expected to be used only from the I2C_B (FX3S) interface. However, the Bridge does not prevent access to these registers from I2C_A interface. The I2C_A_WRITE_ADDR and I2C_A_WRITE_SIZE registers are placed at 0x1E and 0x1F so that FX3S can read the complete 32 byte BMC register space in a single read.

The following are the Bridge special function registers:

I2C_A_WRITE_ADDR

This register along with I2C_A_WRITE_SIZE register allows FX3S to easily identify the last modified address from the BMC side. The Bridge updates the ADDR field whenever BMC finishes a write to the BMC-FX3S register space on I2C_A interface.

I2C_A_WRITE_ADDR		0x1E			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Bit [7:0]	ADDR	R	RW	R	The register holds the last updated start address from I2C_A interface to BMC register space. This allows FX3S to identify the write location from BMC side.

I2C_A_WRITE_SIZE

This register along with I2C_A_WRITE_ADDR register allows FX3S to easily identify the last modified register space from the BMC side. The Bridge updates this register whenever the BMC finishes a write to the BMC-FX3SA register space on I2C_A interface.

I2C_A_WRITE_SIZE		0x1F			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Bit [7:0]	SIZE	R	RW	R	The register holds the size of the last write from I2C_A interface to BMC register space. This allows FX3S to identify the write location from BMC side.

BRIDGE_VERSION

The register holds the Bridge firmware version information. This is a read-only field from both I^2C interfaces. This field can be used to determine whether the Bridge firmware matches the FX3S firmware and whether the Bridge requires a firmware upgrade.

BRIDGE_VERSION		0x60–0x63			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Byte[0]	MAJOR_ VERSION	R	–	R	The byte represents the major firmware revision number.
Byte[1]	MINOR_ VERSION	R	–	R	The byte represents the minor firmware revision number.
Byte[3-2]	PATCH_ VERSION	R	–	R	The word represents the patch revision number.

BRIDGE_BUILD

The register holds the Bridge firmware build number. This is a read-only register from the I^2C interfaces.

BRIDGE_BUILD		0x64–0x67			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Byte[3-0]	BUILD_ NUMBER	R	–	R	The byte represents the Bridge firmware build number.

BRIDGE_MODE

The register holds the active firmware number. This is a read-only register from the I^2C interfaces.

BRIDGE_MODE		0x68			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Bit [7:0]	OP_MODE	R	–	R	0 – Primary (fail-safe) firmware active 1 – Secondary firmware active.

I2C_CTRL

The register allows the FX3S interface to configure I2C_A interface. The lower nibble holds configuration for I2C_A interface and upper nibble holds configuration information for I2C_B interface.

I2C_CTRL		0x69			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Bit [0]	I2C_A_ENABLE	R	–	RW	0 – Disable I2C_A interface. When disabled, the interface shall NAK any request. 1 – Enable I2C_A interface. The reset value of this field is 0.
Bit [4:1]	Reserved	R	–	R	Reserved.
Bit [5]	INT_B_CLEAR	R	–	RW	This bit is used by FX3S interface to de-assert the INT_B line. 0 – Do nothing 1 – Bridge shall de-assert INT_B and clear this bit. Read of this bit shall indicate the current status of the INTR line. If INTR line is asserted the bit shall be set, otherwise it shall be 0.
Bit [7:6]	Reserved	R	–	R	Reserved.

BRIDGE_RESET

The register allows the I2C interfaces to reset the Bridge. The reset operation only performs a soft reset and a hard reset can only be done by asserting the XRES line on the Bridge.

BRIDGE_RESET		0x6A–0x6B			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Byte [0]	RESET_ SIGNATURE	RW	RW	RW	The Bridge shall allow reset only if this byte is loaded with 0xAD (~R). The default value for this field is 0. Once the Bridge acts on the reset request, the field is again reset to 0. This is to prevent spurious reset.
Byte[1]: Bit [0]	RESET	RW	–	RW	Request a reset. 0 – Do nothing 1 – Request for a reset. A read to this field will always return 0.
Byte[1]: Bit [7:1]	Reserved	R	–	R	Reserved.

BRIDGE_MODE_RQT

The register allows the I^2C interfaces to request to Bridge to jump to fail-safe mode. This operation shall result in resetting the Bridge. On subsequent power cycle or reset, the device shall boot back to secondary image if a valid secondary image is available. This register is required for doing a firmware upgrade.

BRIDGE_MODE_RQT		0x6C–0x6D			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Byte [0]	MODE_RQT_ SIGNATURE	RW	RW	RW	The Bridge shall honor the request only if this byte is loaded with 0xB2 (~M). The default value for this field is 0. Once the Bridge acts on the request, the field is again reset to 0.
Byte[1]: Bit [0]	MODE_RQT	RW	–	RW	Request a fail-safe entry. 0 – Do nothing 1 – Request for a fail-safe entry. The Bridge shall jump to primary firmware if running in secondary firmware mode. Otherwise nothing is done. A read to this field will always return 0.
Byte[1]: Bit [7:1]	Reserved	R	–	R	Reserved.

BRIDGE_SPL_RQT

The register allows for various special functions which use the upper 128 byte buffer area of the Bridge. The I^2C interfaces are first expected to load the information into the upper 128 byte buffer area and then indicate the completion by writing to this register. Only one bit in the register can be set at a time. If more than one bit is set, the Bridge shall treat it as a bad request. On completion of a request, the Bridge shall clear the request bits and then load the status of the request into the signature field. If the request was completed successfully, the signature field shall be made zero. The field shall be non-zero if the request failed. The return error codes are:

Error code	Value	Description
SUCCESS	0	Request was completed successfully.
BAD_ARGUMENT	1	Request had bad arguments.
NOT_CONFIGURED	3	Device is not ready to take the request.
TIMEOUT	8	Request handling timed out.
NOT_SUPPORTED	10	Request currently not supported.
ERROR_FAILURE	14	General request failure.

BRIDGE_SPL_RQT		0x6E–0x6F			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Byte [0]	SPL_RQT_ SIGNATURE	RW	RW	RW	The Bridge shall honor the request only if this byte is loaded with 0xB9 (~F). The default value for this field is 0. Once the Bridge acts on the request, the field is again reset to 0.
Byte[1]: Bit [0]	FW_IMG_RQT	RW	–	RW	Indicate to the Bridge that 128 bytes of firmware image for upgrade has been loaded into the buffer area. 0 – Do nothing 1 – FW image indication. The Bridge shall clear the field on programming the flash. A read to this field will always return 0.
Byte[1]: Bit [1]	I2C_A_MASK_ RQT	RW	–	RW	Indicate to the Bridge that 96 bytes of field write enable mask for I2C_A interface is loaded into the buffer area. 0 – Do nothing 1 – Buffer available indication. The Bridge shall clear the field on programming the flash. A read to this field will always return 0.
Byte[1]: Bit [2]	I2C_B_MASK_ RQT	RW	–	RW	Indicate to the Bridge that 96 bytes of field write enable mask for I2C_B interface is loaded into the buffer area. 0 – Do nothing 1 – Buffer available indication. The Bridge shall clear the field on programming the flash. A read to this field will always return 0.
Byte[1]: Bit [3]	FW_IMG_ ABORT	RW	–	RW	Abort any in progress firmware upgrade operation. After this the secondary image cannot be used.
Byte[1]: Bit [4]	FW_IMG_ IN_PROG	R	–	R	Firmware upgrade is in progress. The secondary image is valid only after the complete image is sent across over the I2C interface. This bit is set when Bridge starts updating the first section of the secondary image and is cleared on receiving the last section or in case of any error.
Byte[1]: Bit [7:5]	Reserved	R	–	R	Reserved.

BRIDGE_MEMORY_OP

This register allows the bridge to read and update the Flash and RAM locations. For write operation, the I2C master shall first load the data in the buffer area and then indicate the completion by writing to this register. For read operation, the I2C master is first expected to write to the register with read request. Bridge shall update the buffer area with the requested data bytes. Similar to BRIDGE_SPL_RQT, on completion of a request, the Bridge shall clear the request bits and then load the status of the request into the signature field. If the request was completed successfully, the signature field shall be made zero. The field shall be non zero, if the request failed. For flash operation, data size shall always be 128(Flash Row Size). The flash address should be a 128 bytes multiple. Flash operations are supported only in FAIL SAFE mode.

BRIDGE_MEMORY_OP		0x72–0x78			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Byte [0]	MEMORY_OP_ SIGNATURE	R	RW	RW	The Bridge shall honor the request only if this byte is loaded with 0xBA. The default value for this field is 0. Once the Bridge acts on the request, the field is again reset to 0.
Byte[1]: Bit [0]	WRITE_READ	R	–	RW	Indicates to the bridge if the request is for memory read or write. 0 – Read 1 – Write A read to this field will always return 0.
Byte[1]: Bit [1]	FLASH_RAM	R	–	RW	Indicates to the bridge if the request is for FLASH or RAM operation. 0 – RAM 1 – FLASH A read to this field will always return 0.
Byte[1]: Bit [2:7]	Reserved	R	–	R	Reserved.
Byte[2:5]:	ADDRESS	R	–	RW	The memory address for read or update. As mentioned above, the address shall be multiple of 128 for FLASH operations. For RAM operations, address should be 32 bit aligned.
Byte[6]:	COUNT	R	–	RW	The count of bytes (4 Bytes) to read or write. For FLASH operation, this field is ignored as flash operations shall be 128 bytes only. For RAM operations, the count shall be 32 or less as the size of bridge buffer area is 128 bytes (32 words).

BRIDGE_TIMEOUT_RQT

This register allows the bridge to update the timeout duration for both the interfaces. The default timeout is 500 ms. On completion of a request, bridge shall load the status of the request into the signature field. If the request was completed successfully, the signature field shall be made zero. The field shall be non zero, if the request failed.

BRIDGE_TIMEOUT_RQT		0x7B–0x7D			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Byte [0]	TIMEOUT_RQT SIGNATURE	R	RW	RW	The Bridge shall honor the request only if this byte is loaded with 0xBB. The default value for this field is 0. Once the Bridge successfully acts on the request, the field is again reset to 0.
Byte[1:2]	TIMEOUT_VALUE (ms)	R	–	RW	This field shall be set with the timeout value. The minimum timeout supported by the bridge is 100ms. Any value less than that will be flagged as an error. To disable timeout detection feature this field shall be set with 0xFFFF. The timeout value shall be updated after the completion of the current I2C write request and I2C master on both interface shall read this field to determine the current timeout value The byte order is little endian.

BRIDGE_STATUS

This register shall be used to determine the current status of both I2C interfaces. It shall flag any I2C bus, timeout and state machine errors detected on the interfaces. The lower nibble shall be reserved for I2C_A interface and the upper nibble for I2C_B interface. In case of any error bridge shall reset the corresponding I2C interface.

BRIDGE_STATUS		0x7E			
Field	**Field Name**	**A**	**Br**	**B**	**Description**
Bit[0]	I2C_A_TIMEOUT_ERROR	R	RW	RW	The bit shall be set if a timeout error is encountered on I2C_A interface. The bridge shall de-assert the INT _B line and reset the I2C_A interface. Write with 1 to clear the bit.
Bit[1]	I2C_A_BUS_ERROR	R	RW	RW	This bit shall be set by bridge if an I2C Bus error or arbitration error is detected on I2C_A interface. Write with 1 to clear the bit.
Bit[2]	I2C_A_INVALID_CMD_ERROR	R	RW	RW	This bit shall be set by bridge if a state machine error is detected due to invalid sequence of I2C commands from the master on I2C_A interface. Write Restart, Write across register boundaries and Write rollback to 0 are examples of such error. Write with 1 to clear the bit.
Bit[3]	RESERVED	–	–	–	Reserved for future use.
Bit[4]	I2C_B_TIMEOUT_ERROR	R	RW	RW	The bit shall be set if a timeout error is encountered on I2C_B interface. Write with 1 to clear the bit.
Bit[5]	I2C_B_BUS_ERROR	R	RW	RW	This bit shall be set by bridge if an I2C Bus error or arbitration error is detected on I2C_B interface. Write with 1 to clear the bit.
Bit[6]	I2C_B_INVALID_CMD_ERROR	R	RW	RW	This bit shall be set by bridge if a state machine error is detected due to invalid sequence of I2C commands from the master on I2C_B interface. Write Restart, Write across register boundaries and Write rollback are examples of such error. Write with 1 to clear the bit.
Bit[7]	RESERVED	–	–	–	Reserved for future use.

Bridge Buffer Space

The Bridge provides 128 bytes of buffer space (0x80–0xFF). The buffer area is used for FX3S firmware upgrade.

Bridge I²C Interface

The Bridge provides EEPROM like access to its internal registers / buffers. It exposes a byte addressed 8 bit register space. The lower 128 byte space is expected to be used as control / status registers for the Bridge communication while the upper 128 byte space is expected to be used as data buffer space for communication. The Bridge I²C interfaces support EEPROM like read / writes access. The following are the operations supported at the I²C interface:

WRITE

Figure 1. Bridge Write Sequence

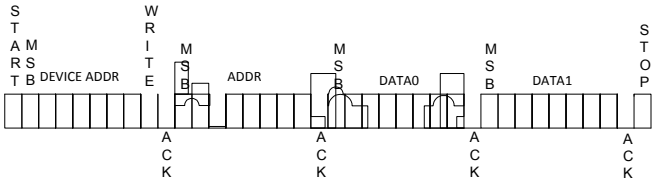


Figure 1 shows the bus sequence for a write operation of two data bytes to the Bridge. The first byte following a write preamble shall always be the start address of the write operation. Any subsequent data bytes shall be written down to the register area. While the data is being received on the I²C bus, the Bridge stores the information in a temporary buffer and updates the register space only on receiving a stop signal on the bus. The writes are done after validating the write and only the fields which are write-enabled are updated. A write operation always needs to be terminated by a stop signal and a re-start after a write operation is not allowed. The write request allows for one or more register location writes in a single operation. The maximum allowed write size is 128 bytes. Any write that crosses the 256 byte boundary shall result in a failed write and none of the bytes in the write operation shall get updated. Any write which crosses boundaries (BMC-FX3S register space – Bridge register space – Buffer space), shall result in a failed write and none of the bytes in the write operation shall get updated.

RANDOM READ

Figure 2. Bridge Random Read Sequence

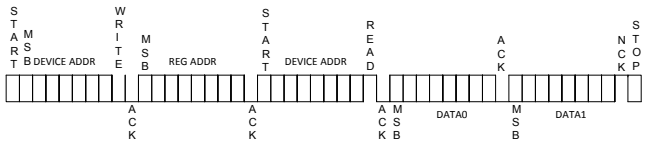


Figure 2 shows the bus sequence for a random read operation of two data bytes from the Bridge. The read operation consists of two parts: 1) Address update sequence; 2) followed by read operation. The address update sequence is essentially a write operation without any data bytes. The read operation follows this with a re-start signal on the bus. The read option allows for reading one or more bytes from the Bridge from the address specified. For read operation, if the read address overflows the 256 byte boundary, then the address shall wrap around and the current address shall be made as zero. The read operation is not failed in this case. This read operation model is the recommended read operation mode as it uses re-start instead of a start followed by a stop. On a multi-master bus, a re-start bit is generally treated as an atomic operation and the bus is freed only on seeing a stop bit. So the address phase and the data phase stay in sync.

SEQUENTIAL READ

Figure 3. Bridge Sequential Read Sequence

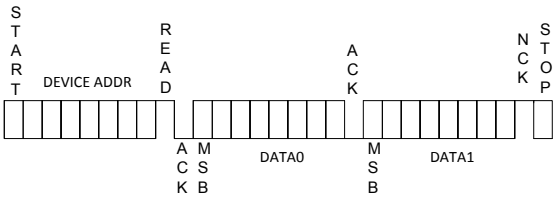
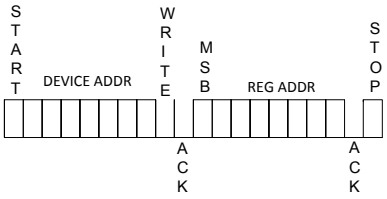


Figure 3 shows the bus sequence for a sequential read operation of two data bytes. A sequential read allows reading data from the current read location. The current read location gets updated on any read / write operation. The address is incremented on every byte read / written from / to the Bridge interface. The read operation is similar to the random read operation but on a multi-master bus, there shall be no guarantee that the read address shall not get modified between transactions resulting in wrong address location to be read back.

SET ADDRESS

Figure 4. Bridge Set Address Sequence



The SET ADDRESS operation is a partial write / random read operation, where only the address location gets updated followed by a stop signal on the bus.

I²C slave address

The Bridge I²C address is derived during boot and is not dynamically changed. The address has two components: 1) Fixed 5 MS bits and 2) Configurable 2 LS bits. The following tables indicate the I²C slave address used for each interface.

I2C_A interface address

A_ADDR1 and A_ADDR0 are the states of the I/O lines at boot.

I2C_A Address						
Bit 6	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	0	0	0	A_ADDR1	A_ADDR0

I2C_B interface address

B_ADDR1 and B_ADDR0 are the states of the I/O lines at boot.

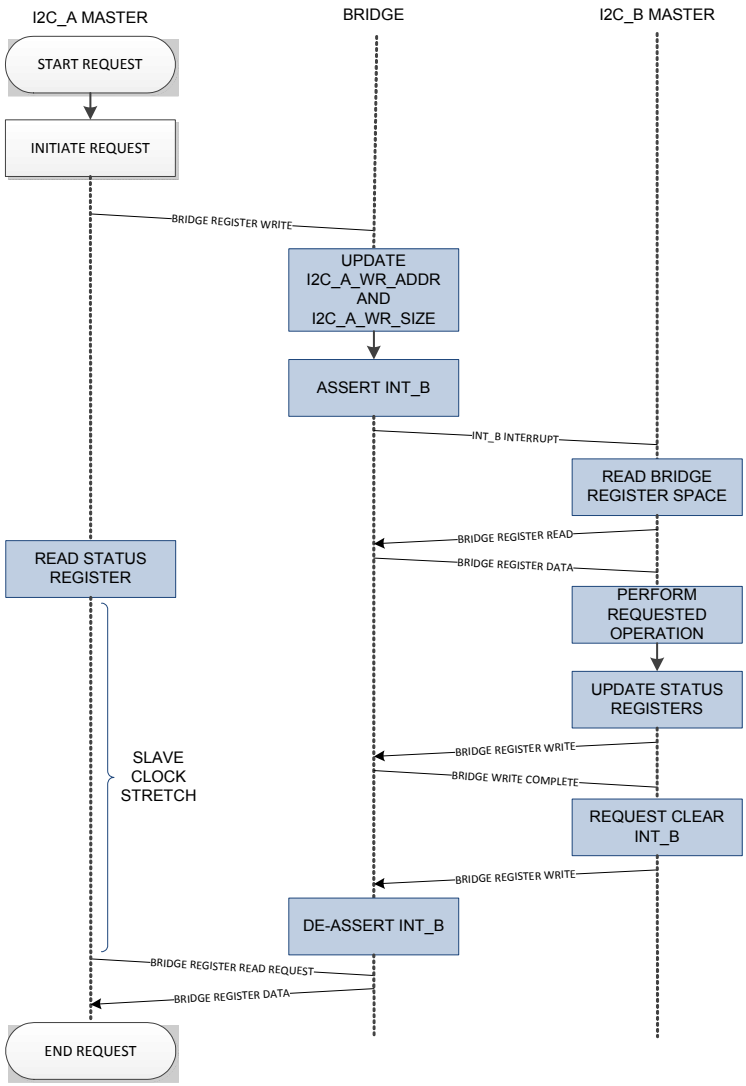
I2C_A Address						
Bit 6	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1	1	0	0	0	B_ADDR1	B_ADDR0

Bridge BMC-FX3S Communication

The BMC communicates with the Bridge through the I2C_A interface while the FX3S uses the I2C_B interface. The BMC and FX3S have full read access to the 256 byte register space of the Bridge. The BMC and FX3S have different read only fields which cannot be updated.

Actual protocol to be used for FX3S Raid Solution is documented in “Internal Dual Secure Digital Module Specification” provided by Dell. Figure 5 describes a typical operation sequence for a BMC request to the FX3S.

Figure 5. BMC Request Operation Sequence



BMC initiates a request by writing into the Bridge register space. Once BMC completes the register write with a stop signal on the I^2C bus, the Bridge updates the register memory and then updates the I2C_A_WRITE_ADDR and I2C_A_WRITE_SIZE registers with information about the BMC write. Once this is done, it initiates an interrupt to FX3S by asserting the INT_B line.

FX3S on receiving an interrupt on INT_B line shall read the Bridge register space to determine the type of request received. It shall then perform the requested operation and then update the Bridge register space with the status information. Once FX3S has updated the status register space, it is expected to clear the INT_B interrupt. On clearing the INT_B interrupt, the Bridge shall de-assert the INT_B line.

The BMC needs to poll the Bridge status register for completion of the request.

Data protection

The Bridge register space can be accessed from both I2C_A and I2C_B interface. This results in possibility of the same register being accessed at the same time from both the interface. The Bridge allows only one interface to access the Bridge at one time. The first access is accepted and the second interface in the event of a contention is clock stretched in the preamble phase. The preamble shall not be ACKd and the clock line stretched until the first interface completes the access.

Additionally, since the Bridge status register has to be updated by FX3S, once BMC completes a write to the lower 128 byte area, the Bridge shall clock stretch any further request from BMC until FX3S clears the INT_B interrupt. This allows FX3S time to update the status register before BMC can read the status registers.

Clock stretching

The Bridge shall use clock stretching on both I2C interfaces until it is ready to take any new request. The clock shall be stretched at the following modes:

1. At the ACK / NAK phase of preamble / data bytes.
2. After DATA ACK If the RX FIFO is full and cannot receive any more data.

Register write-enable masks

The I2C_A interface as well as I2C_B interface has two different write enable masks for the first 96 byte register area in the Bridge. The Bridge uses this mask information to allow writes to go through to the register space. The 32 byte area above this is Bridge register information and cannot be modified. The upper 128 byte is fully writeable from both directions. Addresses 0x1E and 0x1F are always read-only from both interfaces. The Bridge by default allows writes to the first 96 bytes from both sides. The mask information has to be updated by FX3S on boot every time using the BRIDGE_SPL_RQT register based on the Dell register space requirement. For updating the write enable mask information for I2C_A interface, load the 96 byte mask information into the buffer space and then set the I2C_A_MASK_RQT bit in BRIDGE_SPL_RQT register. The Bridge firmware on receiving the request, shall update the local RAM copy with the new information. I2C_B interface mask information can be updated similarly. This information is not retained across Bridge reset and has to be loaded every time.

Bridge Firmware upgrade

The Bridge firmware upgrade can be done by loading the firmware image 128 byte at a time into the Bridge buffer area and trigger the flash programming by writing to the FW_IMG_RQT bit of the BRIDGE_SPL_RQT register. The Bridge shall decode the firmware image and then load the data to the required location. On receiving the last 128 byte packet of firmware image, the Bridge shall update the checksum and signature information to the checksum page in flash for the corresponding image.

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings[1] may shorten the useful life of the device.

Storage temperature ..... –55 °C to +100 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential
V_{DDD} ..... 6.0 V

V_{CCD} ..... 1.95 V

V_{GPIO} ..... V_{DDD} + 0.5

Static discharge voltage ESD protection levels:

■ 2.2-KV HBM per JESD22-A114

Latch-up current ..... 140 mA

Current per GPIO ..... 25 mA

Operating Conditions

T_A (ambient temperature under bias)
Industrial ..... –40 °C to +85 °C

V_{DDD} supply voltage ..... 1.71 V to 5.50 V

V_{CCD} supply voltage ..... 1.71 V to 1.89 V

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and 1.71 V to 5.50 V, except where noted.

Table 2. DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{DDD}	V_{DDD} supply voltage	1.71	1.80	1.89	V	Used to set I/O and core voltage. Set and configure the correct voltage range using a configuration utility for V_{DDD}. Default 3.3 V.
		2.0	3.3	5.5	V	
V_{CCD}	Output voltage (for core logic)	–	1.80	–	V	Do not use this supply to drive the external device. • 1.71 V ≤ V_{DDD} ≤ 1.89 V: Short the V_{CCD} pin with the V_{DDD} pin • V_{DDD} > 2 V – connect a 1-µF capacitor (Cefc) between the V_{CCD} pin and ground
Cefc	External regulator voltage bypass	1.00	1.30	1.60	µF	X5R ceramic or better
I_{DD1}	Operating Supply Current	–	7.25	12	mA	I^2C at 400 kHz dual channel

Table 3. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F1	Frequency	47.04	48	48.96	MHz	I^2C Bridge

Note
1. Usage above the Absolute Maximum conditions may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

GPIO

Table 4. GPIO DC Specification

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[2]	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	CMOS Input
V_{IH}[2]	LVTTL input, V_{DDD} < 2.7 V	0.7 × V_{DDD}	–	–	V	
V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 × V_{DDD}	V	
V_{IH}[2]	LVTTL input, $V_{DDD} \geq$ 2.7 V	2	–	–	V	
V_{IL}	LVTTL input, $V_{DDD} \geq$ 2.7 V	–	–	0.8	V	
V_{OH}	Output voltage high level CMOS Output	V_{DDD} –0.4	–	–	V	I_{OH} = 4 mA, V_{DDD} = 5 V +/- 10%
V_{OH}	Output voltage high level CMOS Output	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA, V_{DDD} = 3.3 V +/- 10%
V_{OH}	Output voltage high level CMOS Output	V_{DDD} –0.5	–	–	V	I_{OH} = 1 mA, V_{DDD} = 1.8 V +/- 5%
V_{OL}	Output voltage low level CMOS Output	–	–	0.4	V	I_{OL} = 8 mA, V_{DDD} = 5 V +/- 10%
V_{OL}	Output voltage low level CMOS Output	–	–	0.6	V	I_{OL} = 8 mA, V_{DDD} = 3.3 V +/- 10%
V_{OL}	Output voltage low level CMOS Output	–	–	0.6	V	I_{OL} = 4 mA, V_{DDD} = 1.8 V +/- 5%
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	
Rpulldown	Pull-down resistor	3.5	5.6	8.5	kΩ	
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
C_{IN}	Input capacitance	–	–	7	pF	
Vhysttl	Input hysteresis LVTTL; V_{DDD} > 2.7 V	25	40	C	mV	
Vhyscmos	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	

Table 5. GPIO AC Specification

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RiseFast1}$	Rise Time in Fast mode	2	–	12	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallFast1}$	Fall Time in Fast mode	2	–	12	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseSlow1}$	Rise Time in Slow mode	10	–	60	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallSlow1}$	Fall Time in Slow mode	10	–	60	ns	V_{DDD} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseFast2}$	Rise Time in Fast mode	2	–	20	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{FallFast2}$	Fall Time in Fast mode	20	–	100	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{RiseSlow2}$	Rise Time in Slow mode	2	–	20	ns	V_{DDD} = 1.8 V, Cload = 25 pF
$T_{FallSlow2}$	Fall Time in Slow mode	20	–	100	ns	V_{DDD} = 1.8 V, Cload = 25 pF

Note
2. V_{IH} must not exceed V_{DDD} + 0.2 V.

nXRES

Table 6. nXRES DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	
V_{IL}	Input voltage low threshold	–	–	0.3 × V_{DDD}	V	
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	
C_{IN}	Input capacitance	–	5	–	pF	
Vhysxres	Input voltage hysteresis	–	100	–	mV	

Table 7. nXRES AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Tresetwidth	Reset pulse width	1	–	–	µs	

I^2C Specifications

Table 8. I^2C AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{I2C}	I^2C frequency	1	–	400	kHz	

Flash Memory Specifications

Table 9. Flash Memory Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Fend	Flash endurance	100K	–	–	cycles	
Fret	Flash retention. $T_A \leq 85$ °C, 10 K program/erase cycles	10	–	–	years	

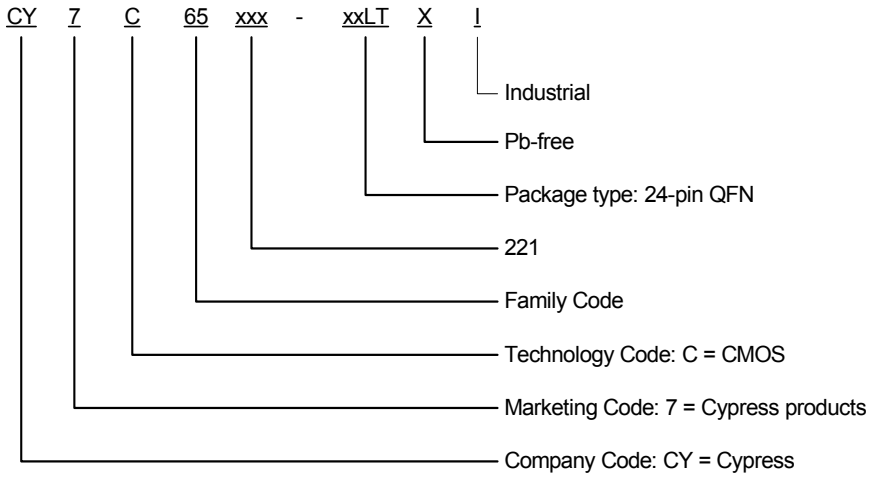
Ordering Information

Table 10 lists the key package features and ordering codes of the CY7C65211. For more information, contact your local sales representative.

Table 10. Key Features and Ordering Information

Package	Ordering Code	Operating Range
24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free)	CY7C65221-24LTXI	Industrial

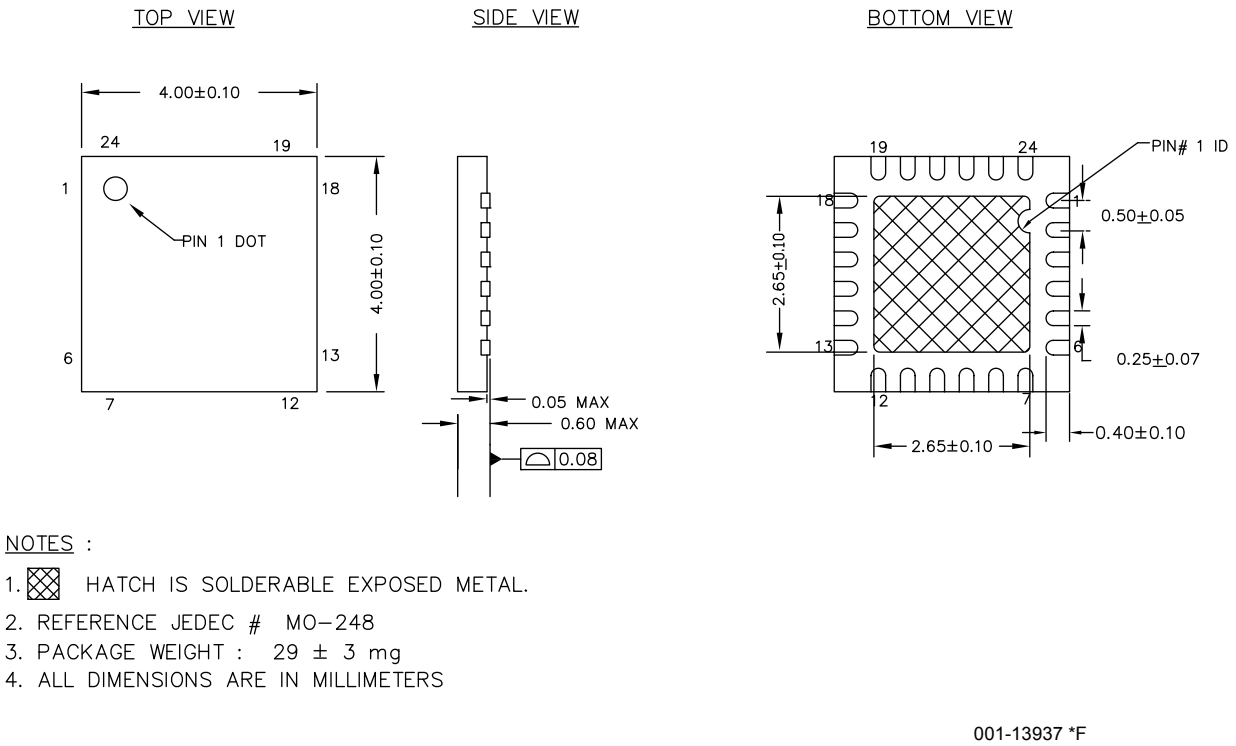
Ordering Code Definitions



Package Information

Support currently is planned for the 24-pin QFN package.

Figure 6. 24-pin QFN (4 × 4 × 0.55 mm) LQ24A 2.65 × 2.65 E-Pad (Sawn) Package Outline, 001-13937



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Table 11. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T_A	Operating ambient temperature	–40	25	85	°C
T_{HJ}	Package θ_{JA}	–	18.4	–	°C/W

Table 12. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
24-pin QFN	260 °C	30 seconds

Table 13. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL 3

Acronyms

Table 14. Acronyms used

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Discharge
GPIO	General Purpose Input/Output
HBM	Human-Body Model
I/O	Input/Output
I^2C	Inter-Integrated Circuit
LVTTL	Low-Voltage Transistor-Transistor Logic
QFN	Quad-Flat No-lead
RoHS	Restriction of Hazardous Substances

Document Conventions

Units of Measure

Table 15. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
kHz	kilohertz
kV	kilovolt
MHz	megahertz
µF	microfarad
mA	milliampere
mm	millimeter
mV	millivolt
nA	nanoampere
ns	nanosecond
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C65221, Dual I²C Slave Bridge Document Number: 001-89547				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4150932	DTNK	10/08/2013	New data sheet.
*A	4340874	MVTA	04/11/2014	Changed status from Preliminary to Final. Updated Pin Description: Updated description of pin 12 and pin 14. Updated Functional Overview: Updated Bridge register space: Updated BMC-FX3S register space: Updated description. Updated Bridge register space: Updated description corresponding to “I2C_A_WRITE_ADDR”. Updated table corresponding to “I2C_CTRL”. Updated table corresponding to “BRIDGE_SPL_RQT”. Added details corresponding to “BRIDGE_MEMORY_OP”. Added details corresponding to “BRIDGE_TIMEOUT_RQT”. Added details corresponding to “BRIDGE_STATUS”. Updated Bridge I2C Interface: Updated WRITE: Updated description. Added Register write-enable masks. Added Bridge Firmware upgrade. Updated Electrical Specifications: Updated Device-Level Specifications: Updated Table 2: Added I_{DD1} parameter and its details. Updated GPIO: Updated Table 4: Updated description of V_{OH} and V_{OL} parameters. Updated Table 5: Updated all the details.
*B	5473879	RAJV	10/13/2016	Updated Package Information: spec 001-13937 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*C	5987021	AESATMP9	12/07/2017	Updated logo and copyright.

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