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REFERENCE DESIGN IRPLCFL4 Rev.C

International Rectifier • 233 Kansas Street, El Segundo, CA 90245 USA

A 3 Way Dimming CFL Ballast

By   Peter Green

TOPICS COVERED

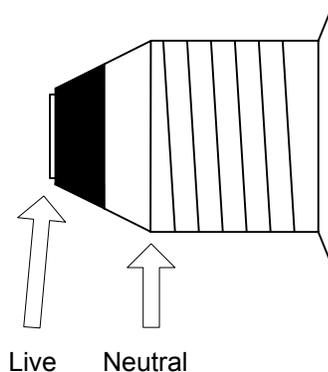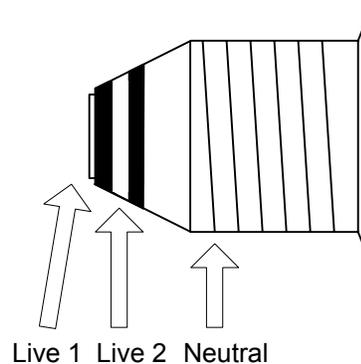|	
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Introduction

The 3 way dimming system widely adopted in the US with conventional filament lamps consists of a light bulb that has a modified Edison screw type base which allows 3 connections to be made to a special lamp socket that also has 3 connections.
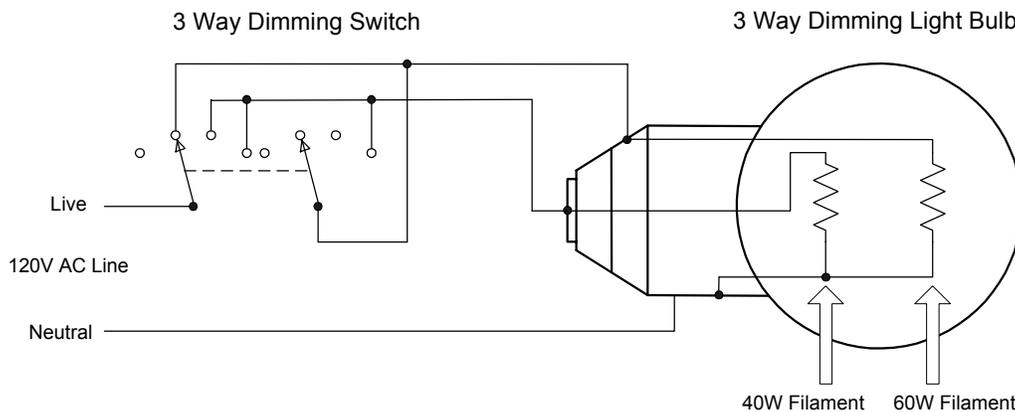

Standard Edison Screw Base

Live   Neutral

3 Way Dimming Edison Screw Base

Live 1 Live 2 Neutral

The 3 way dimming light bulb has two filaments inside which produce different light outputs when connected to the AC line. These filaments are connected in series such that the mid point goes to the line common and the two ends can be connected to the live either independently or both together. Thus with an external switch that has four positions, it is possible to obtain 3 different light levels or to switch off.

3 Way Dimming Switch   3 Way Dimming Light Bulb

Live

120V AC Line

Neutral

40W Filament   60W Filament

Existing Ballast Solutions

There are in existence CFL ballast designs that perform the same task. A common approach is a system whereby the line voltage is full wave rectified when one live input is connected and a voltage doubler circuit comes into operation when the other live input is connected or both are connected together thereby having two DC bus voltages in the ballast during dim level settings. This type of design also operates at two different frequencies, a low frequency (typically 40-45kHz) when both live inputs are connected providing a high lamp current and a higher frequency (for example 70-75kHz) when either of the two lives is connected alone which will produce a lower lamp current. In this way the following combinations are achieved:

1. Low DC bus (150V) / high frequency   ….. minimum output
2. High DC bus (300V) / high frequency   …... medium output
3. High DC bus (300V) / low frequency   …… maximum output

This approach has some serious drawbacks:
Firstly, since the ballast must be designed to give 100% light output for the lamp when the bus voltage is 300V and the frequency is 40kHz, it is not easy to achieve satisfactory preheat and ignition when the bus voltage is at 150V because of the limitations in the peak voltage that the output circuit is able to produce from a 150Vpp half bridge voltage.

One strategy that has been used is to omit the preheating phase and steer the oscillator frequency to resonance during ignition using feedback from the output circuit. This ensures that at switch on the highest possible ignition voltage will be applied to the lamp. In this way the lamp will ignite in whichever position the 3 way switch is set.

Such a scheme could reliably ignite the lamp when the DC bus is at 300V, however without correct preheating the ignition voltage of the lamp and consequently the peak current in the MOSFET half bridge during ignition will be higher. Also the life of the lamp is substantially reduced when there is no preheat due to far greater stress occurring on the cathodes at the point of ignition.

Ignition when the DC bus voltage is at 150V is very difficult. Tests indicated that sweeping the frequency down through resonance failed to produce sufficient ignition voltage leaving the ballast in open circuit running mode with inevitable hard switching at the half bridge. The conclusion from this is that the ballast needs to oscillate at resonance for an extended period of time in order for the lamp to ignite at 150V considering that the output inductor and capacitor have been designed to produce 100% lamp power at 300VDC bus when the frequency is 40-45kHz.

Many CFL ballast designs do not incorporate a current sense and shutdown function to protect the circuit in the case of ignition failure and so the ballast would eventually fail if left switched on due to the high MOSFET switching losses causing thermal destruction. This would not matter with and integrated ballast / lamp type product when the lamp has failed.

It has also been observed that hard switching occurs at the MOSFET half bridge when the DC bus voltage is low in position (1) since when the ballast is running it will be close to resonance, bearing in mind that the resonant frequency shifts downwards in run mode. Hard switching is very undesirable because of the high peak currents that occur when each MOSFET switches on. This has been shown to result in a higher rate of field failures in ballasts due to MOSFET failure.

The conclusion is that the approach to design described above is unable to provide a reliable ballast.
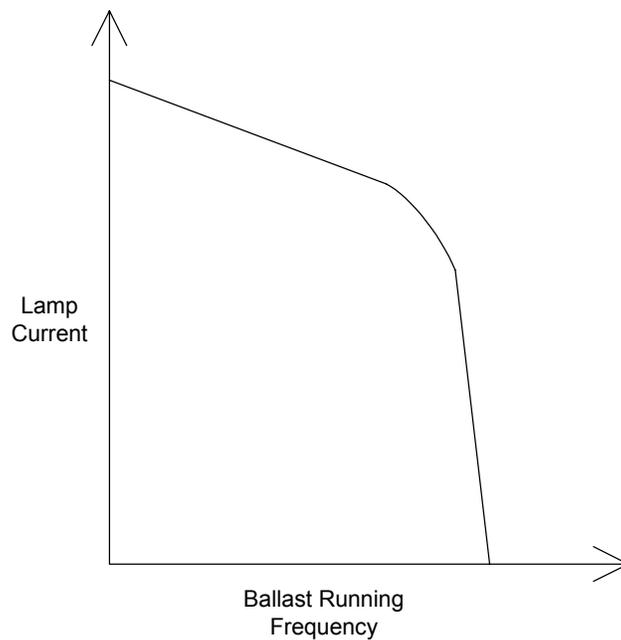
Solution

A completely new approach has been developed that overcomes all of the above limitations based around the popular and versatile IR2156 ballast control I.C.

Functional Description

This solution adopts a completely different approach to the problem. Here we incorporate a voltage doubler at the front end in all modes of operation giving a fixed 300VDC bus. Consequently by choosing correctly the dead time and value of the snubber capacitor it is not difficult to achieve soft switching in all modes of operation.

By simply changing the frequency between 3 defined settings, however, it was found to be extremely difficult to set a point where the dim level is 50%. The problem with this is that the lamp current against ballast frequency characteristic of the system exhibits a very sharp knee such that as the frequency increases the lamp current is gradually reduced up to a point at which a small increase of frequency will result in a very large reduction in the lamp current.
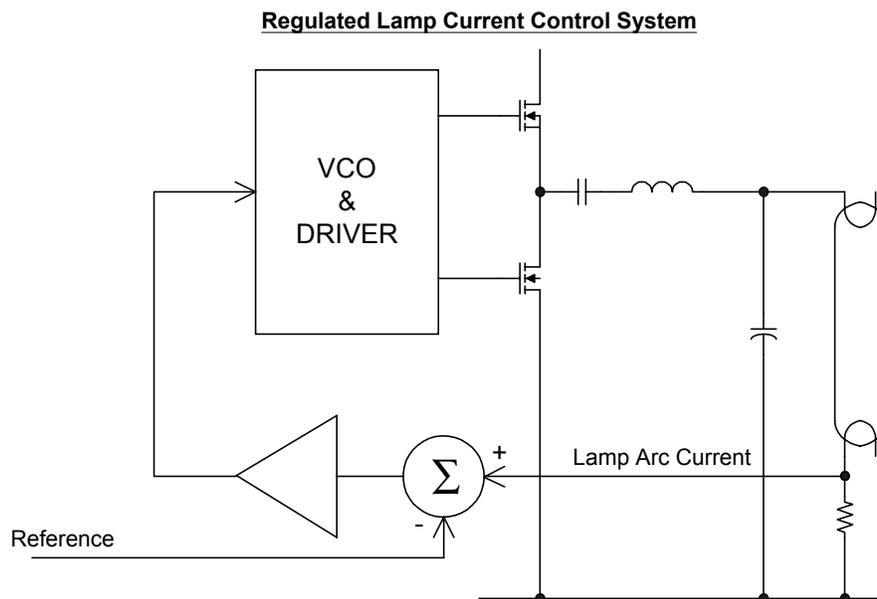
Ballast / Lamp Operating Characteristic

Lamp Current

Ballast Running Frequency

To obtain 50% output the frequency would have to be very precisely set. This is not practical since the tolerances of the output inductor, capacitor and oscillator timing components do not allow this. Even if each ballast was individually adjusted in production variations in lamp behavior over tempera-ture would mean that under some conditions the lamp arc would extinguish at this setting leaving the system in permanent preheat which would burn out the cathodes eventually.

This explains why the 150VDC bus solution has been adopted as this allows 50% output to be achieved without this problem. However the disadvantages discussed in the previous section demon-strate that this approach is not without some major disadvantages.

Consequently it becomes necessary to include a closed loop feedback system that controls the lamp current by adjusting the ballast frequency from a VCO (voltage controlled oscillator) driven by the output of an error amplifier that senses the lamp arc current directly and compares it with a refer-ence. This same strategy has been used in the IRPLCFL3 reference design "A Ballast that can be dimmed from a domestic (phase cut) dimmer" and has been demonstrated to be capable of control-ling the lamp output down to levels below 10% with very good stability. This also compensates for any tolerances in the components of the circuit or the lamp.

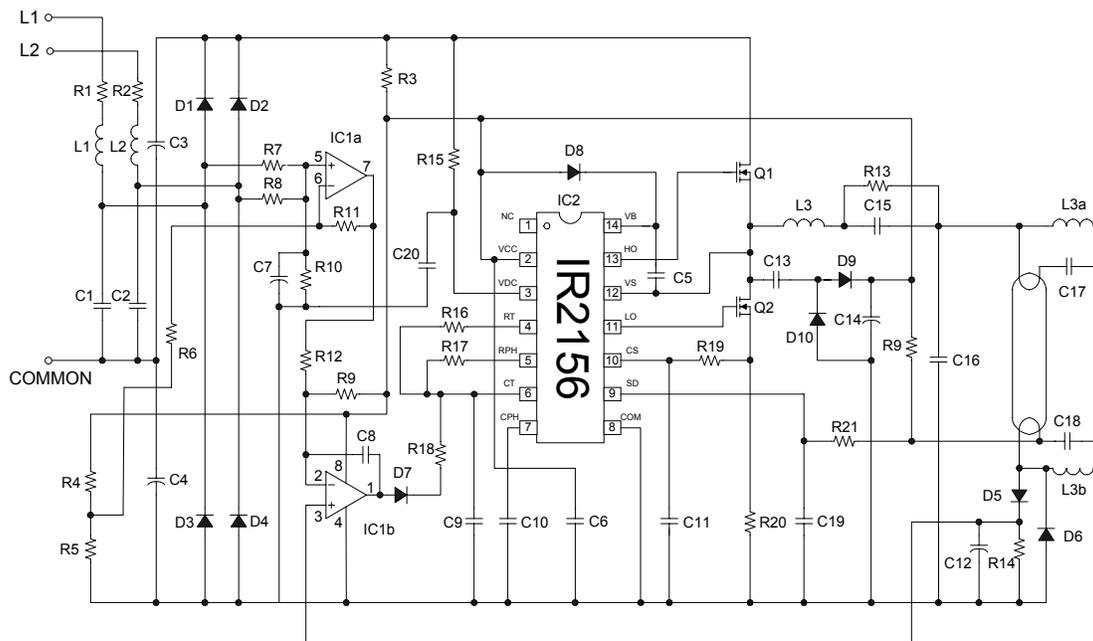**Regulated Lamp Current Control System**

The front end of the ballast shows the neutral line input (i.e. the one that is always connected) going to the center point of the DC bus storage capacitors C3 and C4. Live inputs 1 and 2 are connected to two completely separate voltage doubler diode pairs which are connected to the DC bus. This allows the use of an integrated bridge rectifier or 4 individual diodes, in spite of the fact that the circuit in this case is not a full wave rectifier.

If live input 1 is connected to the line, an 60Hz sinusoidal AC voltage will be present at the point where the anode of D1 joins the cathode of D2. This voltage will swing between the 300V DC bus voltage and the 0V COM point of the circuit. If live input 1 is not connected to the line this point will be floating with no voltage present. The same applies with live input 2 at the point where the anode of D3 meets the cathode of D4. These two points are fed via resistors R7 and R8 to the parallel combination of R10 and C7 which are connected to 0V COM. The value of C7 is high enough to ensure that the amount of ripple that is present at the pin 5 of ICE will be negligible so a DC voltage will effectively appear there. This sets the reference level for the dimming feedback loop.

It follows that this reference voltage will change depending on whether live input 1 is connected only, live input 2 is connected only or both are connected. The values of R7 and R8 will be chosen so that this voltage is substantially different if either live input 1 of live input 2 are connected alone. When both are connected the voltage will be the sum of the voltages produced by each single live input being connected.

For this application in general R7 can be chosen to give the correct reference voltage to provide 50% light output as perceived by the human eye which occurs at a point somewhat lower than 50% ballast power and R8 can be chosen for 75% which is at about 50% of the nominal total ballast power at full light output. The problem here is that these two voltages added together do not produce a high enough reference voltage to give 100% light output when both live inputs are connected. To overcome this an additional opamp has been used which has a reference voltage at pin 6 set at a point above the voltage produced at pin 5 when a single live input is connected and below the voltage at pin 5 when both are connected. The opamp is configured as a non-inverting DC amplifier with a fixed gain so the output will give a higher voltage when both lives are connected and a lower voltage when only one is connected. In this way it is possible by selecting the values of R4, R5, R6 and R11, to achieve any three light levels that may be required.

Circuit Schematic

The closed loop regulation dimming ballast section is identical to that used in the reference design IRFPCFL3. Since we are sensing the lamp arc current with a resistor it is necessary to use voltage mode preheating so as to avoid detecting the sum of the current in the arc and that in the resonant output capacitor C16. This has an additional advantage that during preheat and prior to ignition of the lamp the arc current will always be zero and consequently the feedback circuit will not influence the oscillator frequency at all until the lamp is running. This means that by setting the value of R17 the preheat will occur in exactly the same way regardless of which of the live inputs are connected, thus achieving optimum preheat and ignition under all conditions.

In an integrated CFL design it is not necessary to include R21, R9 and C19 which detect lamp removal or open lower cathode, pin 9 of IC2 SD can be connected directly to COM. Although it is recommended to retain the current sense and shut down at the half bridge provided by R19, R20 and C11, in an integrated CFL these could also be left out and pin 10 CS could be connected directly to COM.

The resistor R13 can be added if necessary to remove *striations* (dark rings) in the lamp that may occur at low dimming levels.

R1 and R2 are fusible resistors that are optional and L1, L2, C1 and C2 are recommended for EMI filtering but have no bearing on the functional operation of the ballast.

Protection Circuits (if included)

The SD pin of the IR2156 is used as lamp removal protection. If there is no lamp present the voltage at SD pin will be pulled above the 5.1V threshold via R9 and R21 charging C19. When a lamp is in circuit the voltage at the junction of R21 and R22 will be held low via D5 and R14.

The current sense resistor R20 has been selected so that if the lamp fails to strike as the frequency approaches resonance in ignition mode, IC2 will shut down thus protecting the Q1 and Q2.

The VDC pin of IC2 is also used connected to the DC bus through R15 with C20 to COM to remove noise. This provides brown out protection for the ballast which works by increasing the frequency when the DC bus drops thus always keeping it above resonance so that hard switching will never occur. Without this protection, if the CS pin is implemented, then the ballast will shut down in the event of any hard switching provided the value of C11 is sufficiently low as not to filter out fast transients. If a brown out occurs and the DC bus briefly falls and hard switching occurs the ballast will shut down and remain off until the line is switched off and then back on again. This is undesirable and with the implementation of the VDC pin of the IR2156 can easily be avoided.

Layout Issues

Care should be taken when laying out this circuit as with any closed loop control system. There should be a star point for all of the 0V returns, particularly IC1 pin 4, IC2 pin 8, R20, C12, R14, D6, C9, C10, C11 and C6, which is then returned to the negative side of C4 via a single track which is as short as possible. This point should as close to IC2 COM pin 8 as possible and C21 should be located as close to IC2 as possible with short tracks. This will avoid potential ground loop problems.

The connecting track from C5 to the MOSFET half-bridge should also be kept short and as far away from the error amplifier as possible. C14 should be close to IC1 and IC2 with short tracks to the positive supply pins to provide maximum decoupling. All tracks carrying HF currents in the output section should be kept away from IC1 and IC2 and associated components.

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Component Selection

The output inductor and capacitor values should be chosen for the ballast to allow it to run at maximum brightness around 40-45kHz. This will minimize losses in the inductor. For this example the *IR Ballast Designer* software * has been used to select the required preheat, ignition and run frequencies for a 25W spiral CFL lamp giving an L3 of 2.2mH and C of 4.7nF.

The values of R16, R17 and C9 have been calculated to give a preheat frequency of 65kHz and a run frequency of 40kHz. The ignition frequency will be around 58kHz.

Output Inductor Design

The output inductor L3 should be designed to allow a high peak ignition current without saturating. This is important as the IR2156 shutdown will be triggered if the inductor saturates. The ignition current depends on the type of lamp being used and must be kept to a minimum by ensuring the preheat is correct. To minimize losses in the inductor multi-stranded wire should be used in combination with Ferrite cores of sufficiently good quality. The best approach to design is to wind as many turns as possible of multi-stranded wire and have the largest gap possible to achieve the correct inductance. This will produce the highest available peak current before saturating the inductor. It is important to bear in mind that when the cores are hot the saturation point and hence the peak current for the inductor will be lower therefore a poorly designed inductor may result in the ballast shutting down during an attempted hot re-strike.

The inductor design process can be greatly simplified by using the *Ballast Designer* software produced by I.R. For this application it is recommended to fix the core size to EF20.

Lamp Preheating

The lamp must be sufficiently preheated before ignition. The correct preheat current can be determined from published data or from International Rectifiers *Ballast Designer* software.

The preheat time can be set by adjusting the value of C10. As a general rule the lamp filament should glow red before ignition. If preheat is insufficient the ballast is likely to shutdown during ignition because the output inductor will be unable to operate at the high current required. The number of turns in the auxiliary cathode windings of the output inductor L2 should be chosen to provide sufficient preheat. In designs for ballasts with integral lamps the shutdown pin can be grounded so that the inductor may saturate without shutting down the circuit.

The lamp filament (Cathode) resistance over the range of dimming levels should be between 3 and 5.5 times the resistance when cold. A simple method for determining the hot resistance is to first connect one cathode to a DC power supply via an ammeter and slowly increase the voltage from zero, noting the current at 1V intervals. This should be done until the cathode can be seen to be glowing red. When this occurs the voltage should not be increased further in order to prevent possible cathode damage. The resistance can then be calculated for each voltage and hence the acceptable voltage range can be found to comply with the 3 to 5.5 times cold resistance, which can be easily measured with a DMM.

Then when the ballast is being run a true RMS digital voltmeter can be connected across one cathode and the voltage can be observed at maximum and minimum brightness. The cathode voltage increases as the ballast is dimmed. The values of C17 and C18 will control how much it increases by, reducing the capacitance will reduce the amount by which the voltage rises. The values should be chosen to prevent the voltage exceeding the upper limit at minimum output.

It is important to bear in mind that using additional windings on the inductor to provide cathode heating means that power is now being transferred through the core and consequently the core losses will increase and hence the core operating temperature. The core will reach its highest operating temperature when the ballast is running at minimum brightness.

The following component values have been selected for a 25W spiral compact lamp. The circuit will need to be optimized for the particular lamp used to obtain best performance.

Bill of Materials

Item #	Qty	Manufacturer	Part Number	Description	Reference
1	1	National Semiconductor	LM358AM	Dual Op Amp	IC1
2	1	International Rectifier	IR2156	Ballast Controller	IC2
3	2	International Rectifier	IRF730	MOSFET	Q1,2
4	1	On Semi	MURS160T	600V 1A Fast Diode SMD	D8
5	5	Microsemi	DL4148	Small Signal Diode SMD	D5,6,7,9,10
6	1	International Rectifier	DF10S	Bridge SMD	D1-4
7	2	Renco	RL-5480-3-2700	Filter Inductor	L1,L2
8	1	B.I. Technologies	HM00-01741	Inductor 2.2mH EF20	L3
9	2	Panasonic	ECQ-E2104KB	100nF 200V	C1,2
10	2	Panasonic	EEU-EB2V220	22uF 200V 105C Electrolytic	C3,4
11	1	Panasonic	ECE-AIVKG220	22uF 35V 105C Electrolytic	C7

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Item #	Qty	Manufacturer	Part Number	Description	Reference
12	2	Panasonic	ECJ-3FCIH103J	10nF 50V 1206	C8,20
13	1	Panasonic	ECU-VIH681KBM	680pF 50V NPO 1206	C9
14	1	Panasonic	ECJ-3VBIE334K	0.33uF 25V 1206	C10
15	1	Panasonic	ECU-VIH471JCH	470pF 50V 1206	C11
16	3	Panasonic	ECJ-3VBIH104K	100nF 50V 1206	C5,6,19
17	2	Panasonic	ECJ-3YB1H224K	220nF 50V 1206	C17,18
18	1	Panasonic	ECKD3A102KBP	1nF 1kV Ceramic	C13
19	1	Panasonic	ECE-AIEF2R2	2.2uF 25V 105C Electrolytic	C14
20	1	Wima	MKS2 Series	47nF 400V	C15
21	1	Wima	MKP4 Series	4.7nF 1kV Polypropylene	C16
22	1	Mallory	TDC474K050NSE	0.47uF 10V Tantalum Bead	C12
23	2	Yageo	CFR-50JB-5R6	5.6R 1W Axial	R1,2
24	2	Yageo	CFR-50JB-1M	1M 0.5W Axial	R7,15
25	1	Yageo	CFR-50JB-220K	220K 0.5W Axial	R3
26	1	Yageo	CFR-50JB-680K	680K 0.5W Axial	R8
27	1	Panasonic	ERJ-8GEYJ683V	68K 1206	R4
28	1	Panasonic	ERJ-8GEYJ332V	3K3 1206	R5
29	1	Yageo	CFR-25JB-100K	100K 0.25W Axial	R21
30	1	Panasonic	ERJ-8GEYJ104V	100K 1206	R6
31	1	Panasonic	ERJ-8GEYJ332V	3K3 1206	R10
32	2	Panasonic	ERJ-8GEYJ103V	10K 1206	R12,18
33	1	Panasonic	ERJ-8GEYJ105V	1M 1206	R9
34	1	Panasonic	ERJ-8GEYJ333V	33K 1206	R16,17
35	1	Panasonic	ERJ-8GEYJ102V	1K 1206	R19
36	1	Panasonic	ERJ-8GEYJ154V	150K 1206	R11
37	1	Dale		0.5R 0.25W Axial	R20
38	1	Panasonic	ERJ-8GEYJ220V	22R 1206	R14
39	1	Not Fitted			R13

- Ballast Designer software may be downloaded free of charge from:
http://ec.irf.com/v6/en/US/direct/ir?cmd=eDownloadBallast

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REVISION HISTORY FOR REFERENCE DESIGN IRPLCFL4

Date	Change
August 8, 2008	Added "Not recommended for new designs – please refer to IRPLCFL8U