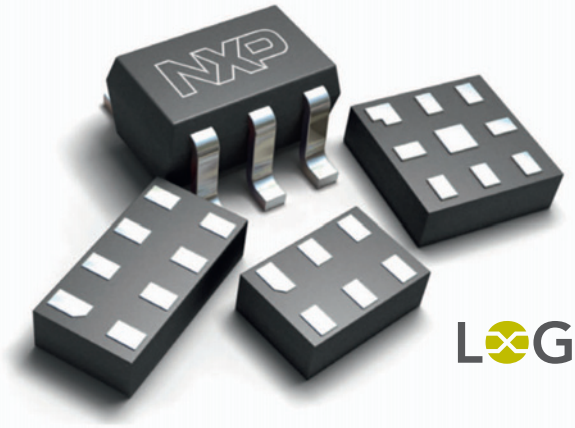


LOGIC^n

NXP ultra-low-power CMOS logic 74AUP1G/2G/3Gxxx

Advanced, ultra-low-power CMOS logic

Designed for high-performance, low-power applications, these low-voltage, Si-gate CMOS devices provide logic solutions with very low static and dynamic power dissipation.

Key features

- Very low dynamic power dissipation (C_{PD})
- t_{pd} of 2.5 ns at V_{cc} of 2.5 V
- Wide supply voltage range (0.8 to 3.6 V)
- Schmitt-trigger action on all inputs
- Low-threshold input options
- 1.9 mA balanced output drive
- Overvoltage-tolerant I/O
- Fully specified (-40 to +85 and -40 to +125 °C)
- Automotive options (-Q100 suffix)
- Pb-free, RoHS-compliant and Dark Green

Benefits

- Low propagation delay
- Suitable for mixed-voltage applications
- High noise immunity
- Extended battery life
- Wide range of functions
- Simplified board layout, mechanical stability

Applications

- Cellular handsets and smartphones
- MP3 players and portable video players
- DSCs and digital camcorders
- Portable devices (laptops, tablets, GPS)
- Consumer entertainment (LCD TVs, DVD+R/W systems, STBs)
- Portable instrumentation

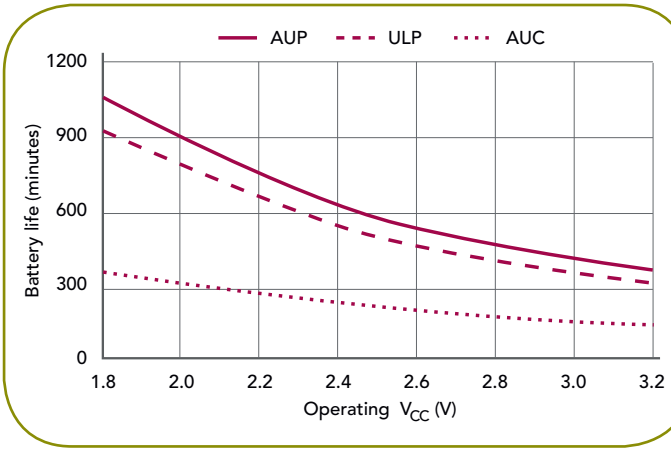
The AUP family of Si-gate CMOS devices uses advanced process technology and next-generation packaging technology to create extremely small functions that consume very little power. The devices are available with one (1G), two (2G), or three (3G) gates.

AUP devices are available in standard, configurable, and combination formats. Special variants are also available, including dual-supply voltage-level translators and devices with low-threshold inputs.

LONGER BATTERY LIFE

On average, the AUP family consumes 30% less power than competing logic families. AUP devices extend battery life by ensuring low power consumption, without sacrificing performance, across the entire V_{cc} range in static and dynamic modes. The typical power dissipation capacitance (C_{PD}) at 1.8 V is only 3.5 pF and at 3.3 V is only 4.3 pF, while the typical propagation delay at 2.5 V is only 2.5 ns.

To save even more battery power, the devices are fully specified for partial power-down applications that use the I_{OFF} feature. The I_{OFF} circuitry disables the output, preventing the damage caused by backflow current passing through the device when it is powered down.



MIXED-VOLTAGE APPLICATIONS

Optimized for 1.8 V applications and operating over a wide supply range of 0.8 to 3.6 V, AUP devices are ideally suited for use in mixed-voltage applications. Inputs that are tolerant to 3.6 V enable a device supplied at 1.8 V to interface between 3.3 and 1.8 V systems. Options with low-threshold inputs (1T) can interface between 1.2 and 3.3 V systems when supplied with 3.3 V. The portfolio also includes dual-supply voltage-level translators in uni- and bidirectional formats. Schmitt-trigger action at all inputs improves noise immunity and makes the circuit tolerant to slower input rise and fall times across the entire range of supply voltage.

CONFIGURABLE LOGIC

A configurable-logic device is a single device that can be configured as any one of up to nine different functions. Examples include standard AND, OR, NAND, NOR, buffers, inverters, and multiplexers, as well as non-standard functions such as a NAND gate with one input inverted.

AUP configurable-logic devices provide design flexibility by integrating nine different functions, including non-standard logic functions, in a single device. Other advantages of configurable logic include reduced PCB space and lower cost. These devices can also reduce the number of types in a bill of materials, simplifying inventory management.

Configurable-logic devices have Schmitt-trigger inputs with fully specified hysteresis, giving them even better noise immunity than the standard part types.

COMBINATION LOGIC

Combination logic offers two or more unique functions in a single package. The functions are either stand alone or internally cascaded.

Figure 1a illustrates standalone operation, with the buffer and the inverter having no internal connection. Figure 1b illustrates the cascaded option, with the output of the AND gate internally applied as an input to the OR gate.

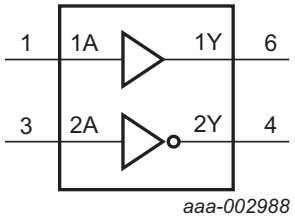


Figure 1a: stand alone combination logic

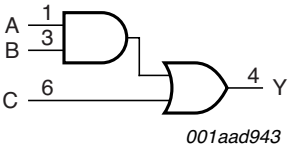


Figure 1b: internally cascaded combination logic

Solutions based on combination logic have lower total cost, including pick and place cost, and reduced PCB area. Combination logic also helps to optimize and simplify the PCB layout and signal routing.

AUP portfolio

Type number	Description	Features							Package (suffix)															
		Low threshold inputs	Schmitt trigger inputs	Schmitt trigger action	3.6 V tolerant I/O's	Open-drain output	Power-off protection (I_{OFF})	Dual supply translator	SOT353-1 (GW)	SOT363 (GW)	SOT753 (GV)	SOT765-1 (DC)	SOT833-1 (GT)	SOT886 (GM)	SOT891 (GF)	SOT902-2 (GM)	SOT996-2 (GD)	SOT1081 (GF)	SOT1089 (GF)	SOT1115 (GN)	SOT1116 (GN)	SOT1202 (GS)	SOT1203 (GS)	SOT1226 (GX)
Configurable																								
74AUP1G57	Single configurable multi-function gate		•		•		•			•				•	•					•		•		
74AUP1G58	Single configurable multi-function gate		•		•		•			•				•	•					•		•		
74AUP1G97	Single configurable multi-function gate		•		•		•			•				•	•					•		•		
74AUP1G98	Single configurable multi-function gate		•		•		•			•				•	•					•		•		
74AUP1T57	Single configurable multi-function gate	•	•		•		•			•				•	•					•		•		
74AUP1T58	Single configurable multi-function gate	•	•		•		•			•				•	•					•		•		
74AUP1T97	Single configurable multi-function gate	•	•		•		•			•				•	•					•		•		
74AUP1T98	Single configurable multi-function gate	•	•		•		•			•				•	•					•		•		
Combination																								
74AUP1G0832	Single 3-input AND-OR gate			•	•		•			•				•	•					•		•		
74AUP1G3208	Single 3-input OR-AND gate			•	•		•			•				•	•					•		•		
74AUP1G885	Single dual-function gate			•	•		•					•	•			•	•	•			•		•	
74AUP1Z04	X-tal driver with enable			•	•		•			•				•	•					•		•		
74AUP1Z125	X-tal driver with enable; 3-state			•	•		•			•				•	•					•		•		
74AUP2G0604	Inverter; open drain and inverter			•	•	•	•			•				•	•					•		•		
74AUP2G3404	Buffer and inverter			•	•		•			•				•	•					•		•		
74AUP2T1326GF	Dual supply buffer/line driver; 3-state			•	•		•	•											•					
74AUP3G0434	Dual inverter and single buffer			•	•		•					•	•			•	•	•			•		•	
74AUP3G3404	Dual buffer and single inverter			•	•		•					•	•			•	•	•			•		•	
Buffers/inverters																								
74AUP1G04	Single inverter			•	•		•		•		•			•	•					•		•		•
74AUP1G06	Single inverter; open drain			•	•	•	•		•					•	•					•		•		•
74AUP1G07	Single buffer; open drain			•	•	•	•		•					•	•					•		•		•
74AUP1G125	Single buffer/line driver; 3-state			•	•		•		•					•	•					•		•		•
74AUP1G126	Single buffer/line driver; 3-state			•	•		•		•					•	•					•		•		•
74AUP1G14	Single inverter; Schmitt trigger		•		•		•		•					•	•					•		•		•
74AUP1G17	Single buffer; Schmitt trigger		•		•		•		•					•	•					•		•		•
74AUP1G240	Single inverter/line driver; 3-state			•	•		•		•					•	•					•		•		•
74AUP1G34	Single buffer			•	•		•		•					•	•					•		•		•
74AUP1GU04	Single unbuffered inverter			•	•		•		•					•	•					•		•		•
74AUP1T34	Single translating buffer			•	•		•	•	•					•	•					•		•		
74AUP2G04	Dual inverter			•	•		•			•				•	•					•		•		
74AUP2G06	Dual inverter; open drain			•	•	•	•			•				•	•					•		•		
74AUP2G07	Dual buffer; open drain			•	•	•	•			•				•	•					•		•		
74AUP2G125	Dual buffer/line driver; 3-state			•	•		•					•	•			•	•	•			•		•	
74AUP2G126	Dual buffer/line driver; 3-state			•	•		•					•	•			•	•	•			•		•	
74AUP2G14	Dual inverter; Schmitt trigger		•		•		•			•				•	•					•		•		
74AUP2G157	Single 2-input multiplexer			•	•		•					•	•			•	•	•			•		•	
74AUP2G17	Dual buffer; Schmitt trigger		•		•		•			•				•	•					•		•		
74AUP2G240	Dual inverter/line driver; 3-state			•	•		•					•	•			•	•	•			•		•	
74AUP2G241	Dual buffer/line driver; 3-state			•	•		•					•	•			•	•	•			•		•	
74AUP2G34	Dual buffer			•	•		•			•				•	•					•		•		
74AUP2GU04	Dual unbuffered inverter			•	•		•			•				•	•					•		•		
74AUP3G04	Triple inverter			•	•		•					•	•			•	•	•			•		•	

More information available at
www.nxp.com/products/logic/gates/configurable_multiple_function_gates/
www.nxp.com/products/logic/gates/combination/
www.nxp.com/products/logic/buffers_inverters_drivers/

AUP portfolio (continued)

Type number	Description	Features							Package (suffix)																
		Low threshold inputs	Schmitt trigger inputs	Schmitt trigger action	3.6 V tolerant I/O's	Open-drain output	Power-off protection (I_{OFF})	Dual supply translator	SOT353-1 (GW)	SOT363 (GW)	SOT753 (GV)	SOT765-1 (DC)	SOT833-1 (GT)	SOT886 (GM)	SOT891 (GF)	SOT902-2 (GM)	SOT996-2 (GD)	SOT1081 (GF)	SOT1089 (GF)	SOT1115 (GN)	SOT1116 (GN)	SOT1202 (GS)	SOT1203 (GS)	SOT1226 (GX)
Gates																								
74AUP1G00	Single 2-input NAND gate			•	•		•		•					•	•					•		•		•
74AUP1G02	Single 2-input NOR gate			•	•		•		•					•	•					•		•		•
74AUP1G08	Single 2-input AND gate			•	•		•		•					•	•					•		•		•
74AUP1G09	Single 2-input AND gate; open drain			•	•	•	•		•					•	•					•		•		•
74AUP1G11	Single 3-input AND gate			•	•		•		•					•	•					•		•		•
74AUP1G132	Single 2-input NAND gate; Schmitt trigger		•		•		•		•					•	•					•		•		•
74AUP1G32	Single 2-input OR-gate			•	•		•		•					•	•					•		•		•
74AUP1G332	Single 3-input OR-gate			•	•		•			•				•	•					•		•		
74AUP1G38	Single 2-input NAND-gate; open drain			•	•	•	•		•					•	•					•		•		•
74AUP1G386	Single 3-input EXCLUSIVE-OR gate			•	•		•			•				•	•					•		•		
74AUP1G86	Single 2-input EXCLUSIVE-OR gate			•	•		•		•					•	•					•		•		•
74AUP2G00	Dual 2-input NAND gate			•	•		•					•	•			•	•	•			•		•	
74AUP2G02	Dual 2-input NOR gate			•	•		•					•	•			•	•	•			•		•	
74AUP2G08	Dual 2-input AND gate			•	•		•					•	•			•	•	•			•		•	
74AUP2G132	Dual 2-input NAND gate; Schmitt trigger		•		•		•					•	•			•	•	•			•		•	
74AUP2G32	Dual 2-input OR gate			•	•		•					•	•			•	•	•			•		•	
74AUP2G38	Dual 2-input NAND gate; open drain			•	•	•	•					•	•			•	•	•			•		•	
74AUP2G86	Dual 2-input EXCLUSIVE-OR gate			•	•		•					•	•			•	•	•			•		•	
Flip-flops																								
74AUP1G175	Single D-type flip-flop with reset			•	•		•			•				•	•					•		•		
74AUP1G374	Single D-type flip-flop; 3-state			•	•		•			•				•	•					•		•		
74AUP1G74	Single D-type flip-flop with set and reset			•	•		•					•	•			•	•	•			•		•	
74AUP1G79	Single D-type flip-flop			•	•		•		•		•			•	•					•		•		•
74AUP1G80	Single D-type flip-flop			•	•		•		•					•	•					•		•		
74AUP2G79	Dual D-type flip-flop			•	•		•					•	•			•	•	•			•		•	
74AUP2G80	Dual D-type flip-flop			•	•		•					•	•			•	•	•			•		•	
Latches																								
74AUP1G373	Single D-type transparent latch; 3-state			•	•		•			•				•	•					•		•		
Multiplexers																								
74AUP1G157	Single 2-input multiplexer			•	•		•			•				•	•					•		•		
74AUP1G158	Single 2-input multiplexer; inverting			•	•		•			•				•	•					•		•		
Demultiplexers																								
74AUP1G18	Single 1-of-2 demultiplexer; 3-state			•	•		•			•				•	•					•		•		
74AUP1G19	Single 1-of-2 decoder/demultiplexer			•	•		•			•				•	•					•		•		
Transceivers																								
74AUP1T45	Single translating transceiver; 3-state			•	•		•	•	•					•	•					•		•		

More information available at
www.nxp.com/products/logic/gates/
www.nxp.com/products/logic/flip_flops/
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More about the AUP family
www.nxp.com/products/logic/family/AUP/

PACKAGES

AUP devices are available in PicoGate and MicroPak packages, which are roughly ten times smaller than a conventional SO14 package. PicoGate and MicroPak products reduce time-to-market by making it easy to implement last-minute changes. They also improve the cost-effectiveness of crowded layouts, because they simplify routing and eliminate dependences in intricate line-layout patterns.

The AUP family operates over an extended temperature range (-40 to +125 °C), so they're suitable for a wide range of applications, including portable, consumer, military, and automotive (-Q100 variants). Multi-pin packages with 5, 6, or 8 pins make it easy to select the right combination of features, packages, and performance.

NXP's new Diamond package (suffix GX) is over 25 percent smaller than our XSON package (suffix GN), which was previously the world's smallest package. Yet, while this game-changing Diamond package is a tiny 0.8 mm square by only 0.35 mm high, its breakthrough design retains the traditional 0.5 mm pad pitch, so it eliminates the need for expensive step-down solder masks and allows simplified PCB assembly.

Package summary

Package suffix	GW	GV	GX	GW	GM	GF	GN	GS
	5-pin	5-pin	5-pin	6-pin	6-pin	6-pin	6-pin	6-pin
								
Package	SOT353-1	SOT753	SOT1226	SOT363	SOT886	SOT891	SOT1115	SOT1202
Width (mm)	2.10	2.75	0.80	2.10	1.00	1.00	1.00	1.00
Length (mm)	2.00	2.90	0.80	2.00	1.45	1.00	0.90	1.00
Height (mm)	1.00	1.00	0.35	1.00	0.50	0.50	0.35	0.35
Pitch (mm)	0.65	0.95	0.50	0.65	0.50	0.35	0.35	0.35

Package suffix	DC	GT	GM	GD	GF	GN	GS	GF
	8-pin	8-pin	8-pin	8-pin	8-pin	8-pin	8-pin	10-pin
								
Package	SOT765-1	SOT833-1	SOT902-2	SOT996-2	SOT1089	SOT1116	SOT1203	SOT1081-2
Width (mm)	3.10	1.00	1.60	3.00	1.00	1.00	1.00	1.00
Length (mm)	2.00	1.95	1.60	2.00	1.35	1.20	1.35	1.70
Height (mm)	1.00	0.50	0.50	0.50	0.50	0.35	0.35	0.50
Pitch (mm)	0.50	0.50	0.50	0.50	0.35	0.30	0.35	0.35

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