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Scatter-Gather Direct Memory Access (DMA) Controller

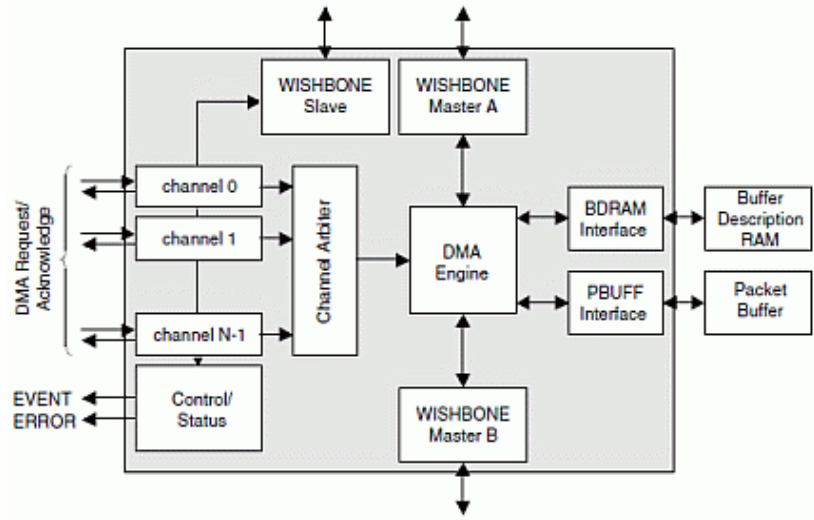
Direct Memory Access (DMA) is a technique for transferring blocks of data between system memory and peripherals without a processor (e.g., system CPU) having to be involved in each transfer. DMA not only offloads a system's processing elements, but can transfer data at much higher rates than processor reads and writes.



Scatter-Gather DMA augments this technique by providing data transfers from one non-contiguous block of memory to another by means of a series of smaller contiguous-block transfers. The Lattice Scatter-Gather DMA Controller core implements a configurable, multi-channel, WISHBONE-compliant DMA controller with scatter-gather capability.

Features

- Supports up to 16 physical channels
- Up to 8 sub-channels per physical channel
- Four priority levels using round-robin arbitration (weighted or simple)
- WISHBONE bus widths from 8 to 128 bits
- Simple DMA, split transfers, scatter-gather
- Direct interface to external RAM for packet buffering
- Autonomous and hardware-directed retry
- Supports WISHBONE burst and classic-cycle transfers
- Supports centralized and distributed DMA control architectures



Performance and Resource Utilization

LatticeECP3¹

IPexpress User-Configurable Mode	SLICES	LUTs	Registers	f _{MAX} (MHz)
Config 3	2117	3591	1300	149

1. Performance and utilization data are generated using an LFE3-95E-7FN672CES device with Lattice Diamond 1.0 software using Synopsys Synplify Pro for Lattice D-2009.12L-1. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M¹

IPexpress User-Configurable Mode	SLICES	LUTs	Registers	f _{MAX} (MHz)
Config 1	2169	3464	1345	133

1. Performance and utilization data are generated using an LFE2M35E/SE-6F672C device with Lattice Diamond 1.0 software using Synopsys Synplify Pro for Lattice D-2009.12L-1. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M/S family.

LatticeECP2¹

IPexpress User-Configurable Mode	SLICES	LUTs	Registers	f _{MAX} (MHz)
Config 2	2963	4838	1713	149

1. Performance and utilization data are generated using an LFE2-35E/SE-6F672C device with Lattice Diamond 1.0 software using Synopsys Synplify Pro for Lattice D-2009.12L-1. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2 family.

LatticeSC/M¹

IPexpress User-Configurable Mode	SLICES	LUTs	Registers	f _{MAX} (MHz)
Config 0	2879	4515	1881	231
Config 1	2249	3627	1364	230
Config 2	3004	4861	1768	199
Config 3	2206	3641	1318	224

1. Performance and utilization data are generated using an LFSC3GA25E-6FF1020C device with Lattice Diamond 1.0 software using Synopsys Synplify Pro for Lattice D-2009.12L-1. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeSC/M family.

LatticeXP2¹

IPexpress User-Configurable Mode	SLICES	LUTs	Registers	f _{MAX} (MHz)
Config 3	2177	3566	1279	109

1. Performance and utilization data are generated using an LFXP2-40E-6F672C device with Lattice Diamond 1.0 software using Synopsys Synplify Pro for Lattice D-2009.12L-1. Performance may vary when using a different software version or targeting a different device density or speed grade within the LatticeXP2 family.

Ordering Information

Family	Part Number
LatticeECP3	DMA-SG-E3-U1
LatticeECP2M	DMA-SG-PM-U1
LatticeECP2	DMA-SG-E2-U1
LatticeSC	DMA-SG-SC-U1
LatticeXP2	DMA-SG-X2-U1

IP Version: 2.5

Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible. For more information on viewing/downloading IP please read the [IP Express Quick Start Guide](#).

Purchase: To find out how to purchase the IP Core, please contact your [local Lattice Sales Office](#).