

# FDZ298N

## N-Channel 2.5 V Specified PowerTrench® BGA MOSFET

### General Description

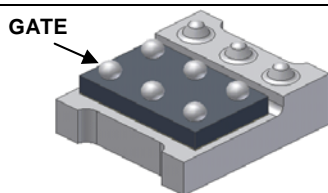
Combining Fairchild's advanced 2.5V specified PowerTrench process with state of the art BGA packaging, the FDZ298N minimizes both PCB space and  $R_{DS(ON)}$ . This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low  $R_{DS(ON)}$ .

### Applications

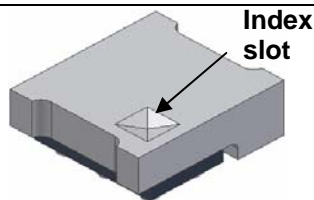
- Battery management
- Battery protection

### Features

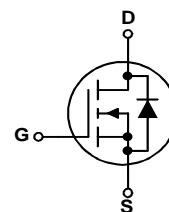
- 6 A, 20 V  $R_{DS(ON)} = 27 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$   
 $R_{DS(ON)} = 39 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- Occupies only 2.25 mm<sup>2</sup> of PCB area.  
Less than 50% of the area of a SSOT-6
- Ultra-thin package: less than 0.80 mm height when mounted to PCB
- Outstanding thermal transfer characteristics:  
4 times better than SSOT-6
- Ultra-low  $Q_g \times R_{DS(ON)}$  figure-of-merit
- High power and current handling capability.



Bottom



Top



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1a)	6	A
		10	
$P_D$	Power Dissipation for Single Operation (Note 1a)	1.7	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	72	$^\circ\text{C/W}$
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### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
C	FDZ298N	7"	8mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-0.3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 2.5\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 4.5\text{ V}, I_D = 6\text{ A}, T_J = 125^\circ\text{C}$		23 28 28	27 39 42	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	10			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 6\text{ A}$		24		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		680		pF
$C_{oss}$	Output Capacitance			165		pF
$C_{riss}$	Reverse Transfer Capacitance			90		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.9		$\Omega$

**Switching Characteristics** (Note 2)

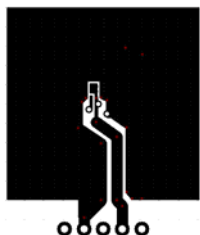
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		8	16	ns
$t_r$	Turn–On Rise Time			7	14	ns
$t_{d(off)}$	Turn–Off Delay Time			14	26	ns
$t_f$	Turn–Off Fall Time			6	12	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 6\text{ A},$ $V_{GS} = 4.5\text{ V}$		7	10	nC
$Q_{gs}$	Gate–Source Charge			1.4		nC
$Q_{gd}$	Gate–Drain Charge			1.8		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain–Source Diode Forward Current			1.4	A	
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.4\text{ A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 6\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		14		nS
$Q_{rr}$	Diode Reverse Recovery Charge			3		nC

**Notes:**

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball,  $R_{\theta JB}$ , is defined for reference. For  $R_{\theta JC}$ , the thermal reference point for the case is defined as the top surface of the copper chip carrier.  $R_{\theta JC}$  and  $R_{\theta JB}$  are guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



- 72 $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB



- 157 $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

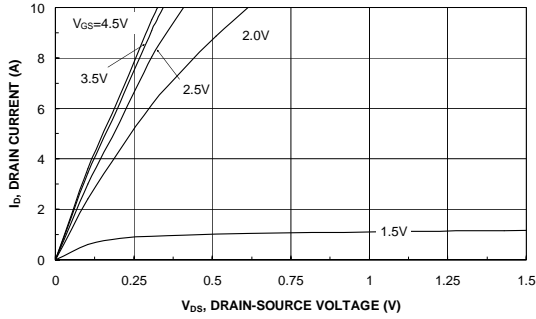


Figure 1. On-Region Characteristics.

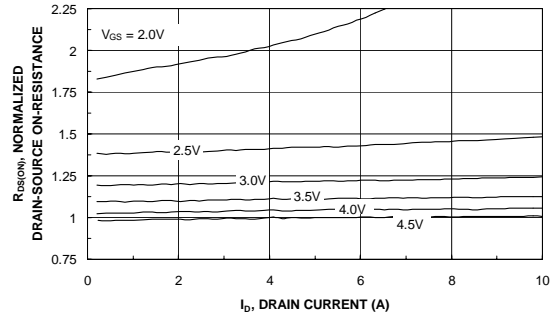


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

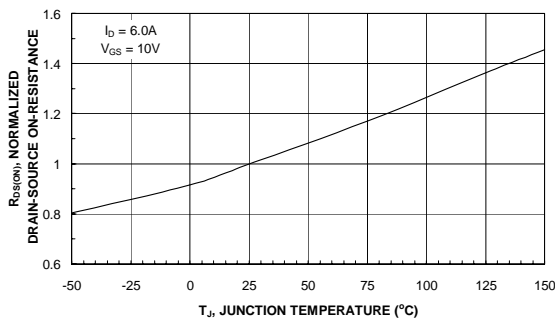


Figure 3. On-Resistance Variation with Temperature.

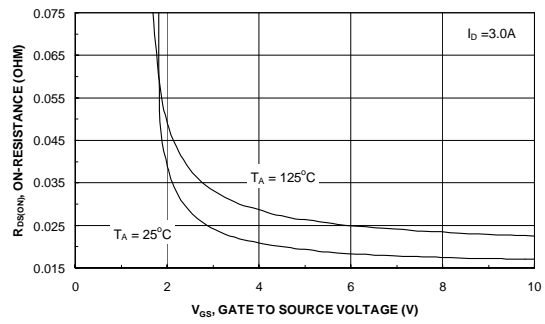


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

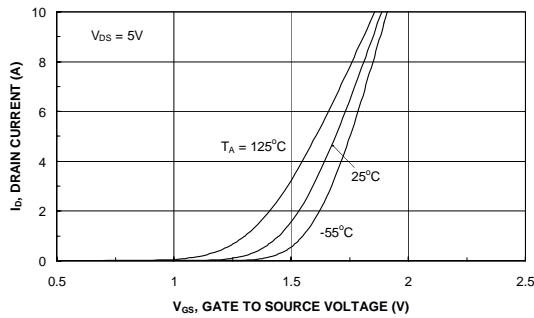


Figure 5. Transfer Characteristics.

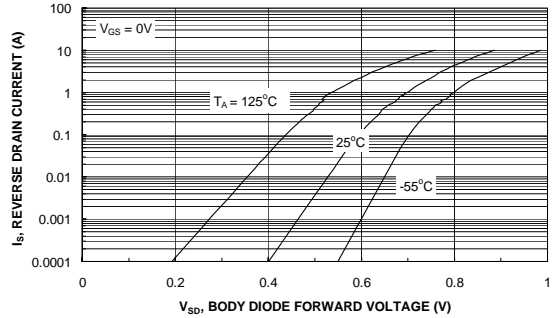


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## Typical Characteristics

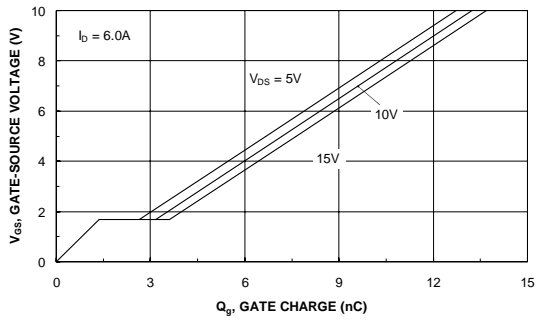


Figure 7. Gate Charge Characteristics.

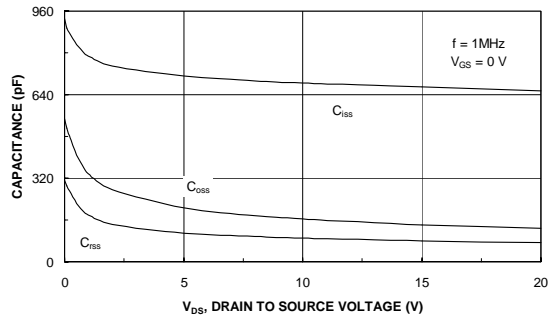


Figure 8. Capacitance Characteristics.

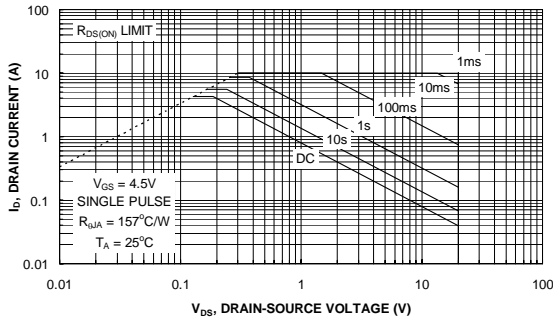


Figure 9. Maximum Safe Operating Area.

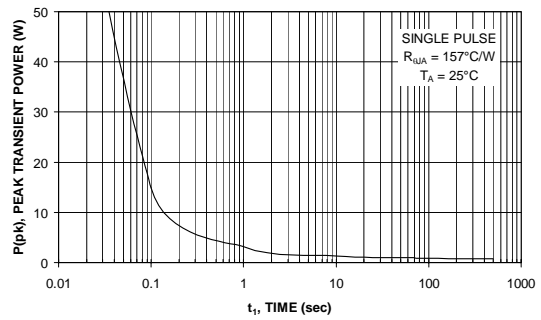
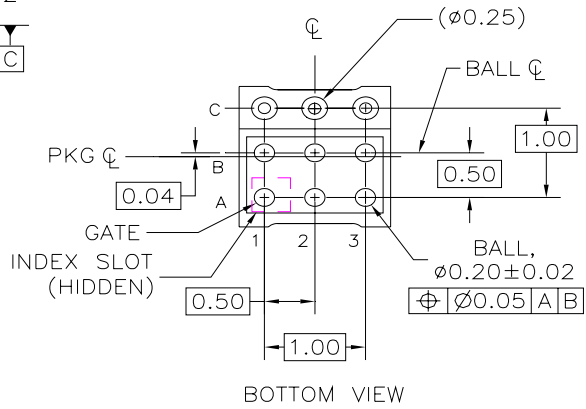
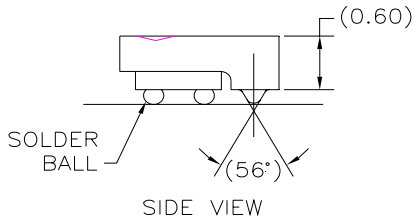
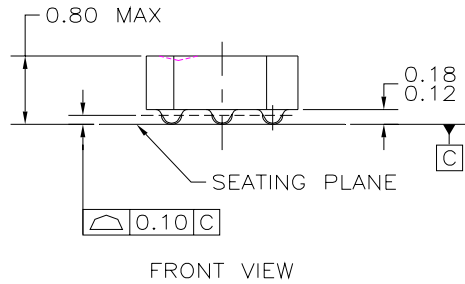
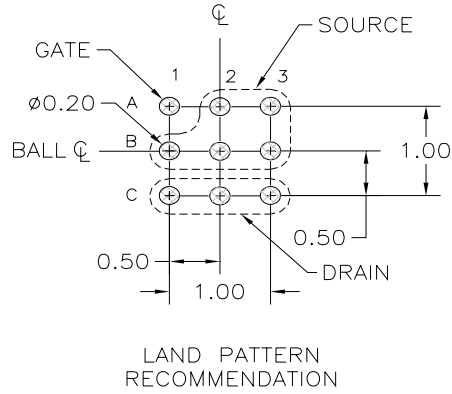
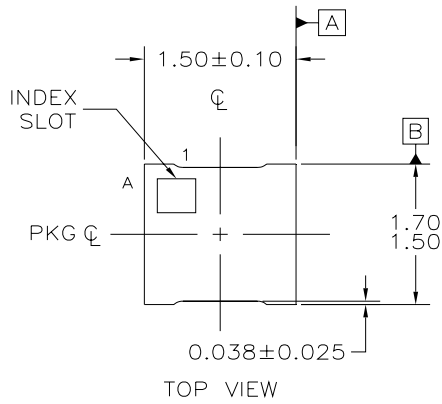


Figure 10. Single Pulse Maximum Power Dissipation.

### Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

### Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.
- C) BALL/STUD CONFIGURATION TABLE

TERMINAL ID	DESIGNATION	TERMINAL TYPE
C1,C2,C3	DRAIN	COPPER STUD
A1	GATE	BALL
A2,A3,B1,B2,B3	SOURCE	BALL

BGA06AREVF

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E <sup>2</sup> C MOS™	ꝑC™	MSX™	QT Optoelectronics™	TinyLogic®
EnSigna™	i-Lo™	MSXPro™	Quiet Series™	TINYOPTO™
FACT™	ImpliedDisconnect™	OCX™	RapidConfigure™	TruTranslation™
FACT Quiet Series™		OCXPro™	RapidConnect™	UHC™
Across the board. Around the world.™		OPTOLOGIC®	µSerDes™	UltraFET®
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Programmable Active Droop™		PACMAN™	SMART START™	VCX™

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