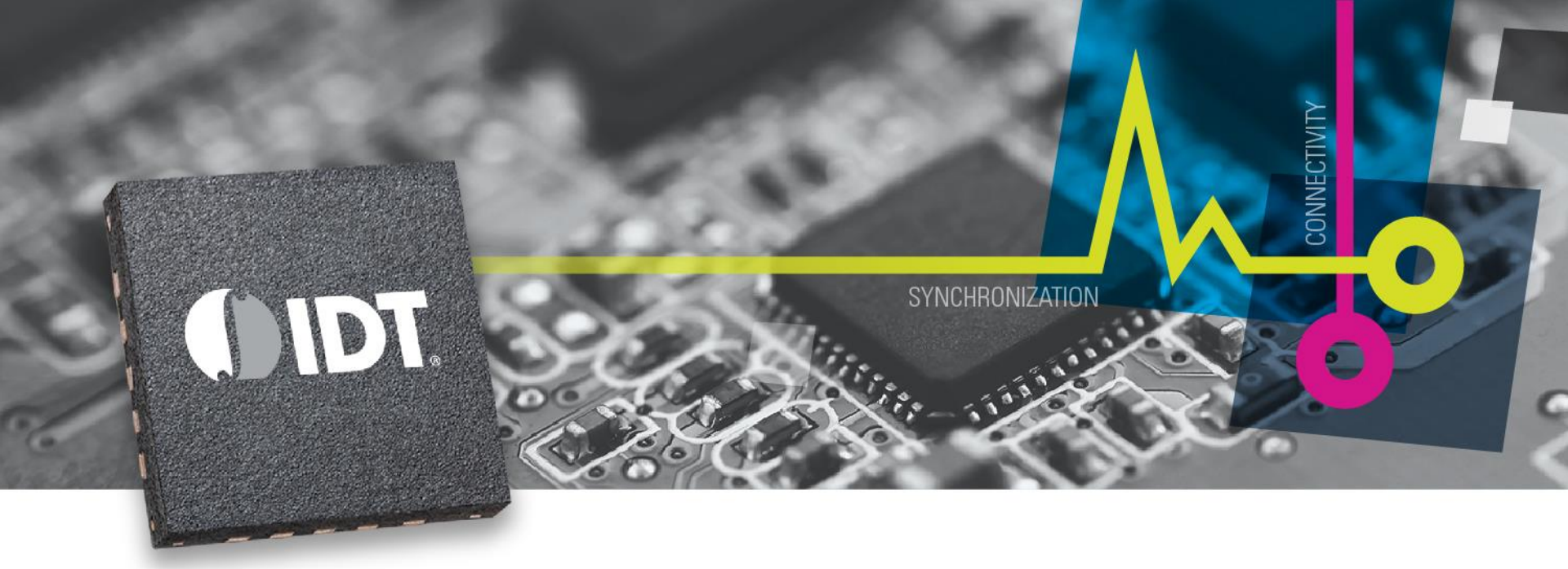

Channel NPI

8V19N490 FemtoClock® NG Jitter Attenuator and Clock Synthesizer
8V79S680 JESD204B-compliant Fanout Buffer and Divider

February 2018

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8V19N490 Overview

Low Phase Noise Clock Generation for 5G New Radio

Features

- High clock frequency generation
- Low phase noise <80fs RMS and high spurious attenuation of 90dBc
- Synchronized 18 outputs with deterministic I/O latency
- Phase stability over temperature
- Build-in SYSREF generation

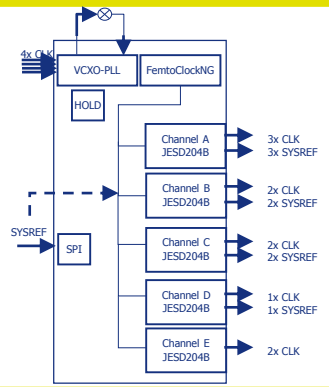
Benefits

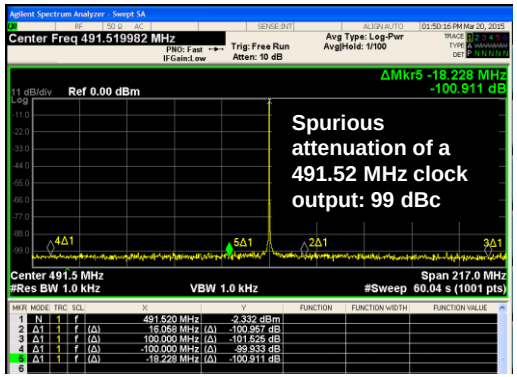
- Supports RF-DAC clocks up to 2.94912GHz
- Supports best EVM radio designs
- Single chip solution for 4T4R-16T16R
- 64T64R and higher: 8V79S680 or cascaded PLL operation
- Best for clock generation in AAS and MIMO systems
- JESD204B subclass 0/1 converter synchronization

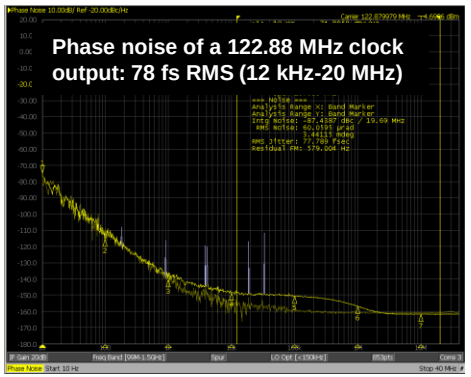
Applications

- 5G Radio clock jitter attenuation, frequency generation and clock/SYSREF distribution
- JESD204B ADC/DAC converter clocking

Supports New Radio Designs with Lowest Phase Noise Clock Signals







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8V79S680 Overview

JESD204B-compliant Clock/SYREF Distribution for 5G New Radio

Features

- High clock/SYSREF signal fanout
- Low additive phase noise <100fs RMS and low noise floor <-160dBc/Hz
- Synchronized 16 outputs with deterministic I/O latency
- Additional fanout for 8V19N490
- Phase stability over temperature
- High clock frequency <3 GHz

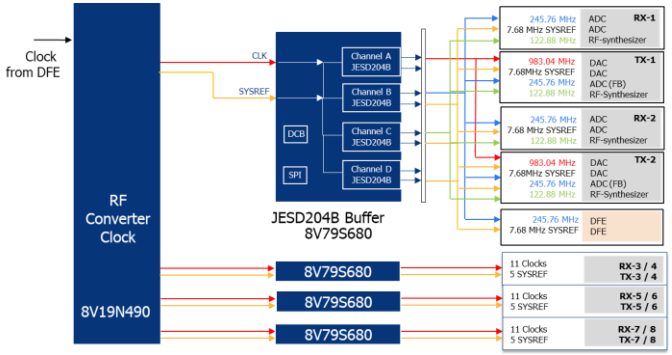
Benefits

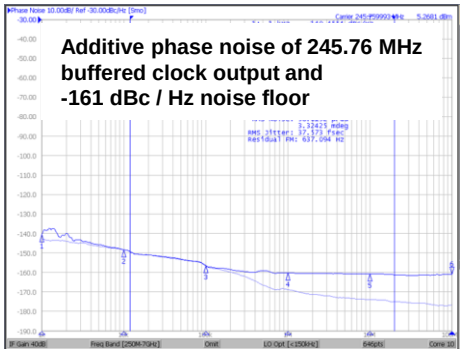
- Solution for 64T64R and higher
- Supports best EVM radio designs
- Best for clock generation in AAS and MIMO systems
- JESD204B subclass 0/1 converter synchronization
- Supports RF-DAC clocks up to 2.94912 GHz

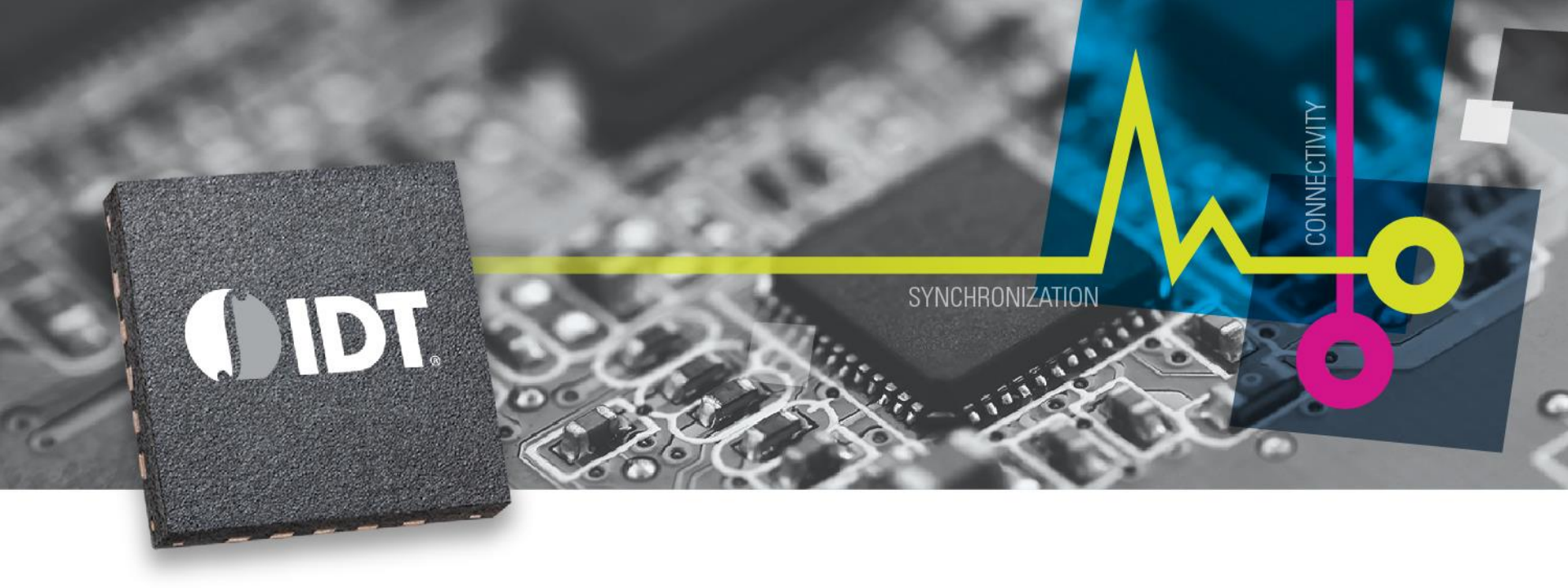
Applications

- 5G Radio clock/SYSREF signal distribution
- JESD204B ADC/DAC converter clocking

Supports New Radio Designs with High Fanout Clock Distribution







Thank You

Analog Mixed Signal Product Leadership in Growth Markets

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