Dimmable, Low Noise, 16 channel EL Lamp Driver

Features

- Sixteen channel EL lamp driver with single common terminal
- 1nF maximum load on each of the sixteen channels
- Independent dimming capability for all lamps
- Sixteen brightness levels for each lamp
- 1.8 to 5.5V operating supply range
- 1.7V logic interface
- Dedicated enable logic pin
- $340V_{P-P}$ nominal output voltage for high brightness
- Low audible noise
- Output voltage regulation
- EL1 - EL16 outputs fall time control
- Two EL frequency controls
- External switching MOSFET
- I^2C data communication control
- Single lithium-ion cell compatible
- One miniature inductor to power sixteen lamps
- Independent lamp and converter frequency setting
- Split supply capability
- 5x5mm, 32-Lead QFN package

Applications

- Multi-segment, variable displays
- Cell phone keypads and displays
- Multi-segment remote controls
- Handheld wireless communication products
- Global Positioning Systems (GPS)

General Description

The Supertex HV881 is a 16 channel EL lamp driver with a single common terminal. It can drive up to a 1nF EL lamp load (approx. 0.3in2 lamp size) on each of the sixteen channels. The input supply voltage range is 1.8 to 5.5V. The logic interface to the device can be as low as 1.7V. The device has an enable logic input pin to turn the device on or off.

The device is designed to minimize audible noise emitted by the EL lamp. The HV881 uses an external MOSFET, a single inductor and minimum number of passive components to drive all sixteen EL lamps. The device is designed such that the input voltage to the inductor can be different from the input voltage to the device (split supply).

The HV881 has two internal oscillators and a high voltage EL lamp driver. An external MOSFET is driven by the switch oscillator to generate output voltage.

The frequency for the external switching MOSFET is set by an external resistor connected between the RSW-Osc pin and the VDD supply pin. The EL lamp driver frequency can be set by either an external logic signal frequency at the SEL pin or by an external resistor connected between the REL-Osc pin and VDD pin. If external frequency is input at the SEL pin, the REL-Osc pin should be connected to ground.

An external inductor is connected between the LX and VDD or VIN pins for split supply applications. Depending upon the EL lamp sizes, a 1.0 to 10.0nF capacitor is connected between the CS pin and ground. The C_S capacitor is connected to the internal H-bridge, and the energy stored in the capacitor is therefore transferred to the EL lamp. One side of all the sixteen EL lamps is connected to the respective EL pins (EL1, EL2, etc.), and the other side is connected to the COM pin.

The external switching MOSFET charges the inductor and discharges it into the capacitor at CS. The voltage at CS will start to increase. Once the voltage at CS reaches the desired regulation limit, the external switching MOSFET is turned off to conserve power.

The HV881 allows for controlling the fall time of the EL1 - EL16 outputs by an external resistor from the RSLOPE pin to the VDD pin. This feature can be used to reduce the audible noise of the EL lamp or to increase the lamp brightness.

The brightness of each of the sixteen EL lamps can be independently controlled to have one of fifteen brightness levels or can be completely turned off by the serial data (SDA) input. The serial data input has a 4-bit binary code for each lamp, to control the brightness level from level 0 to level 15. The brightness is controlled by controlling the number of EL frequency cycles (from 0 to 15) in a group of 15 cycles.

Ordering Information

Device	32-Lead QFN *5.00x5.00mm body* *0.8mm height (max)* *0.50mm pitch*
HV881	HV881K7-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{DD}, supply voltage	-0.5 to 7.0V
EN, SDA, SCL, S_{EL}	-0.5 to V_{DD} +0.5V
V_{CS}, output voltage	-0.5 to 215V
V_{REG}, external input voltage	0.48V
Storage temperature	-65°C to +150°C
Maximum junction temperature	+125°C

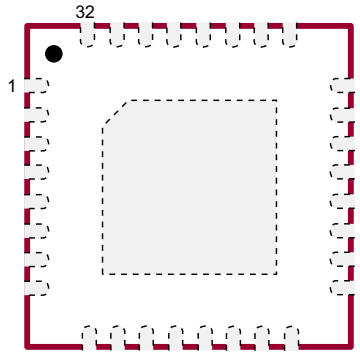
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Thermal Resistance

Package	θ_{ja}
32-Lead QFN	25°C/W

(Mounted on 4-layer FR4 9-via PCB, 76mm x 114mm x 1.44mm)

Pin Configuration



32-Lead QFN Package
(top view)

Note:
Pads are at the bottom of the package. Center heat slug is at ground potential.

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

32-Lead QFN Package

Package may or may not include the following marks: Si or

Recommended Operating Conditions

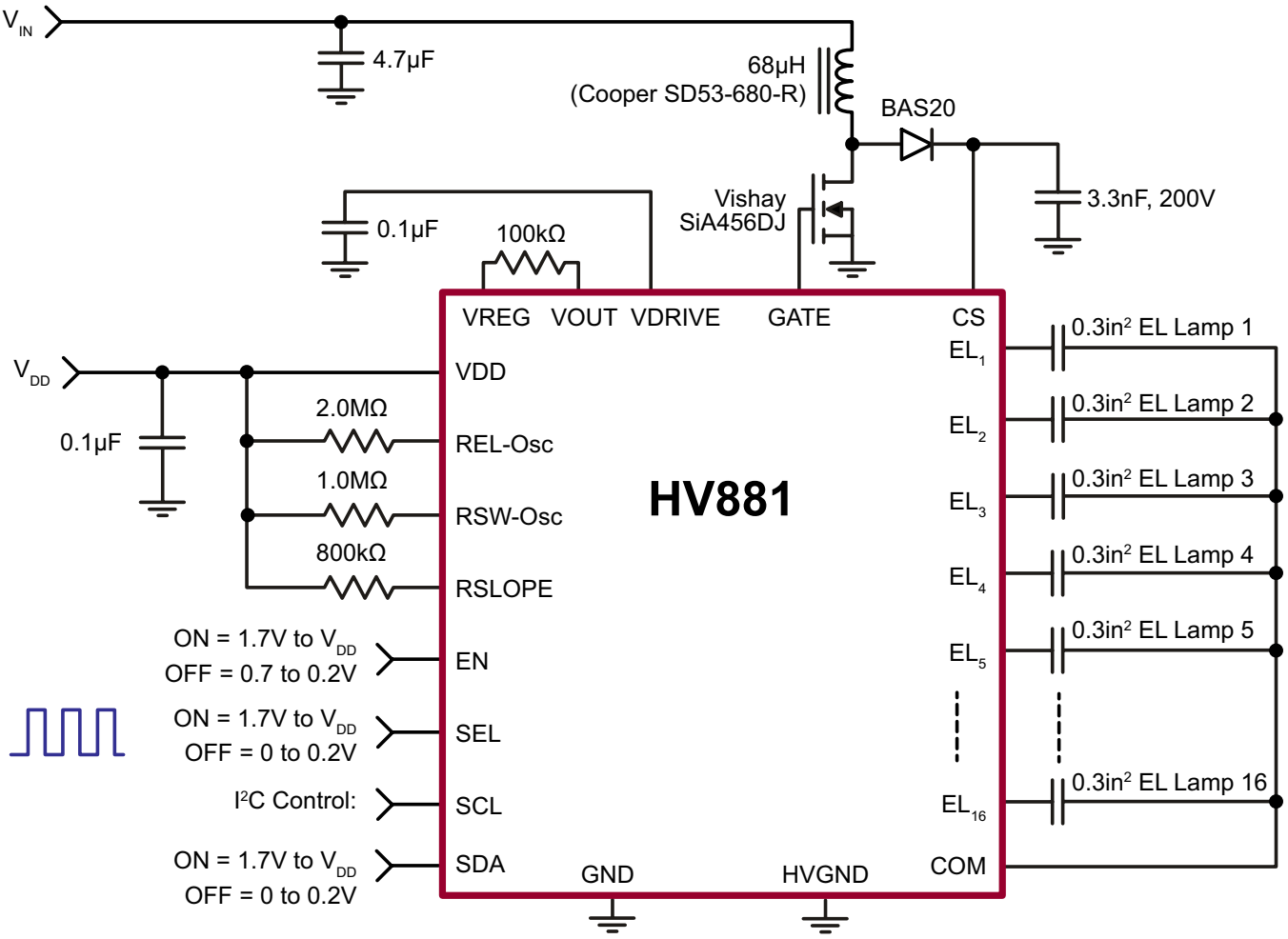
Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	1.8	-	5.5	V	---
f_{SW}	Switching frequency	50	-	200	kHz	---
f_{EL}	EL output frequency	200	-	1000	Hz	---
S_{EL}	Input for EL output frequency	1600	-	8000	Hz	S_{EL} = 8 x (f_{EL}) and 50% duty cycle
C_{LOAD}	Lamp capacitance per EL output	0	-	1.0	nF	---
C_{COM}	COM lamp capacitance	0	-	16	nF	---
T_j	Operating temperature	-40	-	+85	°C	---

Electrical Characteristics

(Over recommended operating conditions unless otherwise specified T_J = 25°C)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
V_{CS}	Output regulation voltage	145	170	195	V	V_{DD} = 1.8 to 5.5V
V_{LAMP}	Differential output voltage	290	340	390	V	V_{DD} = 1.8 to 5.5V
I_{DDQ}	Quiescent V_{DD} supply current	-	-	1000	nA	V_{DD} = 5.5V
I_{DD}	Input current going into the V_{DD} pin	-	-	350	µA	V_{DD} = 5.5V, R_{EL} = 2.0MΩ R_{SW} =1.0MΩ, R_{SL} = 800kΩ
I_{IN}	Input current including inductor current	-	-	110	mA	See Typical Application Circuit, V_{IN} = 4.2V
V_{REG}	External input voltage range	0	-	0.44	V	V_{DD} = 1.8 to 5.5V
f_{EL}	EL Lamp frequency	-	200	-	Hz	R_{EL} =2.0MΩ
f_{SW}	Switching transistor frequency	-	90	-	kHz	R_{SW} =1.0MΩ
D	External MOSFET duty cycle	-	-	88	%	---
V_{IH}	SEL, EN, SDA, SCL logic pins input high level	1.7	-	V_{DD}	V	V_{DD} = 1.8 to 5.5V
V_{IL}	SEL, EN, SDA, SCL logic pins input low level	0	-	0.2	V	V_{DD} = 1.8 to 5.5V
I_{Logic}	EN, SDA, SCL pins input current	-1.0	-	1.0	µA	V_{DD} = 1.8 to 5.5V
$I_{Logic-SEL}$	SEL logic pin input current	-1.0	-	12.0	µA	V_{DD} = 1.8 to 5.5V
V_{GATE}	External MOSFET gate voltage	-	8.0	-	V	V_{DD} = 1.8 to 5.5V
$t_{GATE-RISE}$	External MOSFET gate voltage rise time	-	100	-	ns	V_{DD} = 1.8 to 5.5V, C_L = 330pF
$t_{GATE-FALL}$	External MOSFET gate voltage fall time	-	-	20	ns	V_{DD} = 1.8 to 5.5V, C_L = 330pF
t_f	EL1 - EL16 outputs fall time for ½ EL cycle	-	190	-	µs	R_{SL} = 800kΩ, V_{DD} = 3.0V, V_{CS} =170V
f_{CLK}	SCL speed	-	-	500	kHz	---
t_{SU}	Setup time before clock falls	300	-	-	ns	---
t_H	Hold time after clock falls	850	-	-	ns	---

Typical Application Circuit

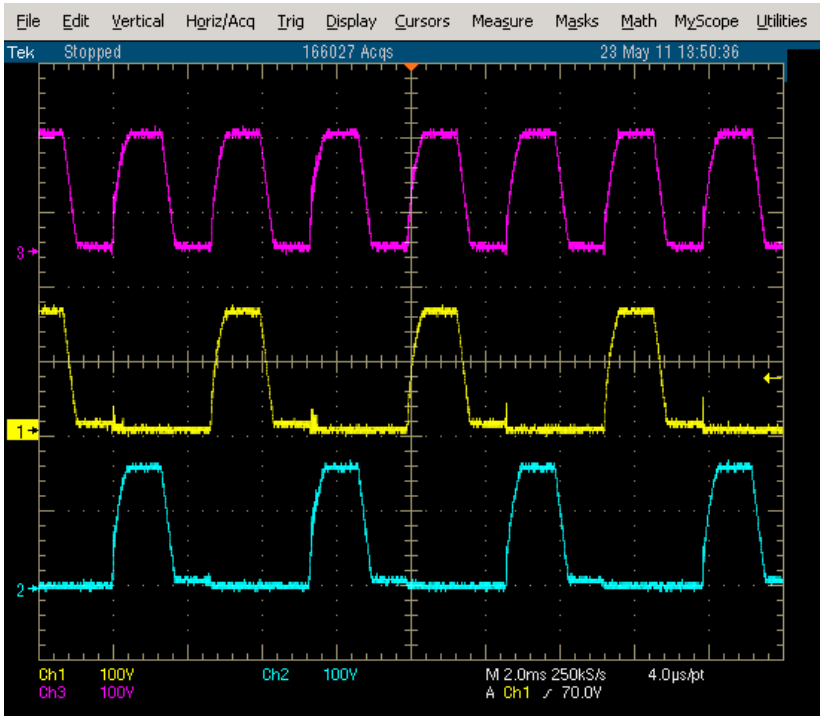


Note:
The L_x MOSFET may be changed depending on output load and required output power.

Test Data

V_{DD} (V)	Lamp Size	V_{IN} (V)	I_{IN} (mA)	V_{CS} (V)	f_{EL} (Hz)	Lamp Brightness (cd/m²)
3.0	0.3in² lamp on each of the EL1 - EL16 outputs	3.2	72.1	160	190	33
		3.7	62.3	160	190	35
		4.2	52.3	160	190	36

Typical Output Waveform



EL Lamp Brightness Control using I²C

No of bits	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit
-	start bit	slave addr	$\overline{W}$ bit	Ack	byte 0	Ack	byte 1	Ack	byte 2	Ack	byte 3	Ack	byte 4	Ack	byte 5	Ack	byte 6	Ack	byte 7	Ack	stop bit

The I²C format for the SDA input is shown below:

Note:

The I²C is write-only. So the W bit has to always be logic low. (A "0" indicates a transmission write).

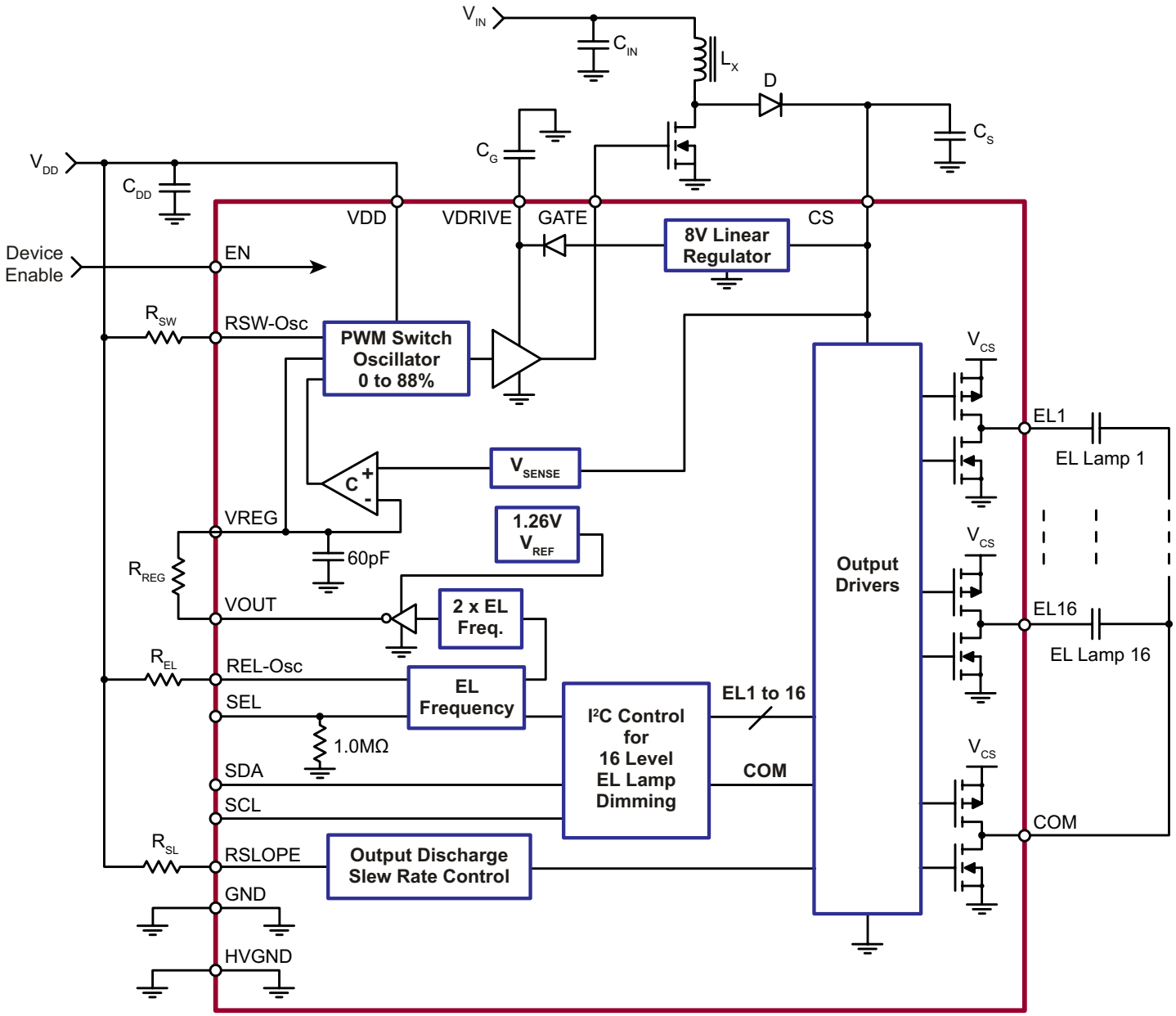
7-bit slave address: 000 0110 (0x06 in hex)

Each of the EL lamp's brightness controls is a 4-bit binary number which is provided by the serial data input (SDA).

Byte 0 controls both the 16 level brightness of EL_lamp1 (bit0 - bit3) and EL_lamp2 (bit4 - bit7) and similarly, other bytes control the brightness of other pairs of lamp.

1. If all the 4 bits for a designated EL lamp are L, the differential voltage across the lamp is zero.
2. If any of the 4 bits for a designated EL lamp is H:
   a. The 4-bit value sets the average number of cycles for which the EL lamp voltage is non-zero.
   b. The EL lamp brightness is linearly proportional to the binary lamp control code.

Block Diagram

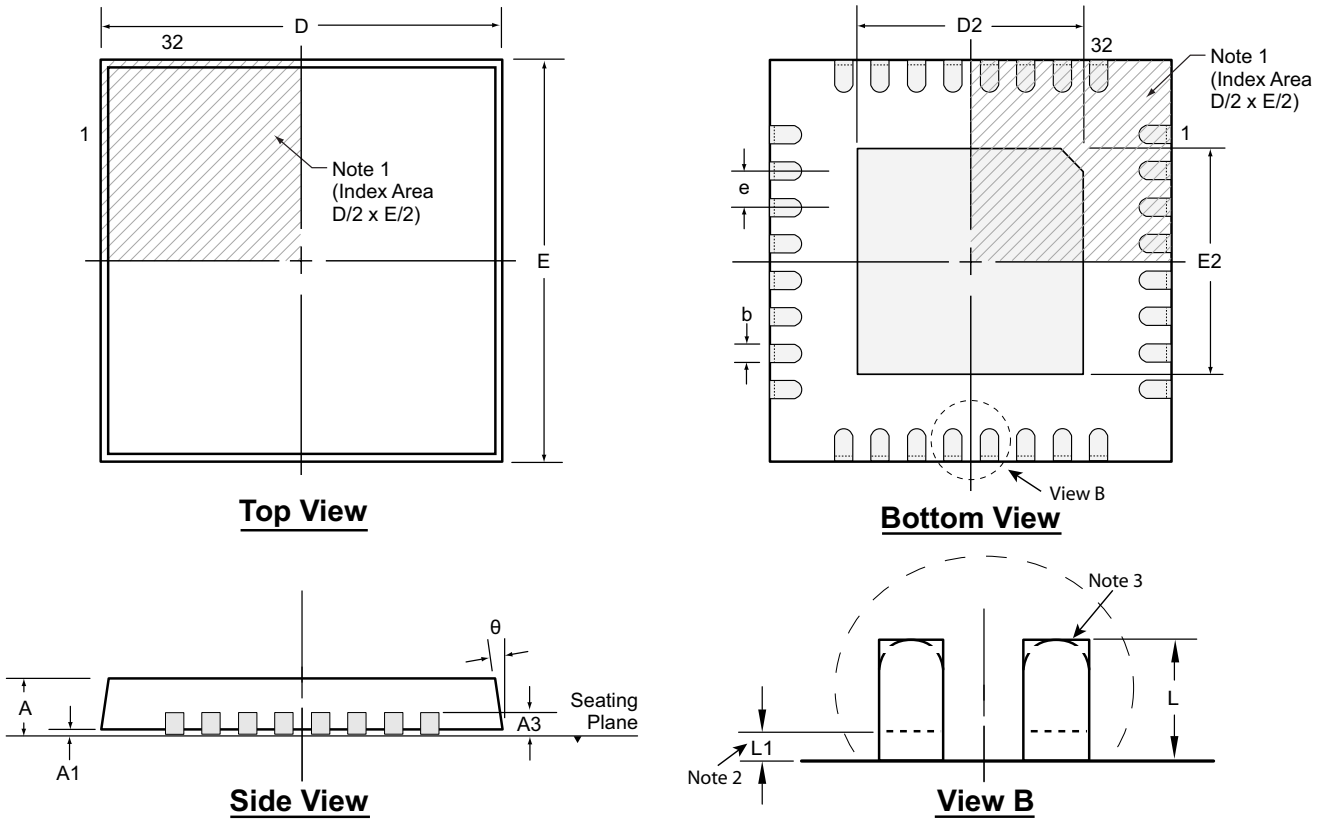


Pin Configuration and External Component Description

Pin #	Pin Name	Description
1	REL-Osc	The external resistor from REL-Osc to VDD sets the EL frequency. The EL frequency is inversely proportional to the external R_{EL} resistor value. Reducing the resistor value by a factor of two will result in increasing the EL frequency by two.
2	RSLOPE	The external resistor, R_{SL}, from RSLOPE to VDD, controls the EL1 - EL16 outputs discharge time. The equation for the EL1 - EL16 outputs typical fall time is: $t_{f(typ)} = V_{CS} / ((V_{DD} - 0.85) / (R_{SL} \bullet 3pF))\mu s$.
3	RSW-Osc	The external resistor from RSW-Osc to VDD sets the switch converter frequency. The switch converter frequency is inversely proportional to the R_{SW} resistor value. Reducing the resistor value by a factor of two will result in increasing the switch converter frequency by two.
4	VREG	The input voltage to set the V_{CS} regulation voltage. This pin allows an external voltage source to control the V_{CS} amplitude in the range from 0 to 195V. The output voltage is (403 ± 10%) • V_{REG}. The V_{REG} voltage can also be set by using an external resistor between VREG and VOUT pins. The output charging rate is inversely proportional to the resistor value.
5	VOUT	Switched and voltage divided to one-third the internal reference voltage. An external resistor between VREG and VOUT pins controls the V_{CS} charging rate. If this pin is not used, then it should be left floating.
6	VDD	The low voltage input supply pin.
7	GND	Device ground.
8	EN	1.7V logic input pin to turn the device ON/OFF. A logic high turns ON the device and a logic LOW turns the device OFF.
9 – 16	EL16 - EL9	EL lamp 16, EL lamp 15 …. EL lamp 9 connections.
17	COM	The common connection for all the 16 EL lamps.
18 – 25	EL8 - EL1	EL lamp 8, EL lamp 7 …. EL lamp 1 connections.
26	HVGND	High voltage ground. It should be connected to device ground.
27	CS	Connect a 0.001µF to 0.01µF 200V capacitor between this pin and ground. This capacitor stores the energy transferred from the inductor.
28	SCL	The I^2C logic serial clock input pin.
29	SDA	The I^2C logic serial data input pin.
30	GATE	The gate control pin for the switching MOSFET. The connection for an external MOSFET. In general, low R_{ON} MOSFET's, which can handle more current, are more suitable to drive larger size lamps. Also a small value inductor should be used. But as the R_{ON} value and the inductor value decrease, the switching frequency of the inductor (controlled by R_{SW}) should be increased to avoid inductor saturation. The external MOSFET threshold voltage minimum value should be equal to V_{DD} or lower.
31	VDRIVE	Drive voltage for the MOSFET gate voltage. An external bypass capacitor (C_G) is required to ground.
32	SEL	The external logic signal input pin to set the EL frequency. If this pin is used, the REL-Osc pin should be connected to ground. The frequency input at this pin should be at 50% duty cycle and at eight times the desired EL output frequency. If this pin is not used then it should be left floating. This pin has an internal pull-down resistor of 1.0MΩ ± 50%.
Center Pad		Center heat slug, externally connected to Ground.

32-Lead QFN Package Outline (K7)

5.00x5.00mm body, 0.80mm height (max), 0.50mm pitch



Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	4.85*	1.05	4.85*	1.05	0.50 BSC	0.30†	0.00	0°
	NOM	0.75	0.02		0.25	5.00	-	5.00	-		0.40†	-	-
	MAX	0.80	0.05		0.30	5.15*	3.55†	5.15*	3.55†		0.50†	0.15	14°

JEDEC Registration MO-220, Variation WHHD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc. #: *DSPD-32QFNK75X5P050, Version A052311.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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