

**Features**

- fully assembled and tested
- on-board mode selection switch
- on-board PLL Lock and Loss of Signal LED indicators
- SMA connectors for all high-speed data inputs and outputs

**General Description**

The XBN2004 Rev 7 evaluation board is designed to simplify and speed-up the evaluation process of Gennum's GN2004, GN2004S and GN2014 devices.

This document describes the application of the XBN2004 Rev 7 Evaluation Board for the GN2004S SONET XFP Tx Signal Conditioner.

The block diagram of the XBN2004 Rev 7 evaluation board is shown on [page 2](#).

An input signal is applied to the board through the Equalizer Input (EQIn) SMA connectors using 50Ω coaxial cables .

The on-board GN2004S chip performs conditioning of the received signal.

The conditioned signal is available on the Serial Data Output (SDO) SMA connectors and, when required, on the Loop Back Serial Data Output (LBSDO) SMA connectors.

The LBSDO output can be used for interconnect troubleshooting purposes.

Two LEDs indicate the status of the GN2004S device.

- The PLL Lock green LED (D1), when lit, indicates that the PLL is locked.
- The LOS red LED (D2), when lit, indicates that the equalizer input signal level is below application set threshold level.

The schematic diagram of the XBN2004 Rev 7 evaluation board is shown in [Figure 2-1](#).

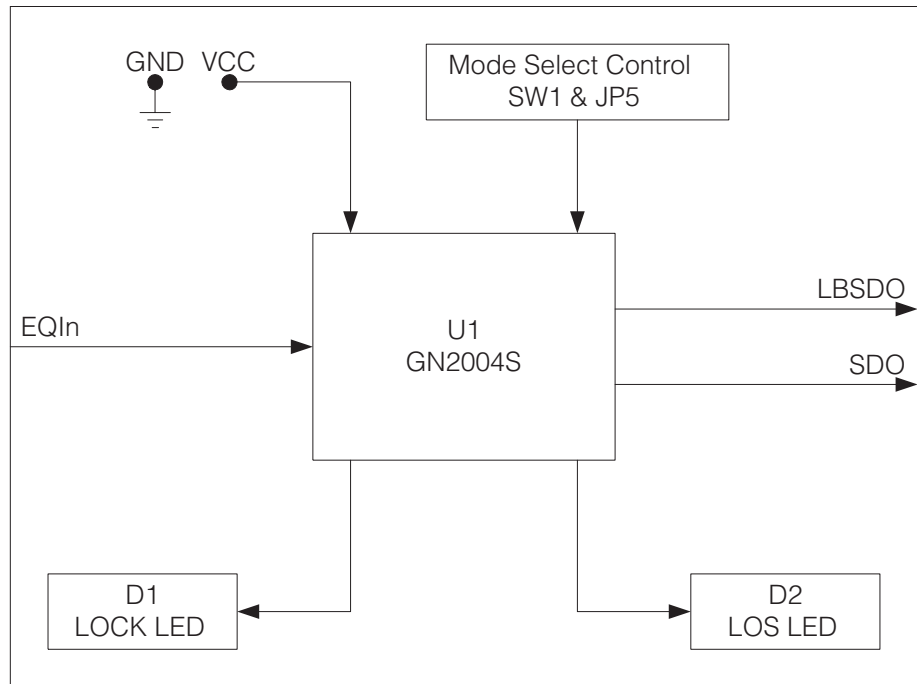
The PCB layout information is shown in [Figure 2-2](#), [Figure 2-3](#), and [Figure 2-4](#).

The XBN2004 Rev 7 printed circuit board is a four-layer, .062" board.

Top layer uses RT Duriod 6002, low dielectric loss material.

All other layers are standard FR-4 material.

All high-speed data traces between SMA connectors and the GN2004S device are 100Ω differential microstrip lines on the top layer.



**XBN2004 Rev 7 Evaluation Board Block Diagram**

**Contents**

Features ..... 1

General Description ..... 1

1. Quick Start Sequence ..... 3

2. Evaluation Board Schematic and PCB Layout ..... 4

3. GN2004S Evaluation Board Mode Settings ..... 8

    3.1 Mission Mode ..... 8

    3.2 Loop Back Mode ..... 9

    3.3 Trace Equalization with Retiming Bypass Mode ..... 10

4. Revision History ..... 11

# 1. Quick Start Sequence

1. Configure the evaluation board in accordance to the desired mode (see [Figure 3-1](#), [Figure 3-2](#), and [Figure 3-3](#)).
2. Connect the power supply ground to the on-board "GND" connector.
3. Connect a +3.3V power supply to the on-board "VCC" connector (current limit on the power supply should be set to 120mA).
4. Using 50 $\Omega$  coaxial cables, apply an input amplitude between 120mVppd and 1000mVppd to the EQIn SMA connectors.
5. Use the SDO SMA connectors to monitor the GN2004S output. The SDO output can also be connected to a bit error detector for bit error rate measurements.
6. Connect high-speed oscilloscope to the LBSDO SMA connectors to monitor the GN2004S LBSDO output.
7. Observe the LOCK and LOS LEDs.



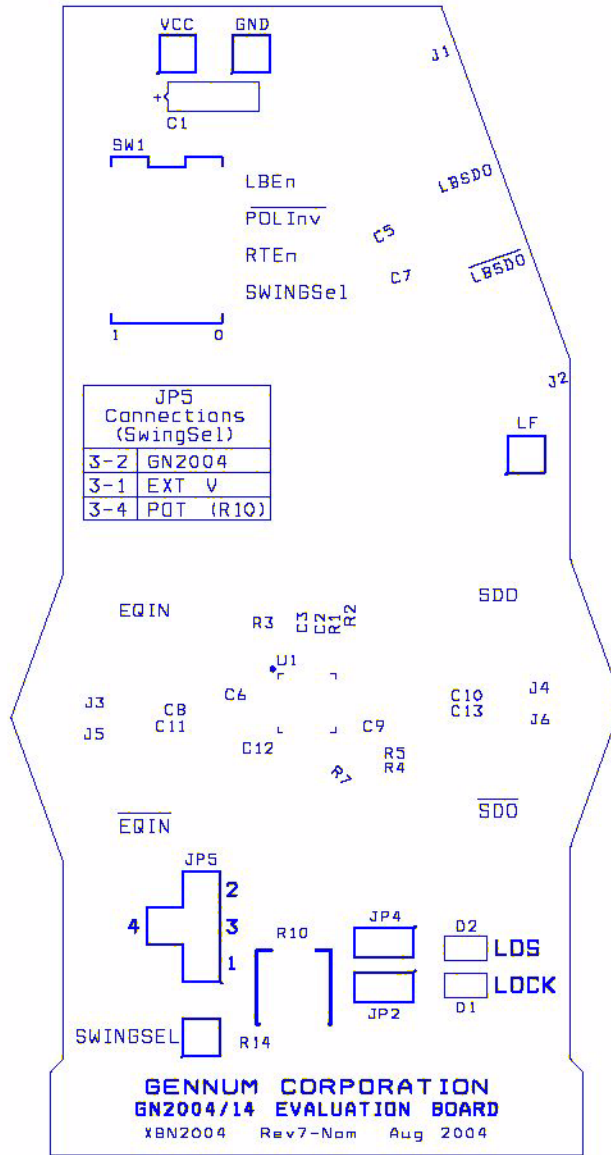


Figure 2-2: XBN2004 PCB Layout - Top Silk

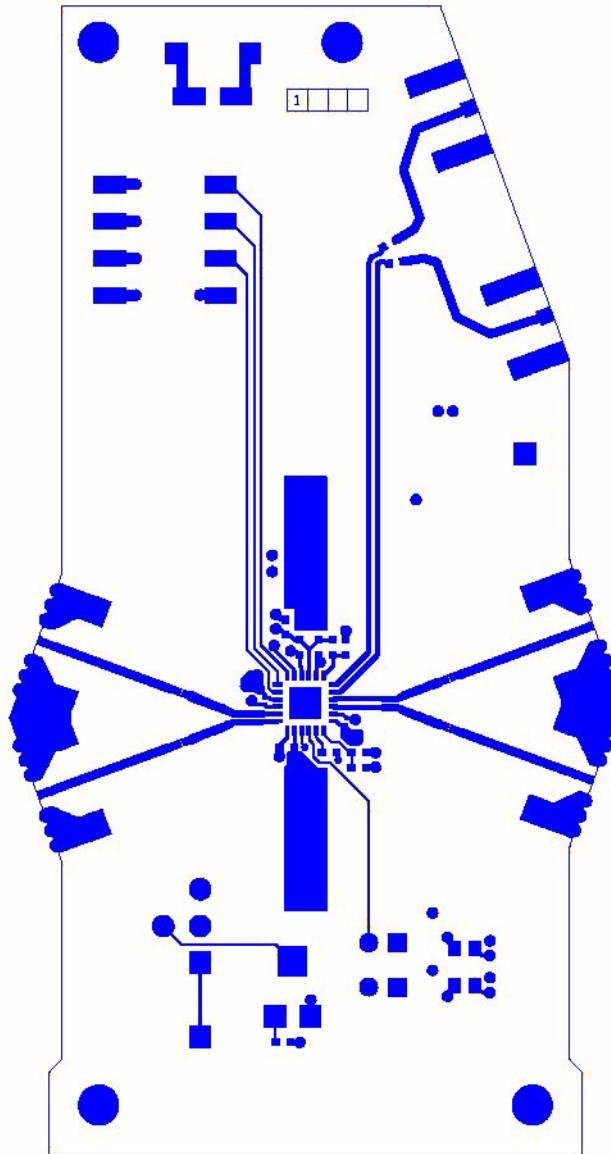


Figure 2-3: XBN2004 PCB Layout - Top Comp.

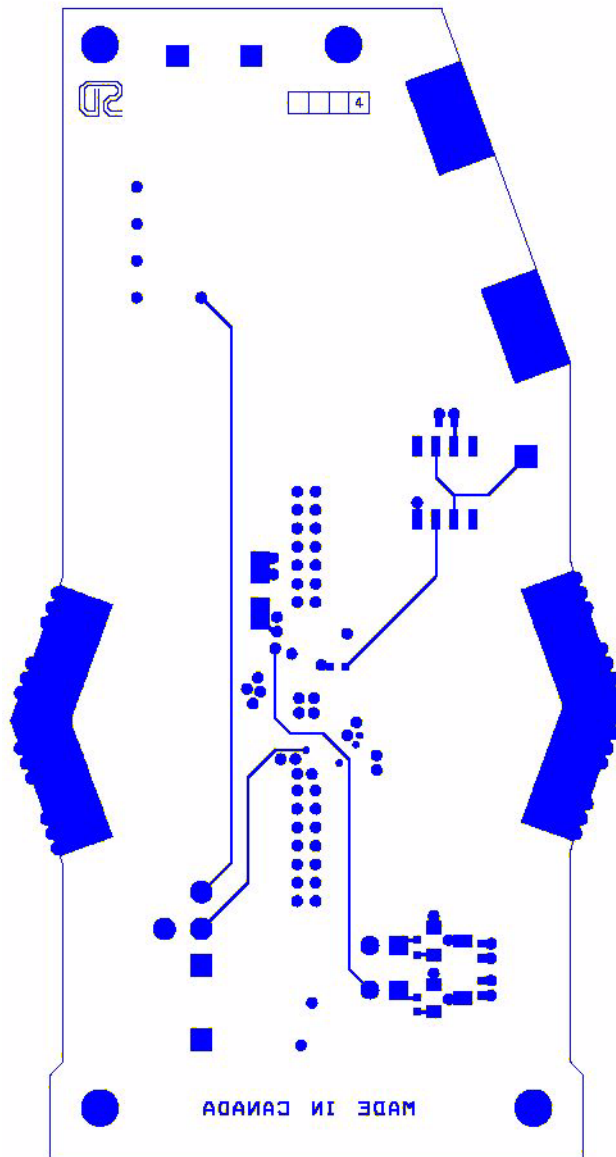


Figure 2-4: XBN2004 PCB Layout - Bottom Components

### 3. GN2004S Evaluation Board Mode Settings

The GN2004S SONET XFP Tx Signal Conditioner is designed such that it can operate in various modes.

This section of the document describes the SW1 switch and JP5 jumper settings for some of the available modes.

For more information on the GN2004S operational modes please refer to the GN2004S Data Sheet.

#### 3.1 Mission Mode

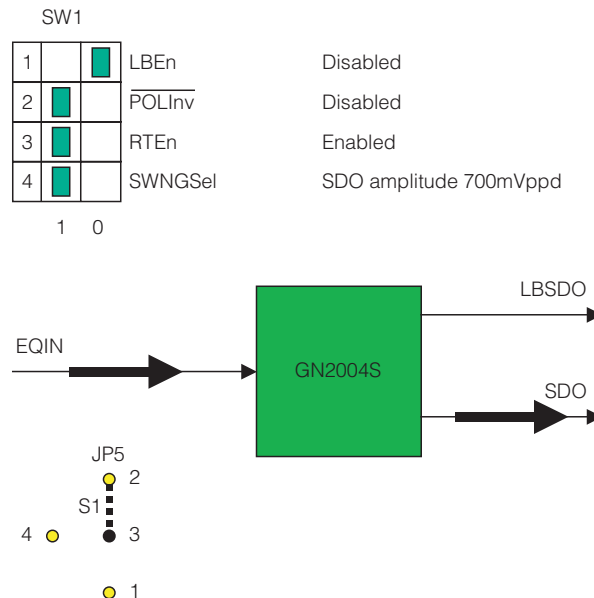
In this mode 9.95Gb/s - 11.3Gb/s data from EQIn input is first equalized and then retimed.

The retimed data is available on the SDO output only.

The setting shown in [Figure 3-1](#) configures the GN2004S device to operate in this mode and also sets the device to:

- Normal (not inverted) polarity on the SDO output (EQINP → SDOP and EQINN → SDON)
- The SDO output amplitude of 700mVppd

This mode can be used to evaluate the GN2004S device performance in Mission Mode (Equalizer plus CDR).



**Figure 3-1: Settings for Mission Mode**



### 3.2 Loop Back Mode

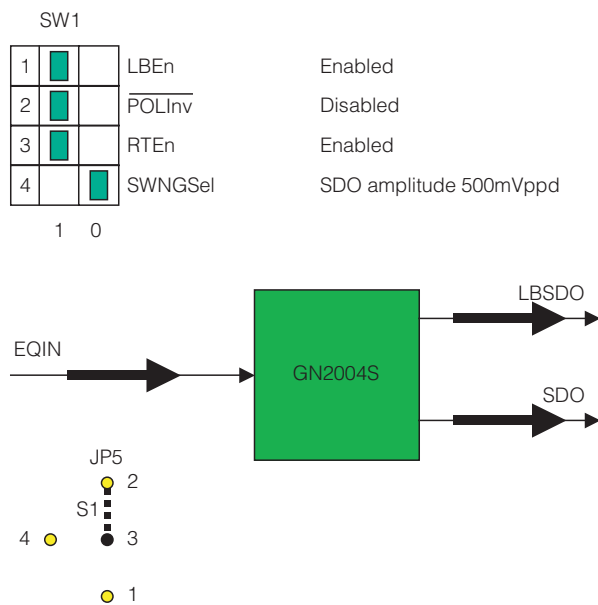
Figure 3-2 shows the setting for Loop Back mode.

In this mode the data from the EQIn input is equalized and retimed.

The retimed data is available on the SDO and LBSDO outputs simultaneously.

This setting also sets the device to:

- Normal (not inverted) polarity on the SDO and the LBSDO outputs. (EQINP → SDOP and EQINN → SDON)
- The SDO output amplitude of 500mVppd.
- The LBSDO output amplitude of 200mVppd typical.



**Figure 3-2: Settings for Loop Back Mode**

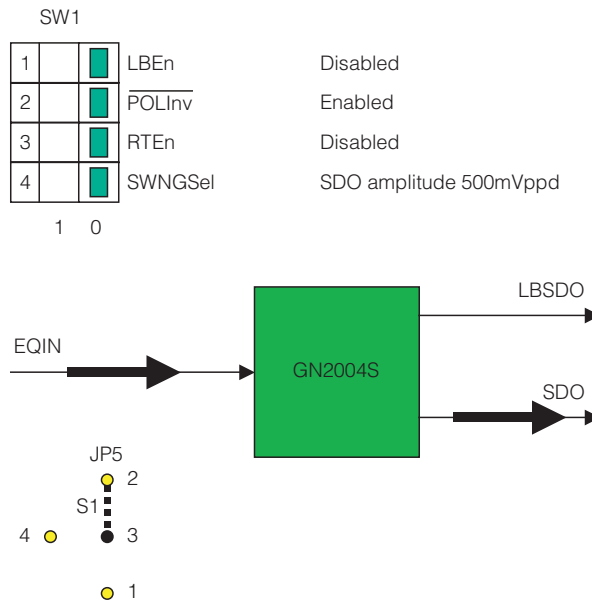
### 3.3 Trace Equalization with Retiming Bypass Mode

Figure 3-3 shows the setting for Retiming Bypass mode.

In this mode the data from the EQIn input is just equalized, bypassing internal CDR. The equalized data is available on the SDO output only. This setting also sets the device to:

- Inverted polarity on the SDO output (EQINN → SDOP and EQINP → SDON)
- The SDO output amplitude of 500mVppd.

This mode can be used to evaluate the GN2004S equalizer performance. The information can be used to analyze the CDR's jitter tolerance after equalization.



**Figure 3-3: Settings for CDR Bypass Mode**

## 4. Revision History

Version	ECR	Date	Changes and / or Modifications
0	137098	June 2005	New document.

### CAUTION

ELECTROSTATIC SENSITIVE DEVICES  
DO NOT OPEN PACKAGES OR HANDLE  
EXCEPT AT A STATIC-FREE WORKSTATION



### DOCUMENT IDENTIFICATION

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