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About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

The MB90350-series with 1 channel FULL-CAN interface and Flash ROM is especially designed for automotive and industrial applications. Its main feature is the on-board CAN interface, which conforms to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal full CAN approach. With the new 0.35 μm CMOS technology, Cypress now offers on-chip Flash-ROM program memory up to 128 Kbytes.

The power supply (3 V) is supplied to the internal MCU core from an internal regulator circuit. This creates a major advantage in terms of EMI and power consumption.

The internal PLL clock frequency multiplier provides an internal 42 ns instruction execution time from an external 4 MHz clock. Also, the clock monitor function can monitor main clock and sub clock independently.

As the peripheral resources, the unit features a 4-channel Output Compare Unit, 6-channel Input Capture Unit, 2 separate 16-bit freerun timers, 2-channel UART and 15-channel 8/10-bit A/D converter.

Features

Clock

- Built-in PLL clock frequency multiplication circuit
- Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 6 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 24 MHz).
- Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed. (devices without S-suffix only)
- Minimum execution time of instruction : 42 ns (when operating with 4-MHz oscillation clock, and 6-time multiplied PLL clock).
- Built-in clock modulation circuit

16 Mbytes CPU memory space

- 24-bit internal addressing

Clock monitor function (MB90x356x and MB90x357x only)

- Main clock or sub clock is monitored independently.
- Internal CR oscillation clock (100 kHz typical) can be used as sub clock.

Instruction system best suited to controller

- Wide choice of data types (bit, byte, word, and long word)
- Wide choice of addressing modes (23 types)
- Enhanced multiply-divide instructions with sign and RETI instructions
- Enhanced high-precision computing with 32-bit accumulator

Instruction system compatible with high-level language (C language) and multitask

- Employing system stack pointer
- Enhanced various pointer indirect instructions
- Barrel shift instructions

Increased processing speed

- 4-byte instruction queue

Powerful interrupt function

- Powerful 8-level, 34-condition interrupt feature
- Up to 8 channels external interrupts are supported.

Automatic data transfer function independent of CPU

- Extended intelligent I/O service function (EI²OS) : up to 16 channels
- DMA: up to 16 channels

Low power consumption (standby) mode

- Sleep mode (a mode that halts CPU operating clock)
- Main timer mode (a timebase timer mode switched from the main clock mode)
- PLL timer mode (a timebase timer mode switched from the PLL clock mode)
- Watch mode (a mode that operates sub clock and watch timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU intermittent operation mode

Process

- CMOS technology

I/O port

- General-purpose input/output port (CMOS output)
 - 49 ports (devices without S-suffix : devices that correspond to sub clock)
 - 51 ports (devices with S-suffix : devices that do not correspond to sub clock)

Sub clock pin (X0A, X1A)

- Yes (using the external oscillation) : devices without S-suffix
- No (using the sub clock mode at internal CR oscillation) : devices with S-suffix

Timer

- Timebase timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit × 10 channels or 16-bit × 6 channels
- 16-bit reload timer: 4 channels
- 16-bit input/output timer
 - 16-bit freerun timer : 2 channels (FRT0: ICU0/1, FRT1: ICU 4/5/6/7, OCU 4/5/6/7)
 - 16-bit input capture: (ICU): 6 channels
 - 16-bit output compare: (OCU): 4 channels

FULL-CAN interface 1 channel

- Compliant with Ver2.0 part A and Ver2.0 part B CAN specifications
- Flexible message buffering (mailbox and FIFO buffering can be mixed)
- CAN wake-up function

UART (LIN/SCI): 2 channels

- Equipped with full-duplex double buffer
- Clock-asynchronous or clock-synchronous serial transmission is available.

I²C interface: 1 channel

- Up to 400 Kbit/s transfer rate

DTP/External interrupt: 8 channels, CAN wakeup: 1 channel

- Module for activation of extended intelligent I/O service (E²OS), DMA, and generation of external interrupt by external input.

Delay interrupt generator module

- Generates interrupt request for task switching.

8/10-bit A/D converter: 15 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 3 μs (at 24-MHz machine clock, including sampling time)

Program patch function

- Address matching detection for 6 address pointers.

Capable of changing input voltage level for port

- Automotive/CMOS-Schmitt (initial level is Automotive in single chip mode)
- TTL level (corresponds to external bus pins only, initial level of these pins is TTL in external bus mode)

Low voltage/CPU operation detection reset (devices with T-suffix)

- Detects low voltage (4.0 V ± 0.3 V) and resets automatically
- Resets automatically when program is runaway and counter is not cleared within interval time (approx. 262 ms : external 4 MHz)

Dual operation flash memory (only flash memory devices with A-suffix)

- Erase/write and read can be executed in the different bank (Upper Bank/Lower Bank) at the same time.

Models that support + 125 °C

- Devices without A-suffix (excluding evaluation device)
: The maximum operating frequency is 16 MHz (at T_A = +125 °C) .
- Devices with A-suffix (excluding evaluation device)
: The maximum operating frequency is 24 MHz (at T_A = +125 °C) .

Flash security function

- Protects the content of Flash memory (MB90F352x and MB90F357x only)

External bus interface

- 4 Mbytes external memory space

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1. Product Lineup 1

Part Number Parameter	MB90F351, MB90F352	MB90F351S, MB90F352S	MB90F351A, MB90F352A	MB90F351TA, MB90F352TA	MB90F351AS, MB90F352AS	MB90F351TAS, MB90F352TAS
CPU	F ² MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	Flash memory 64Kbytes :MB90F351(S) 128Kbytes :MB90F352(S)		Dual operation flash memory 64Kbytes :MB90F351A(S), MB90F351TA(S) 128Kbytes :MB90F352A(S), MB90F352TA(S)			
RAM	4 Kbytes					
Emulator-specific power supply*	—					
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes	No	Yes		No	
Clock monitor function	No					
Low voltage/CPU operation detection reset	No		No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter/Flash programming 4.5 V to 5.5 V : at using external bus					
Operating temperature range	−40 °C to +105 °C (+125 °C up to 16 MHz machine clock)		−40 °C to +125 °C			
Package	LQFP-64					
UART	2 channels					
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
	1 channel					
A/D Converter	15 channels					
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.					
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$, $f_{sys}/2^5$, $f_{sys}/2^6$, $f_{sys}/2^7$ (f_{sys} = Machine clock frequency)					
16-bit Output Compare	4 channels					
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit Input Capture	6 channels					
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					

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Part Number Parameter	MB90F351, MB90F352	MB90F351S, MB90F352S	MB90F351A, MB90F352A	MB90F351TA, MB90F352TA	MB90F351AS, MB90F352AS	MB90F351TAS, MB90F352TAS
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12 Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = Machine clock frequency, f_{osc} = Oscillation clock frequency)					
CAN Interface	1 channel Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External Interrupt	8 channels Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI ² OS) and DMA.					
D/A converter	—					
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash Memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F352x only)					
Corresponding EVA name	MB90V340A-102	MB90V340A-101	MB90V340A-102		MB90V340A-101	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
 Please refer to the Emulator hardware manual about details.

2. Product Lineup 2

Part Number	MB90351A, MB90352A	MB90351TA, MB90352TA	MB90351AS, MB90352AS	MB90351TAS, MB90352TAS	MB90V340A- 101	MB90V340A- 102
CPU	F ² MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64Kbytes :MB90351A(S), MB90351TA(S) 128Kbytes :MB90352A(S), MB90352TA(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A) (Max 100 kHz)	Yes		No		No	Yes
Clock monitor function	No					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	−40 °C to +125 °C				—	
Package	LQFP-64				PGA-299	
UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I ² C (400 Kbps)	1 channel				2 channels	
A/D Converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				I/O Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. I/O Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$, $f_{sys}/2^5$, $f_{sys}/2^6$, $f_{sys}/2^7$ (f_{sys} = Machine clock frequency)					
16-bit Output Compare	4 channels				8 channels	
	Signals an interrupt when 16-bit I/O Timer matches output compare registers. A pair of compare registers can be used to generate an output signal.					
16-bit Input Capture	6 channels				8 channels	
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					

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Part Number Parameter	MB90351A, MB90352A	MB90351TA, MB90352TA	MB90351AS, MB90352AS	MB90351TAS, MB90352TAS	MB90V340A- 101	MB90V340A- 102
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12				8 channels (16-bit)/ 16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = Machine clock frequency, f_{osc} = Oscillation clock frequency)					
CAN Interface	1 channel				3 channels	
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External Interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI ² OS) and DMA.					
D/A converter	—				2 channels	
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash Memory	—					
Corresponding EVA name	MB90V340A-102		MB90V340A-101		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

3. Product Lineup 3

Part Number Parameter	MB90F356A, MB90F357A	MB90F356TA, MB90F357TA	MB90F356AS, MB90F357AS	MB90F356TAS, MB90F357TAS
CPU	F ² MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)			
ROM	Dual operation flash memory 64Kbytes :MB90F356A(S), MB90F356TA(S) 128Kbytes :MB90F357A(S), MB90F357TA(S)			
RAM	4 Kbytes			
Emulator-specific power supply*	—			
Sub clock pin (X0A, X1A)	Yes		No (internal CR oscillation can be used as sub clock)	
Clock monitor function	Yes			
Low voltage/CPU operation detection reset	No	Yes	No	Yes
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 3.5 V to 5.5 V : at using A/D converter/Flash programming 3.5 V to 5.5 V : at using external bus			
Operating temperature range	−40 °C to +125 °C			
Package	LQFP-64			
UART	2 channels			
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I ² C (400 Kbps)	1 channel			
A/D Converter	15 channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)			
16-bit Reload Timer (4 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = Machine clock frequency) Supports External Event Count function.			
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.			
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$, $f_{sys}/2^5$, $f_{sys}/2^6$, $f_{sys}/2^7$ (f_{sys} = Machine clock frequency)			
16-bit Output Compare	4 channels			
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.			
16-bit Input Capture	6 channels			
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.			

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Part Number Parameter	MB90F356A, MB90F357A	MB90F356TA, MB90F357TA	MB90F356AS, MB90F357AS	MB90F356TAS, MB90F357TAS
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12 Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = Machine clock frequency, f_{osc} = Oscillation clock frequency)			
CAN Interface	1 channel Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.			
External Interrupt	8 channels Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI ² OS) and DMA.			
D/A converter	—			
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)			
Flash Memory	Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Number of erase cycles : 10,000 times Data retention time : 10 years Boot block configuration Erase can be performed on each block. Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash (MB90F357x only)			
Corresponding EVA name	MB90V340A-104		MB90V340A-103	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
 Please refer to the Emulator hardware manual about details.

4. Product Lineup 4

Part Number Parameter	MB90356A, MB90357A	MB90356TA, MB90357TA	MB90356AS, MB90357AS	MB90356TAS, MB90357TAS	MB90V340A- 103	MB90V340A- 104
CPU	F ² MC-16LX CPU					
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, 1/2 when PLL stops) Minimum instruction execution time : 42 ns (oscillation clock 4 MHz, PLL × 6)					
ROM	MASK ROM 64Kbytes :MB90356A(S), MB90356TA(S) 128Kbytes :MB90357A(S), MB90357TA(S)				External	
RAM	4 Kbytes				30 Kbytes	
Emulator-specific power supply*	—				Yes	
Sub clock pin (X0A, X1A)	Yes	No (internal CR oscillation can be used as sub clock)			No (internal CR oscillation can be used as sub clock)	Yes
Clock monitor function	Yes					
Low voltage/CPU operation detection reset	No	Yes	No	Yes	No	
Operating voltage range	3.5 V to 5.5 V : at normal operating (not using A/D converter) 4.0 V to 5.5 V : at using A/D converter 4.5 V to 5.5 V : at using external bus				5 V ± 10%	
Operating temperature range	-40 °C to +125 °C				—	
Package	LQFP-64				PGA-299	
UART	2 channels				5 channels	
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device					
I ² C (400 Kbps)	1 channel				2 channels	
A/D Converter	15 channels				24 channels	
	10-bit or 8-bit resolution Conversion time : Min 3 μs includes sample time (per one channel)					
16-bit Reload Timer (4 channels)	Operation clock frequency : $f_{sys}/2^1$, $f_{sys}/2^3$, $f_{sys}/2^5$ (f_{sys} = Machine clock frequency) Supports External Event Count function.					
16-bit I/O Timer (2 channels)	I/O Timer 0 (clock input FRCK0) corresponds to ICU 0/1. I/O Timer 1 (clock input FRCK1) corresponds to ICU 4/5/6/7, OCU 4/5/6/7.				I/O Timer 0 corresponds to ICU 0/1/2/3, OCU 0/1/2/3. I/O Timer 1 corresponds to ICU 4/5/6/7, OCU 4/5/6/7.	
	Signals an interrupt when overflowing. Supports Timer Clear when a match with Output Compare (Channel 0, 4) . Operation clock frequency : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$, $f_{sys}/2^5$, $f_{sys}/2^6$, $f_{sys}/2^7$ (f_{sys} = Machine clock frequency)					
16-bit Output Compare	4 channels				8 channels	
	Signals an interrupt when 16-bit I/O Timer matches with output compare registers. A pair of compare registers can be used to generate an output signal.					

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Part Number Parameter	MB90356A, MB90357A	MB90356TA, MB90357TA	MB90356AS, MB90357AS	MB90356TAS, MB90357TAS	MB90V340A- 103	MB90V340A- 104
16-bit Input Capture	6 channels				8 channels	
	Retains freerun timer value by (rising edge, falling edge or rising & falling edge), signals an interrupt.					
8/16-bit Programmable Pulse Generator	6 channels (16-bit)/10 channels (8-bit) 8-bit reload counters × 12 8-bit reload registers for L pulse width × 12 8-bit reload registers for H pulse width × 12				8 channels (16-bit)/16 channels (8-bit) 8-bit reload counters × 16 8-bit reload registers for L pulse width × 16 8-bit reload registers for H pulse width × 16	
	Supports 8-bit and 16-bit operation modes. A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler + 8-bit reload counter. Operation clock frequency : f_{sys} , $f_{sys}/2^1$, $f_{sys}/2^2$, $f_{sys}/2^3$, $f_{sys}/2^4$ or $128 \mu s @ f_{osc} = 4 \text{ MHz}$ (f_{sys} = Machine clock frequency, f_{osc} = Oscillation clock frequency)					
CAN Interface	1 channel				3 channels	
	Conforms to CAN Specification Version 2.0 Part A and B. Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID Supports multiple messages. Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps.					
External Interrupt	8 channels				16 channels	
	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, extended intelligent I/O services (EI ² OS) and DMA.					
D/A converter	—				2 channels	
I/O Ports	Virtually all external pins can be used as general purpose I/O port. All push-pull outputs Bit-wise settable as input/output or peripheral module signal Settable as CMOS schmitt trigger/ automotive inputs TTL input level settable for external bus (only for external bus pin)					
Flash Memory	—					
Corresponding EVA name	MB90V340A-104		MB90V340A-103		—	

* : It is setting of Jumper switch (TOOL VCC) when Emulator (MB2147-01) is used.
Please refer to the Emulator hardware manual about details.

5. Packages and Product Correspondence

Package	MB90V340A -101 -102 -103 -104	MB90F351 MB90F351S MB90F352 MB90F352S	MB90F351A (S), MB90F351TA (S) MB90F352A (S), MB90F352TA (S) MB90F356A (S), MB90F356TA (S) MB90F357A (S), MB90F357TA (S) MB90351A (S), MB90351TA (S) MB90352A (S), MB90352TA (S) MB90356A (S), MB90356TA (S) MB90357A (S), MB90357TA (S)
PGA-299C-A01	○	×	×
FPT-64P-M23 (12 mm □, 0.65 mm pitch)	×	○	○
FPT-64P-M24 (10 mm □, 0.50 mm pitch)	×	×	○*

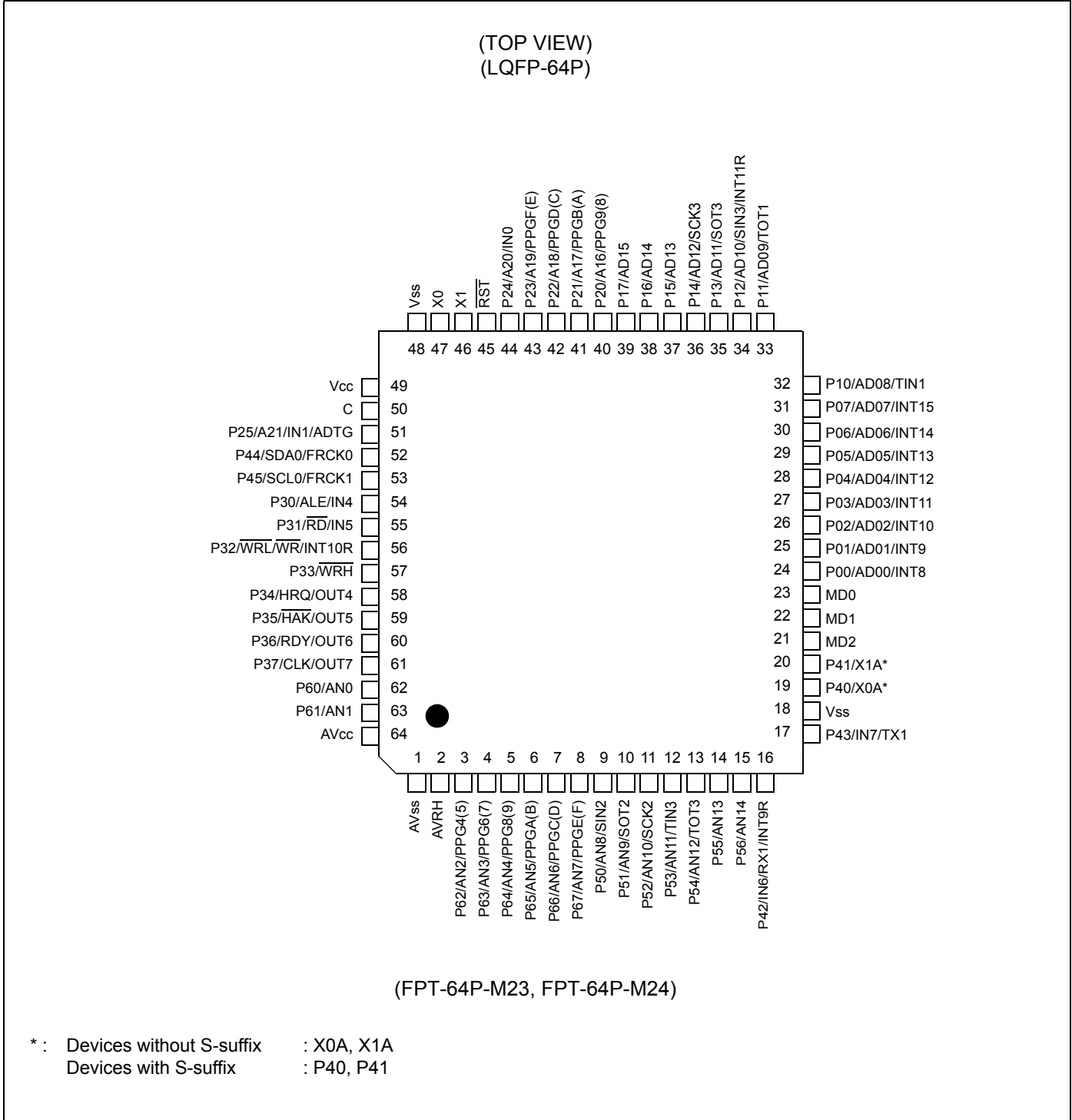
* : This device is under development.

○ : Yes, × : No

Note : Refer to "[Package Dimensions](#)" for detail of each package.

6. Pin Assignments

- MB90F351(S), MB90F352(S), MB90F351A(S), MB90F351TA(S), MB90F352A(S), MB90F352TA(S), MB90F356A(S), MB90F356TA(S), MB90F357A(S), MB90F357TA(S), MB90351A(S), MB90351TA(S), MB90352A(S), MB90352TA(S), MB90356A(S), MB90356TA(S), MB90357A(S), MB90357TA(S),



7. Pin Description

Pin No. LQFP64*	Pin name	Circuit type	Function
46	X1	A	Oscillation output pin
47	X0		Oscillation input pin
45	RST	E	Reset input pin
3 to 8	P62 to P67	I	General purpose I/O ports
	AN2 to AN7		Analog input pins for A/D converter
	PPG4 (5) , 6 (7) , 8 (9) , A (B) , C (D) , E (F)		Output pins for PPGs
9	P50	O	General purpose I/O port
	AN8		Analog input pin for A/D converter
	SIN2		Serial data input pin for UART2
10	P51	I	General purpose I/O port
	AN9		Analog input pin for A/D converter
	SOT2		Serial data output pin for UART2
11	P52	I	General purpose I/O port
	AN10		Analog input pin for A/D converter
	SCK2		Serial clock I/O pin for UART2
12	P53	I	General purpose I/O port
	AN11		Analog input pin for A/D converter
	TIN3		Event input pin for reload timer3
13	P54	I	General purpose I/O port
	AN12		Analog input pin for A/D converter
	TOT3		Output pin for reload timer3
14, 15	P55, P56	I	General purpose I/O ports
	AN13, AN14		Analog input pins for A/D converter
16	P42	F	General purpose I/O port
	IN6		Data sample input pin for input capture ICU6
	RX1		RX input pin for CAN1
	INT9R		External interrupt request input pin for INT9
17	P43	F	General purpose I/O port
	IN7		Data sample input pin for input capture ICU7
	TX1		TX output pin for CAN1
19, 20	P40, P41	F	General purpose I/O ports (devices with S-suffix and MB90V340A-101/103)
	X0A, X1A	B	X0A : Oscillation input pins for sub clock X1A : Oscillation output pins for sub clock (devices without S-suffix and MB90V340A-102/104)
24 to 31	P00 to P07	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD00 to AD07		Input/output pins of external address data bus lower 8 bits. This function is enabled when the external bus is enabled.
	INT8 to INT15		External interrupt request input pins for INT8 to INT15

(Continued)

Pin No. LQFP64*	Pin name	Circuit type	Function
32	P10	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD08		Input/output pin for external bus address data bus bit 8. This function is enabled when external bus is enabled.
	TIN1		Event input pin for reload timer1
33	P11	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD09		Input/output pin for external bus address data bus bit 9. This function is enabled when external bus is enabled.
	TOT1		Output pin for reload timer1
34	P12	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD10		Input/output pin for external bus address data bus bit 10. This function is enabled when external bus is enabled.
	SIN3		Serial data input pin for UART3
	INT11R		External interrupt request input pin for INT11
35	P13	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD11		Input/output pin for external bus address data bus bit 11. This function is enabled when external bus is enabled.
	SOT3		Serial data output pin for UART3
36	P14	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD12		Input/output pin for external bus address data bus bit 12. This function is enabled when external bus is enabled.
	SCK3		Clock input/output pin for UART3
37	P15	N	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD13		Input/output pin for external bus address data bus bit 13. This function is enabled when external bus is enabled.
38	P16	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD14		Input/output pin for external bus address data bus bit 14. This function is enabled when external bus is enabled.
39	P17	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	AD15		Input/output pin for external bus address data bus bit 15. This function is enabled when external bus is enabled.
40 to 43	P20 to P23	G	General purpose I/O ports. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pins are enabled as a general purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A16 to A19		Output pins for A16 to A19 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins A16 to A19.
	PPG9 (8) , PPGB (A) , PPGD (C) , PPGF (E)		Output pins for PPGs

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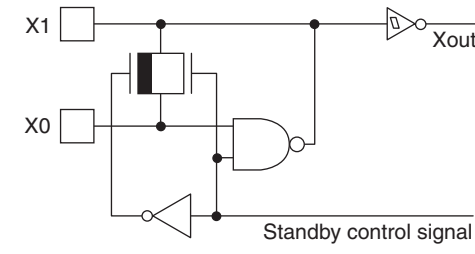
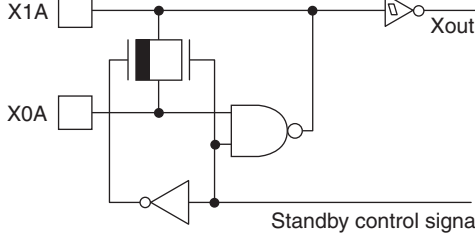
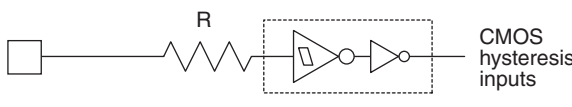
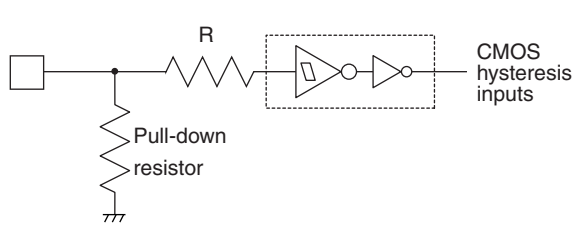
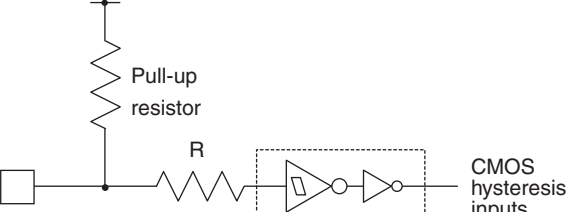
Pin No. LQFP64*	Pin name	Circuit type	Function
44	P24	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A20		Output pin for A20 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A20.
	IN0		Data sample input pin for input capture ICU0
51	P25	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
	A21		Output pin for A21 of the external address data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pin is enabled as high address output pin A21.
	IN1		Data sample input pin for input capture ICU1
	ADTG		Trigger input pin for A/D converter
52	P44	H	General purpose I/O port
	SDA0		Serial data I/O pin for I ² C 0
	FRCK0		Input pin for the 16-bit I/O Timer 0
53	P45	H	General purpose I/O port
	SCL0		Serial clock I/O pin for I ² C 0
	FRCK1		Input pin for the 16-bit I/O Timer 1
54	P30	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	ALE		Address latch enable output pin. This function is enabled when external bus is enabled.
	IN4		Data sample input pin for input capture ICU4
55	P31	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
	RD		Read strobe output pin for data bus. This function is enabled when external bus is enabled.
	IN5		Data sample input pin for input capture ICU5
56	P32	G	General purpose I/O port. The register can be set to select whether to <u>use a pull-up resistor</u> . This function is enabled either in single-chip mode or with the WR/WRL pin output disabled.
	$\overline{\text{WR/WRL}}$		Write strobe <u>output pin</u> for the data bus. This <u>function</u> is enabled when both the external bus and the <u>WR/WRL pin output are enabled</u> . WRL is used to write-strobe 8 lower bits of the data bus in 16-bit access. WR is used to write-strobe 8 bits of the data bus in 8-bit access.
	INT10R		External interrupt request input pin for INT10
57	P33	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled <u>either in single-chip mode, in external bus 8-bit mode or with the WRH pin output disabled</u> .
	WRH		Write strobe output pin for the 8 higher bits of the data bus. This function is enabled when the <u>external bus is enabled, when the external bus 16-bit mode is selected, and when the WRH output pin is enabled</u> .

(Continued)

Pin No.	Pin name	Circuit type	Function
LQFP64*			
58	P34	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT4		Waveform output pin for output compare OCU4
59	P35	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the hold function disabled.
	HAK		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
	OUT5		Waveform output pin for output compare OCU5
60	P36	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the external ready function disabled.
	RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
	OUT6		Waveform output pin for output compare OCU6
61	P37	G	General purpose I/O port. The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or with the CLK output disabled.
	CLK		CLK output pin. This function is enabled when both the external bus and CLK output are enabled.
	OUT7		Waveform output pin for output compare OCU7
62, 63	P60, P61	I	General purpose I/O ports
	AN0, AN1		Analog input pins for A/D converter
64	AV _{CC}	K	V _{CC} power input pin for analog circuits
2	AVRH	L	Reference voltage input for the A/D converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV _{CC} .
1	AV _{SS}	K	V _{SS} power input pin for analog circuits
22, 23	MD1, MD0	C	Input pins for specifying the operating mode
21	MD2	D	Input pin for specifying the operating mode
49	V _{CC}	—	Power (3.5 V to 5.5 V) input pin
18, 48	V _{SS}	—	Power (0 V) input pins
50	C	K	This is the power supply stabilization capacitor pin. It should be connected to a higher than or equal to 0.1 μF ceramic capacitor.

* : FPT-64P-M23, FPT-64P-M24

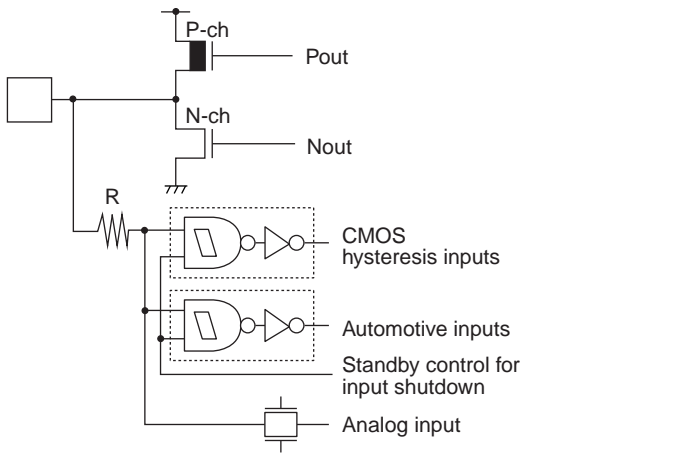
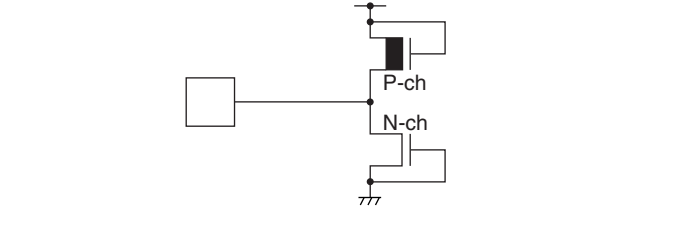
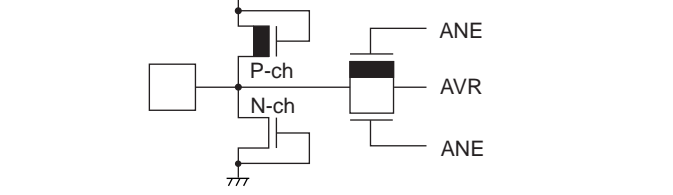
8. I/O Circuit Type

Type	Circuit	Remarks
A		Oscillation circuit <ul style="list-style-type: none"> • High-speed oscillation feedback resistor = approx. 1 MΩ
B		Oscillation circuit <ul style="list-style-type: none"> • Low-speed oscillation feedback resistor = approx. 10 MΩ
C		Mask ROM device: <ul style="list-style-type: none"> • CMOS hysteresis input pin Flash memory device: <ul style="list-style-type: none"> • CMOS input pin
D		Mask ROM device: <ul style="list-style-type: none"> • CMOS hysteresis input pin • Pull-down resistor value: approx. 50 kΩ Flash memory device: <ul style="list-style-type: none"> • CMOS input pin • No Pull-down
E		CMOS hysteresis input pin <ul style="list-style-type: none"> • Pull-up resistor value: approx. 50 kΩ

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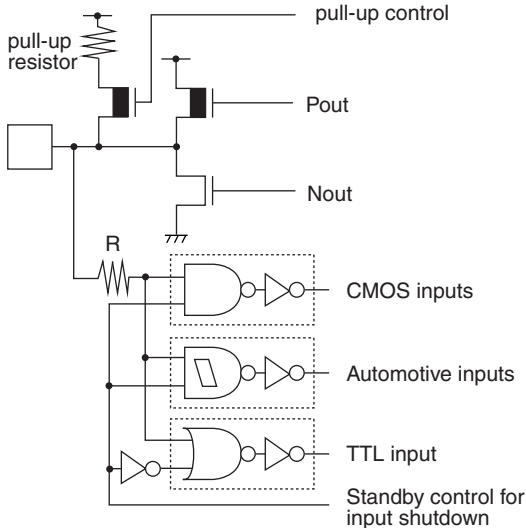
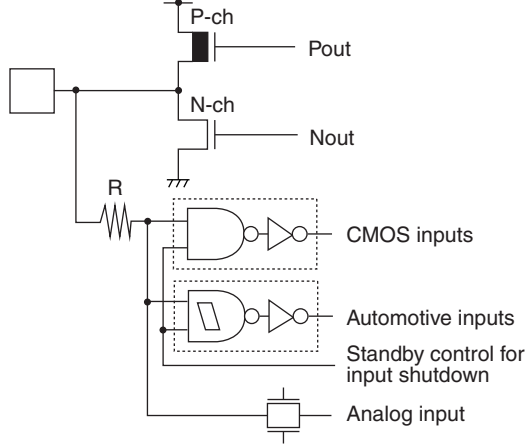
Type	Circuit	Remarks
F		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)
G		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) • Programmable pull-up resistor: approx. $50 \text{ k}\Omega$
H		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function)

(Continued)

Type	Circuit	Remarks
I		<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS hysteresis inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input
K		<ul style="list-style-type: none"> • Power supply input protection circuit
L		<ul style="list-style-type: none"> • A/D converter reference voltage power supply input pin, with the protection circuit • Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH.

(Continued)

(Continued)

Type	Circuit	Remarks
N	 <p>The diagram for Type N shows a pull-up resistor connected to a node that branches to a P-channel MOSFET (Pout) and an N-channel MOSFET (Nout). A resistor R is connected to the node between the pull-up resistor and the CMOS inputs. The CMOS inputs are connected to a NAND gate followed by an inverter. The Automotive inputs are connected to a NAND gate with a triangle symbol followed by an inverter. The TTL input is connected to a NAND gate followed by an inverter. A Standby control for input shutdown is connected to the CMOS inputs.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • TTL input (With the standby-time input shutdown function) • Programmable pull-up resistor: approx. $50 \text{ k}\Omega$
O	 <p>The diagram for Type O shows a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch) connected to a node. A resistor R is connected to the node between the pull-up resistor and the CMOS inputs. The CMOS inputs are connected to a NAND gate followed by an inverter. The Automotive inputs are connected to a NAND gate with a triangle symbol followed by an inverter. A Standby control for input shutdown is connected to the CMOS inputs. An Analog input is connected to the node between the pull-up resistor and the CMOS inputs.</p>	<ul style="list-style-type: none"> • CMOS level output ($I_{OL} = 4 \text{ mA}$, $I_{OH} = -4 \text{ mA}$) • CMOS inputs (With the standby-time input shutdown function) • Automotive input (With the standby-time input shutdown function) • A/D analog input

9. Handling Devices

Special care is required for the following when handling the device :

- Preventing latch-up
- Treatment of unused pins
- Using external clock
- Precautions for when not using a sub clock signal
- Notes on during operation of PLL clock mode
- Power supply pins (V_{CC}/V_{SS})
- Pull-up/down resistors
- Crystal Oscillator Circuit
- Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
- Connection of Unused Pins of A/D Converter
- Notes on Energization
- Stabilization of power supply voltage
- Initialization
- Port0 to port3 output during Power-on (External-bus mode)
- Notes on using CAN Function
- Flash security Function
- Correspondence with $T_A = +105\text{ }^\circ\text{C}$ or more
- Low voltage/CPU operation detection reset circuit
- Internal CR oscillation circuit

9.1 Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pin and V_{SS} pin.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

In using the devices, take sufficient care to avoid exceeding maximum ratings.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC} , $AVRH$) exceed the digital power-supply voltage.

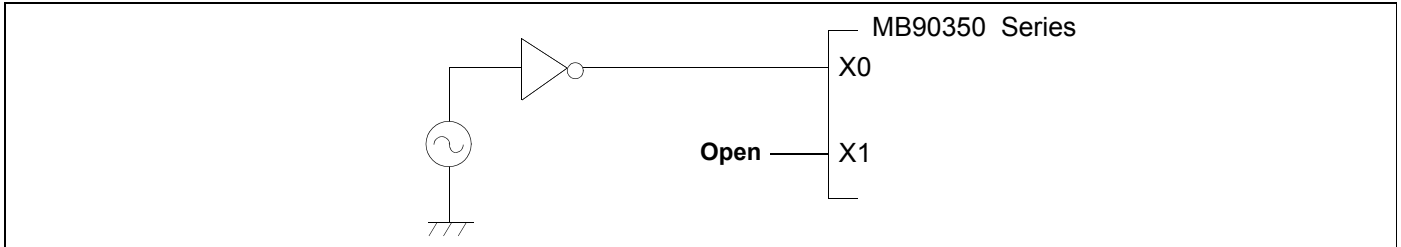
9.2 Handling unused pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than $2\text{ k}\Omega$.

Unused I/O pins should be set to the output state and can be left open, or the input state with the above described connection.

9.3 Using external clock

To use external clock, drive the X0 pin and leave X1 pin open.



9.4 Precautions for when not using a sub clock signal

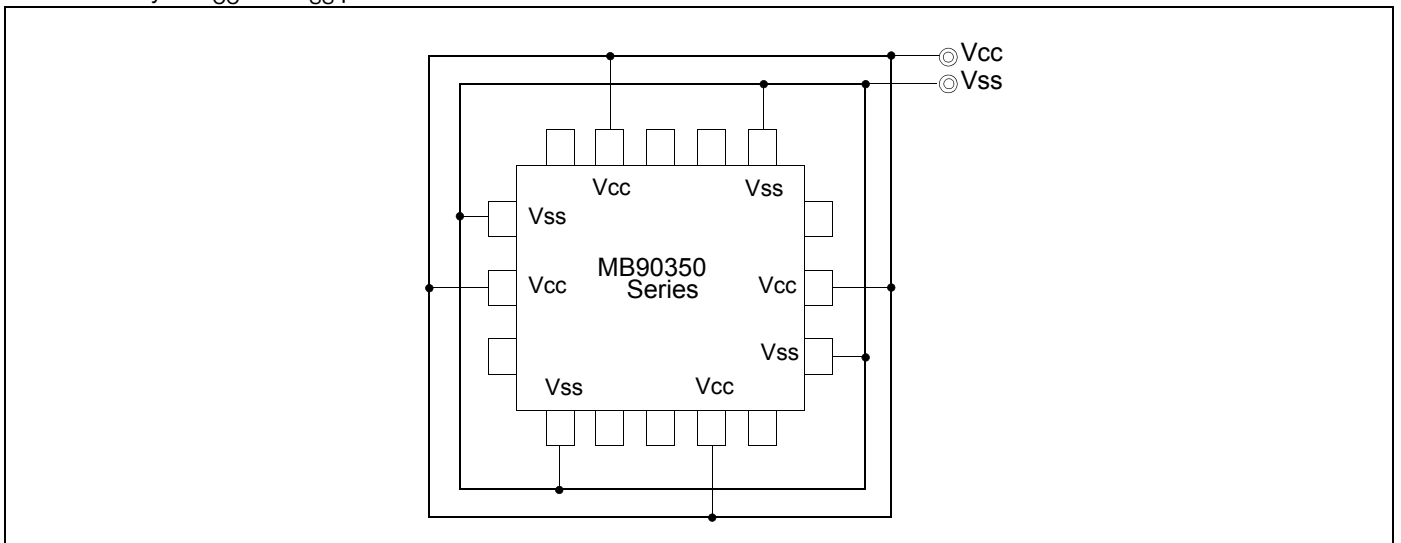
If you do not connect pins X0A and X1A to an oscillator, use pull-down handling on the X0A pin, and leave the X1A pin open.

9.5 Notes on during operation of PLL clock mode

If the PLL clock mode is selected, the microcontroller attempts to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

9.6 Power supply pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, from the point of view of device design, pins to be of the same potential are connected inside of the device to prevent such malfunctioning as latch up.
To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally. Connect V_{CC} and V_{SS} pins to the device from the current supply source at a low impedance.
- As a measure against power supply noise, connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device.



9.7 Pull-up/down resistors

The MB90350 series does not support internal pull-up/down resistors (Port 0 to Port 3: built-in pull-up resistors). Use external components where needed.

9.8 Crystal Oscillator Circuit

Noises around X0 or X1 pins may be possible causes of abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure, to the utmost effort, that lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0 and X1 pins with a ground area for stabilizing the operation.

Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device.

9.9 Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC} , $AVRH$) and analog inputs ($AN0$ to $AN14$) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter power supply and analog inputs. In this case, make sure that the voltage does not exceed $AVRH$ or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

9.10 Connection of Unused Pins of A/D Converter if A/D Converter is not used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = V_{SS}$.

9.11 Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 μ s or more (0.2 V to 2.7 V).

9.12 Stabilization of power supply voltage

A sudden change in the power supply voltage may cause the device to malfunction even within the specified V_{CC} power supply voltage operating range. Therefore, the V_{CC} power supply voltage should be stabilized.

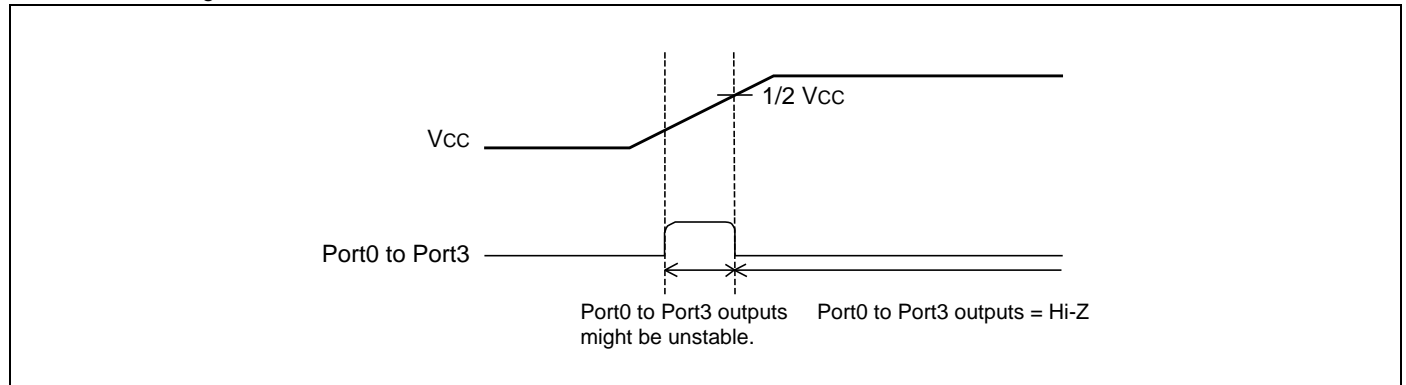
For reference, the power supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz to 60 Hz) fall below 10% of the standard V_{CC} power supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

9.13 Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

9.14 Port 0 to port 3 output during Power-on (External-bus mode)

As shown below, when power is turned in external-bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable.



9.15 Notes on using CAN Function

To use CAN function, please set "1" to DIRECT bit of CAN direct mode register (CDMR).

If DIRECT bit is set to "0" (initial value), wait states will be performed when accessing CAN registers.

Note : Please refer to section "22.15 CAN Direct Mode Register" in Hardware Manual of MB90350 series for detail of CAN direct mode register.

9.16 Flash security Function

The security byte is located in the area of the flash memory.

If protection code 01_H is written in the security byte, the flash memory is in the protected state by security.

Therefore please do not write 01_H in this address if you do not use the security function.

Please refer to following table for the address of the security byte.

	Flash memory size	Address for security bit
MB90F352(S) MB90F352A(S) MB90F352TA(S) MB90F357A(S) MB90F357TA(S)	Embedded 1 Mbit Flash Memory	FE0001 _H

9.17 Correspondence with T_A = +105 °C or more

If used exceeding T_A = +105 °C, please contact sales representatives for reliability limitations.

9.18 Low voltage/CPU operation reset circuit

The low voltage detection reset circuit is a function that monitors power supply voltage in order to detect when a voltage drops below a given voltage level. When a low voltage condition is detected, an internal reset signal is generated.

The CPU operation detection reset circuit is a 20-bit counter that uses oscillation as a count clock and generates an internal reset signal if not cleared within a given time after startup.

9.18.1 Low voltage detection reset circuit

Detection voltage
4.0 V ± 0.3 V

When a low voltage condition is detected, the low voltage detection flag (LVRC: LVRF) is set to “1” and an internal reset signal is output. Because the low voltage detection reset circuit continues to operate even in stop mode, detection of a low voltage condition generates an internal reset and releases stop mode.

During an internal RAM write cycle, low voltage reset is generated after the completion of writing. During the output of this internal reset, the reset output from the low voltage detection reset circuit is suppressed.

9.18.2 CPU operation detection reset circuit

The CPU operation detection reset circuit is a counter that prevents program runaway. The counter starts automatically after a power-on reset, and must be continually cleared within a given time. If the given time interval elapses and the counter has not been cleared, a cause such as infinite program looping is assumed and an internal reset signal is generated. The internal reset generated from the CPU operation detection circuit has a width of 5 machine cycles.

Interval time
2 ²⁰ /F _C (approx. 262 ms*)

* : This value assumes the interval time at an oscillation clock frequency of 4 MHz.

During recovery from standby mode, the detection period is the maximum interval plus 20 μs.

This circuit does not operate in modes where CPU operation is stopped.

The CPU operation detection reset circuit counter is cleared under any of the following conditions.

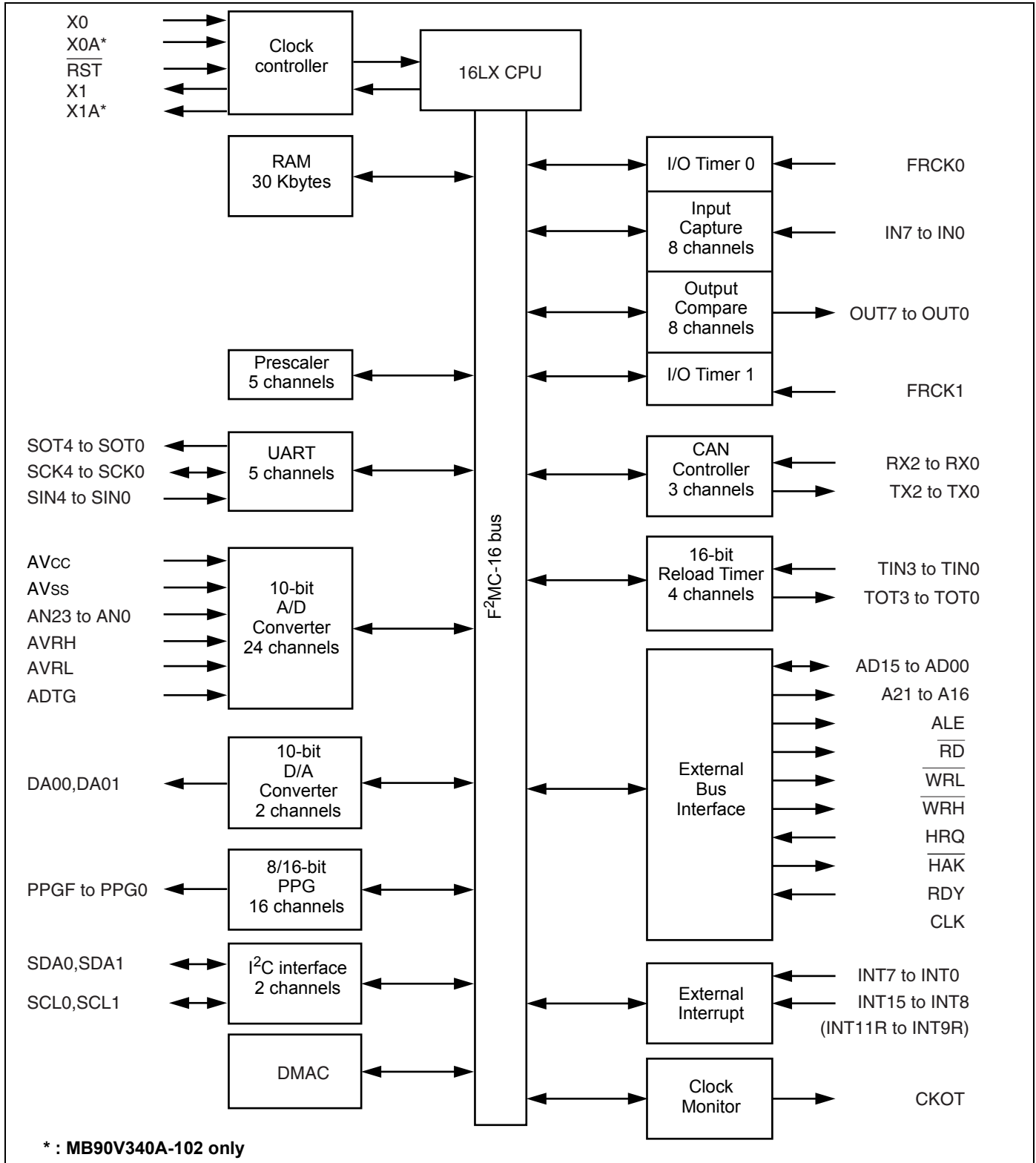
- “0” writing to CL bit of LVRC register
- Internal reset
- Main oscillation clock stop
- Transit to sleep mode
- Transit to timebase timer mode and watch mode

9.19 Internal CR oscillation circuit

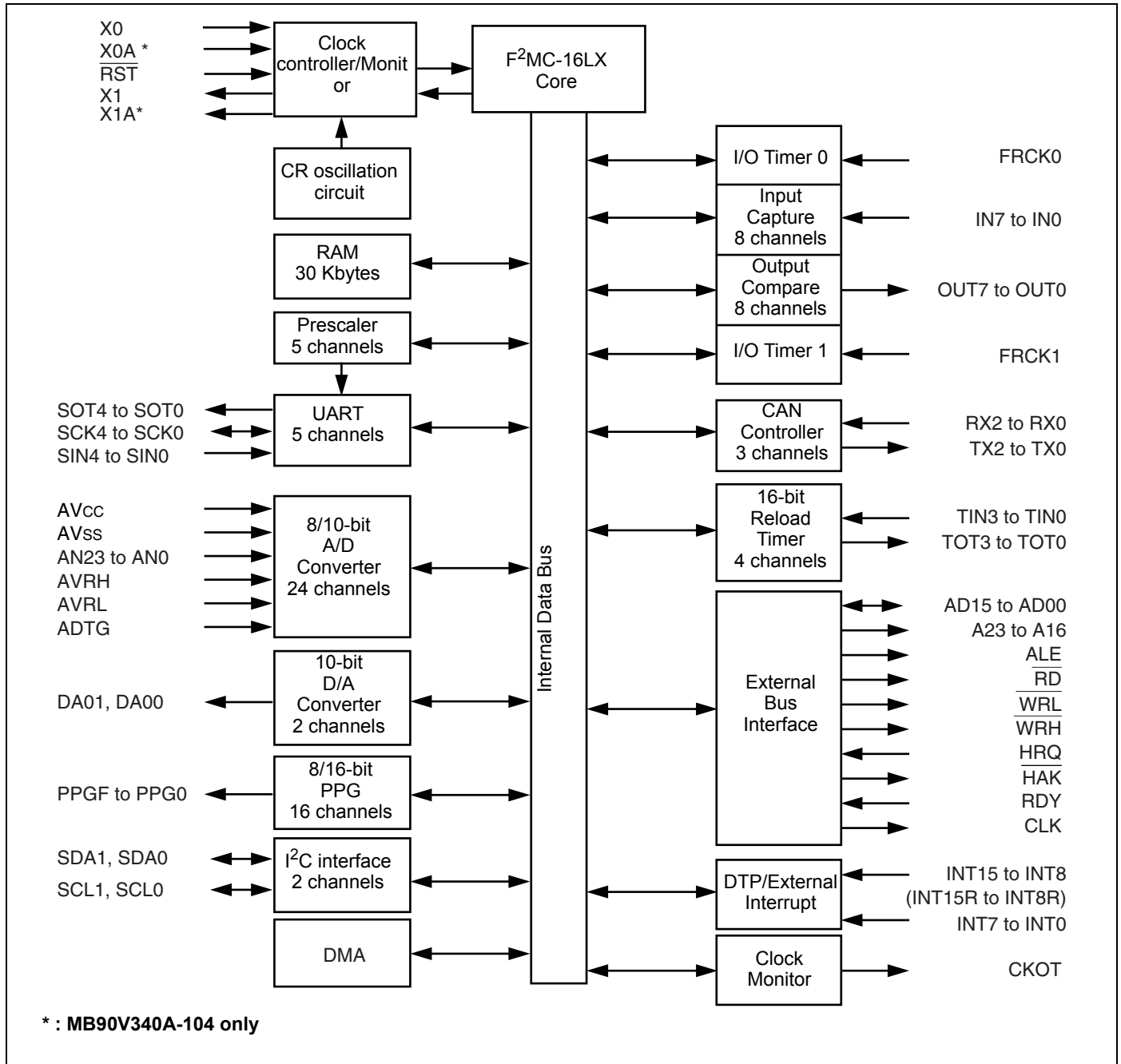
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Oscillation frequency	f_{RC}	50	100	200	kHz
Oscillation stabilization wait time	tstab	—	—	100	μ s

10. Block Diagrams

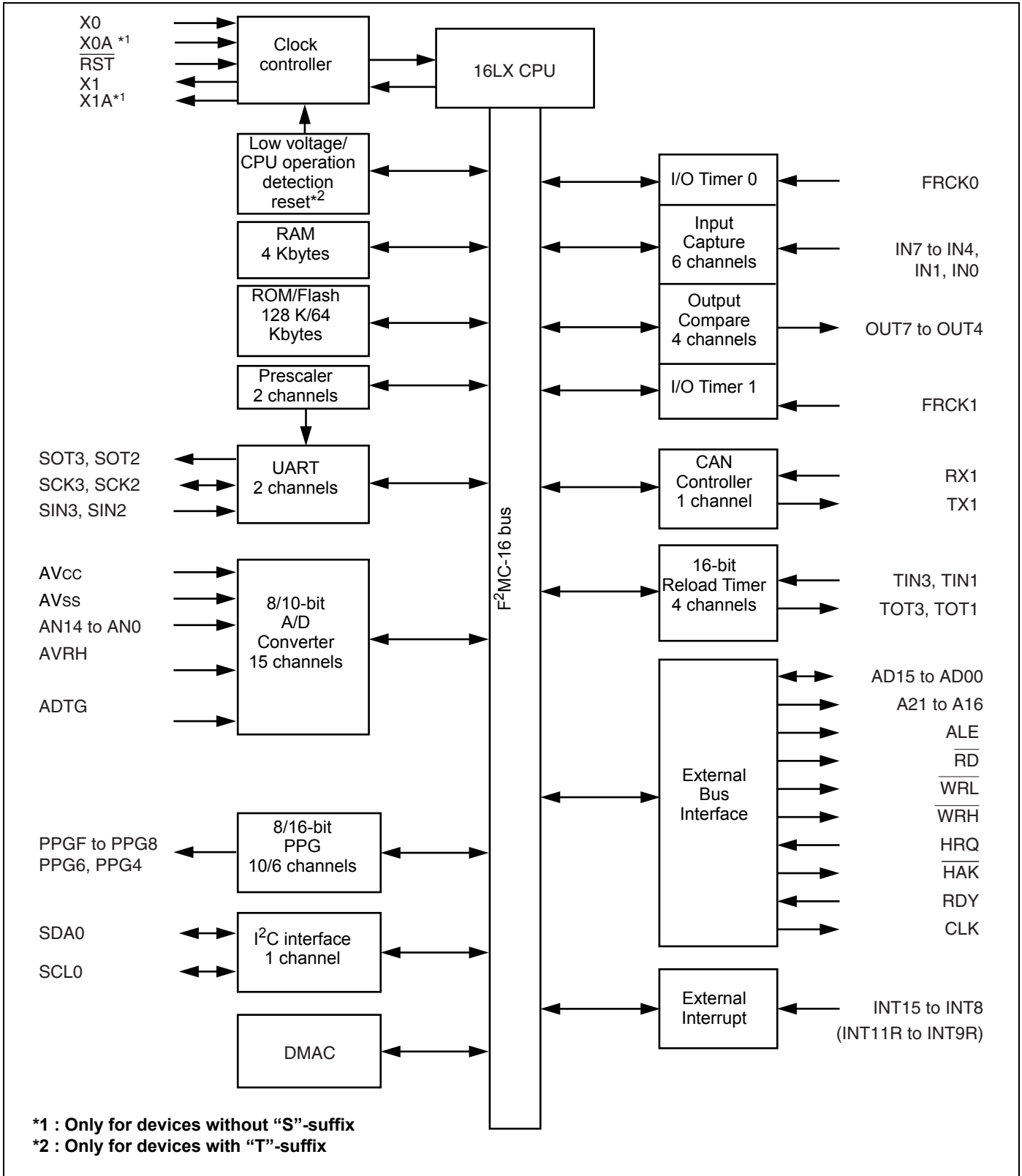
■ MB90V340A-101/102



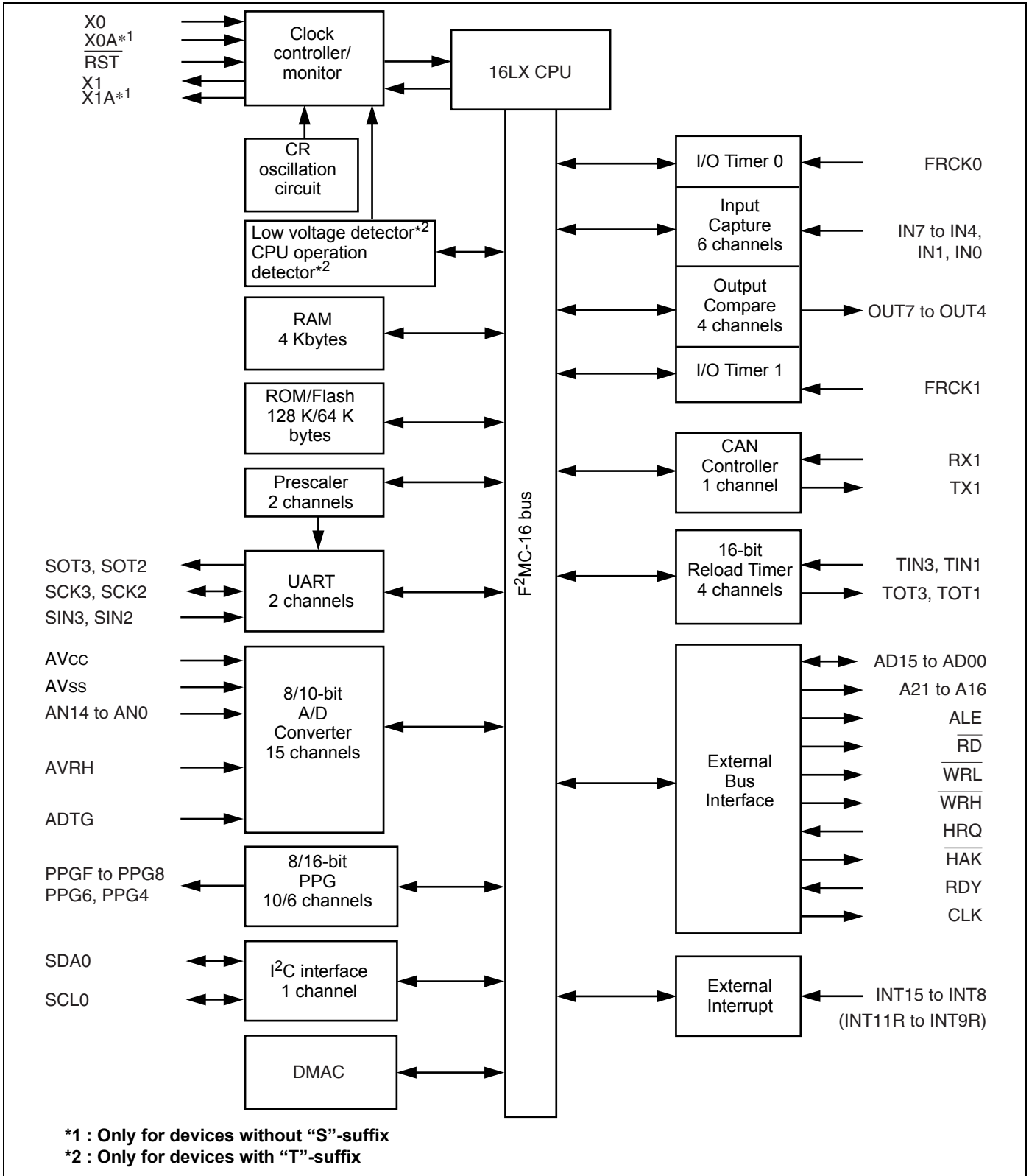
■ MB90V340A-103/104



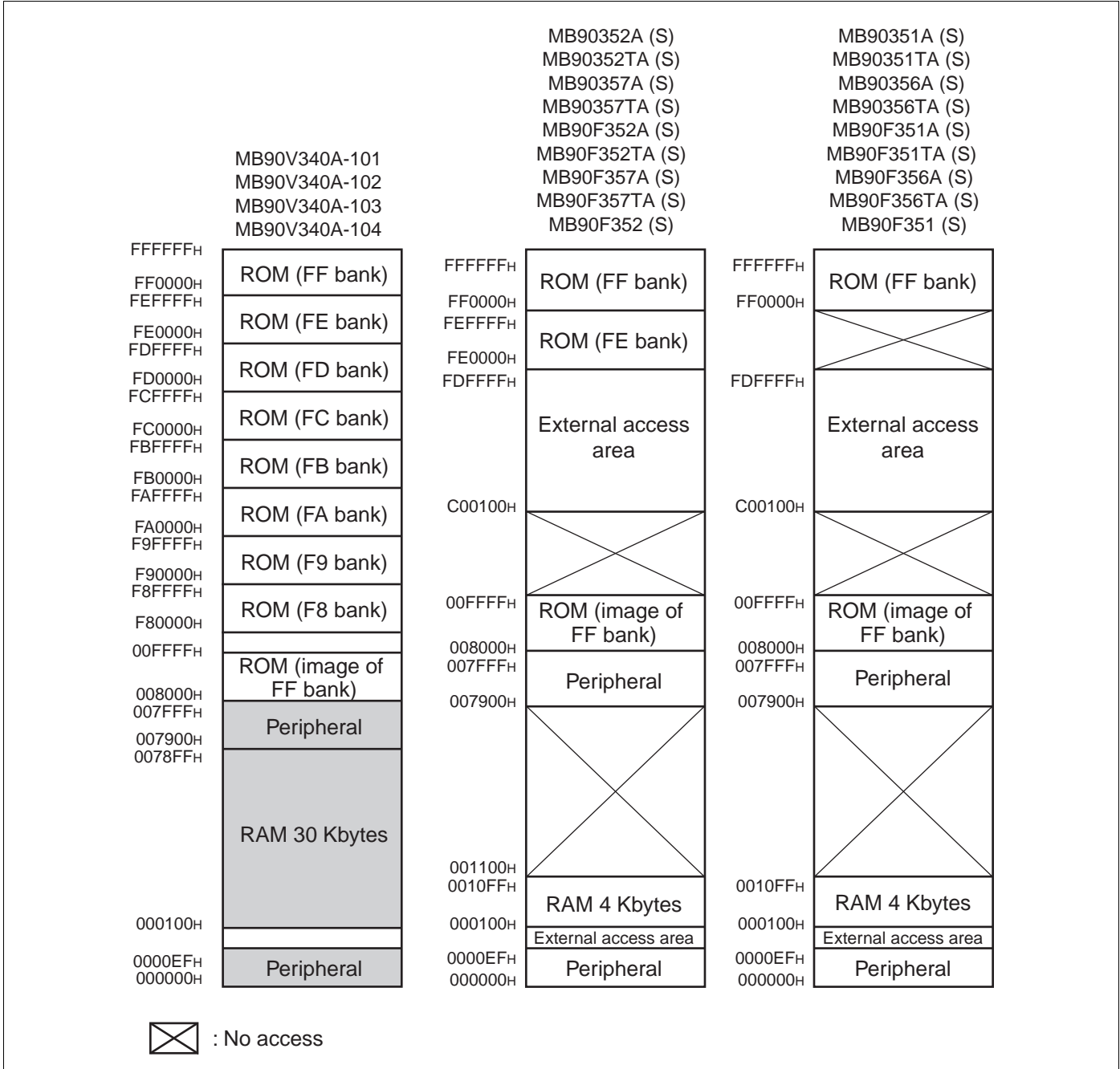
■ MB90F352 (S) , MB90F351 (S) , MB90F352A (S) , MB90F352TA (S) , MB90F351A (S) , MB90F351TA (S) , MB90352A (S) , MB90352TA (S) , MB90351A (S) , MB90351TA (S)



■ MB90F357A (S) , MB90F357TA (S) , MB90F356A (S) , MB90F356TA (S) , MB90357A (S) , MB90357TA (S) , MB90356A (S) , MB90356TA (S)



11. Memory Map



Note : The high-order portion of bank 00 gives the image of the FF bank ROM to make the small model of the C compiler effective. Since the low-order 16 bits are the same, the table in ROM can be referenced without using the far specification in the pointer declaration. For example, an attempt to access 00C000_H accesses the value at FFC000_H in ROM. The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00. The image between FF8000_H and FFFFFFF_H is visible in bank 00, while the image between FF0000_H and FF7FFF_H is visible only in bank FF.

12. I/O Map

Address	Register	Abbreviation	Access	Resource name	Initial value
00 _H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
01 _H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
02 _H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
03 _H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
04 _H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
05 _H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
06 _H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
07 _H to 0A _H	Reserved				
0B _H	Port 5 Analog Input Enable Register	ADER5	R/W	Port 5, A/D	11111111 _B
0C _H	Port 6 Analog Input Enable Register	ADER6	R/W	Port 6, A/D	11111111 _B
0D _H	Reserved				
0E _H	Input Level Select Register 0	ILSR0	R/W	Ports	00000000 _B
0F _H	Input Level Select Register 1	ILSR1	R/W	Ports	00000000 _B
10 _H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000 _B
11 _H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000 _B
12 _H	Port 2 Direction Register	DDR2	R/W	Port 2	XX000000 _B
13 _H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000 _B
14 _H	Port 4 Direction Register	DDR4	R/W	Port 4	XX000000 _B
15 _H	Port 5 Direction Register	DDR5	R/W	Port 5	X0000000 _B
16 _H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000 _B
17 _H to 19 _H	Reserved				
1A _H	SIN input Level Setting Register	DDRA	W	UART2, UART3	X00XXXXX _B
1B _H	Reserved				
1C _H	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000 _B
1D _H	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000 _B
1E _H	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000 _B
1F _H	Port 3 Pull-up Control Register	PUCR3	R/W	Port 3	00000000 _B
20 _H to 37 _H	Reserved				
38 _H	PPG 4 Operation Mode Control Register	PPGC4	W, R/W	16-bit Programmable Pulse Generator 4/5	0X000XX1 _B
39 _H	PPG 5 Operation Mode Control Register	PPGC5	W, R/W		0X000001 _B
3A _H	PPG 4/5 Count Clock Select Register	PPG45	R/W		000000X0 _B
3B _H	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	00000000 _B
3C _H	PPG 6 Operation Mode Control Register	PPGC6	W, R/W	16-bit Programmable Pulse Generator 6/7	0X000XX1 _B
3D _H	PPG 7 Operation Mode Control Register	PPGC7	W, R/W		0X000001 _B
3E _H	PPG 6/7 Count Clock Select Register	PPG67	R/W		000000X0 _B
3F _H	Reserved				
40 _H	PPG 8 Operation Mode Control Register	PPGC8	W, R/W	16-bit Programmable Pulse Generator 8/9	0X000XX1 _B
41 _H	PPG 9 Operation Mode Control Register	PPGC9	W, R/W		0X000001 _B
42 _H	PPG 8/9 Count Clock Select Register	PPG89	R/W		000000X0 _B
43 _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value	
44 _H	PPG A Operation Mode Control Register	PPGCA	W, R/W	16-bit Programmable Pulse Generator A/B	0X000XX1 _B	
45 _H	PPG B Operation Mode Control Register	PPGCB	W, R/W		0X000001 _B	
46 _H	PPG A/B Count Clock Select Register	PPGAB	R/W		000000X0 _B	
47 _H	Reserved					
48 _H	PPG C Operation Mode Control Register	PPGCC	W,R/W	16-bit Programmable Pulse Generator C/D	0X000XX1 _B	
49 _H	PPG D Operation Mode Control Register	PPGCD	W,R/W		0X000001 _B	
4A _H	PPG C/D Count Clock Select Register	PPGCD	R/W		000000X0 _B	
4B _H	Reserved					
4C _H	PPG E Operation Mode Control Register	PPGCE	W,R/W	16-bit Programmable Pulse Generator E/F	0X000XX1 _B	
4D _H	PPG F Operation Mode Control Register	PPGCF	W,R/W		0X000001 _B	
4E _H	PPG E/F Count Clock Select Register	PPGEF	R/W		000000X0 _B	
4F _H	Reserved					
50 _H	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	00000000 _B	
51 _H	Input Capture Edge Register 0/1	ICE01	R/W, R		XXX0X0XX _B	
52 _H , 53 _H	Reserved					
54 _H	Input Capture Control Status Register 4/5	ICS45	R/W	Input Capture 4/5	00000000 _B	
55 _H	Input Capture Edge Register 4/5	ICE45	R		XXXXXXXXXX _B	
56 _H	Input Capture Control Status Register 6/7	ICS67	R/W	Input Capture 6/7	00000000 _B	
57 _H	Input Capture Edge Register 6/7	ICE67	R/W, R		XXX000XX _B	
58 _H to 5B _H	Reserved					
5C _H	Output Compare Control Status Register 4	OCS4	R/W	Output Compare 4/5	0000XX00 _B	
5D _H	Output Compare Control Status Register 5	OCS5	R/W		0XX00000 _B	
5E _H	Output Compare Control Status Register 6	OCS6	R/W	Output Compare 6/7	0000XX00 _B	
5F _H	Output Compare Control Status Register 7	OCS7	R/W		0XX00000 _B	
60 _H	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	00000000 _B	
61 _H	Timer Control Status Register 0	TMCSR0	R/W		XXXX0000 _B	
62 _H	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	00000000 _B	
63 _H	Timer Control Status Register 1	TMCSR1	R/W		XXXX0000 _B	
64 _H	Timer Control Status Register 2	TMCSR2	R/W	16-bit Reload Timer 2	00000000 _B	
65 _H	Timer Control Status Register 2	TMCSR2	R/W		XXXX0000 _B	
66 _H	Timer Control Status Register 3	TMCSR3	R/W	16-bit Reload Timer 3	00000000 _B	
67 _H	Timer Control Status Register 3	TMCSR3	R/W		XXXX0000 _B	
68 _H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	000XXXX0 _B	
69 _H	A/D Control Status Register 1	ADCS1	R/W		0000000X _B	
6A _H	A/D Data Register 0	ADCR0	R		00000000 _B	
6B _H	A/D Data Register 1	ADCR1	R		XXXXXXXX00 _B	
6C _H	ADC Setting Register 0	ADSR0	R/W		00000000 _B	
6D _H	ADC Setting Register 1	ADSR1	R/W		00000000 _B	
6E _H	Low Voltage/CPU Operation Detection Reset Control Register	LVRC	R/W, W		Low Voltage/CPU Operation Detection Reset	00111000 _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
6F _H	ROM Mirror Function Select Register	ROMM	W	ROM Mirror	XXXXXXXX _{1B}
70 _H to 7F _H	Reserved				
80 _H to 8F _H	Reserved for CAN Interface 1. Refer to “CAN Controllers”				
90 _H to 9A _H	Reserved				
9B _H	DMA Descriptor Channel Specification Register	DCSR	R/W	DMA	00000000 _B
9C _H	DMA Status Register L	DSRL	R/W		00000000 _B
9D _H	DMA Status Register H	DSRH	R/W		00000000 _B
9E _H	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	00000000 _B
9F _H	Delayed Interrupt/Release Register	DIRR	R/W	Delayed Interrupt	XXXXXXXX0 _B
A0 _H	Low-power Consumption Mode Control Register	LPMCR	W,R/W	Low Power Consumption Control Circuit	00011000 _B
A1 _H	Clock Selection Register	CKSCR	R,R/W	Low Power Consumption Control Circuit	11111100 _B
A2 _H , A3 _H	Reserved				
A4 _H	DMA Stop Status Register	DSSR	R/W	DMA	00000000 _B
A5 _H	Automatic Ready Function Selection Register	ARSR	W	External Memory Access	0011XX00 _B
A6 _H	External Address Output Control Register	HACR	W		00000000 _B
A7 _H	Bus Control Signal Selection Register	ECSR	W		0000000X _B
A8 _H	Watchdog Control Register	WDTC	R,W	Watchdog Timer	XXXXX111 _B
A9 _H	Timebase Timer Control Register	TBTC	W,R/W	Timebase timer	1XX00100 _B
AA _H	Watch Timer Control Register	WTC	R,R/W	Watch Timer	1X001000 _B
AB _H	Reserved				
AC _H	DMA Enable Register L	DERL	R/W	DMA	00000000 _B
AD _H	DMA Enable Register H	DERH	R/W		00000000 _B
AE _H	Flash Control Status Register (Flash Devices only. Otherwise reserved)	FMCS	R,R/W	Flash Memory	000X0000 _B
AF _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
B0 _H	Interrupt Control Register 00	ICR00	W,R/W	Interrupt Control	00000111 _B
B1 _H	Interrupt Control Register 01	ICR01	W,R/W		00000111 _B
B2 _H	Interrupt Control Register 02	ICR02	W,R/W		00000111 _B
B3 _H	Interrupt Control Register 03	ICR03	W,R/W		00000111 _B
B4 _H	Interrupt Control Register 04	ICR04	W,R/W		00000111 _B
B5 _H	Interrupt Control Register 05	ICR05	W,R/W		00000111 _B
B6 _H	Interrupt Control Register 06	ICR06	W,R/W		00000111 _B
B7 _H	Interrupt Control Register 07	ICR07	W,R/W		00000111 _B
B8 _H	Interrupt Control Register 08	ICR08	W,R/W		00000111 _B
B9 _H	Interrupt Control Register 09	ICR09	W,R/W		00000111 _B
BA _H	Interrupt Control Register 10	ICR10	W,R/W		00000111 _B
BB _H	Interrupt Control Register 11	ICR11	W,R/W		00000111 _B
BC _H	Interrupt Control Register 12	ICR12	W,R/W		00000111 _B
BD _H	Interrupt Control Register 13	ICR13	W,R/W		00000111 _B
BE _H	Interrupt Control Register 14	ICR14	W,R/W		00000111 _B
BF _H	Interrupt Control Register 15	ICR15	W,R/W		00000111 _B
C0 _H to C9 _H	Reserved				
CA _H	External Interrupt Enable Register 1	ENIR1	R/W	External Interrupt 1	00000000 _B
CB _H	External Interrupt Source Register 1	EIRR1	R/W		XXXXXXXX _B
CC _H	External Interrupt Level Register 1	ELVR1	R/W		00000000 _B
CD _H	External Interrupt Level Register 1	ELVR1	R/W		00000000 _B
CE _H	External Interrupt Source Select Register	EISSR	R/W		00000000 _B
CF _H	PLL/Sub clock Control register	PSCCR	W	PLL	XXXX0000 _B
D0 _H	DMA Buffer Address Pointer L	BAPL	R/W	DMA	XXXXXXXX _B
D1 _H	DMA Buffer Address Pointer M	BAPM	R/W		XXXXXXXX _B
D2 _H	DMA Buffer Address Pointer H	BAPH	R/W		XXXXXXXX _B
D3 _H	DMA Control Register	DMACS	R/W		XXXXXXXX _B
D4 _H	I/O Register Address Pointer L	IOAL	R/W		XXXXXXXX _B
D5 _H	I/O Register Address Pointer H	IOAH	R/W		XXXXXXXX _B
D6 _H	Data Counter L	DCTL	R/W		XXXXXXXX _B
D7 _H	Data Counter H	DCTH	R/W	XXXXXXXX _B	
D8 _H	Serial Mode Register 2	SMR2	W,R/W	UART2	00000000 _B
D9 _H	Serial Control Register 2	SCR2	W,R/W		00000000 _B
DA _H	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000 _B
DB _H	Serial Status Register 2	SSR2	R,R/W		00001000 _B
DC _H	Extended Communication Control Register 2	ECCR2	R,W, R/W		000000XX _B
DD _H	Extended Status/Control Register 2	ESCR2	R/W		00000100 _B
DE _H	Baud Rate Generator Register 20	BGR20	R/W		00000000 _B
DF _H	Baud Rate Generator Register 21	BGR21	R/W		00000000 _B
E0 _H to EF _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
F0 _H to FF _H	External area				
7900 _H to 7907 _H	Reserved				
7908 _H	Reload Register L4	PRL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
7909 _H	Reload Register H4	PRLH4	R/W		XXXXXXXX _B
790A _H	Reload Register L5	PRL5	R/W		XXXXXXXX _B
790B _H	Reload Register H5	PRLH5	R/W		XXXXXXXX _B
790C _H	Reload Register L6	PRL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
790D _H	Reload Register H6	PRLH6	R/W		XXXXXXXX _B
790E _H	Reload Register L7	PRL7	R/W		XXXXXXXX _B
790F _H	Reload Register H7	PRLH7	R/W		XXXXXXXX _B
7910 _H	Reload Register L8	PRL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX _B
7911 _H	Reload Register H8	PRLH8	R/W		XXXXXXXX _B
7912 _H	Reload Register L9	PRL9	R/W		XXXXXXXX _B
7913 _H	Reload Register H9	PRLH9	R/W		XXXXXXXX _B
7914 _H	Reload Register LA	PRLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX _B
7915 _H	Reload Register HA	PRLHA	R/W		XXXXXXXX _B
7916 _H	Reload Register LB	PRLB	R/W		XXXXXXXX _B
7917 _H	Reload Register HB	PRLHB	R/W		XXXXXXXX _B
7918 _H	Reload Register LC	PRLC	R/W	16-bit Programmable Pulse Generator C/D	XXXXXXXX _B
7919 _H	Reload Register HC	PRLHC	R/W		XXXXXXXX _B
791A _H	Reload Register LD	PRLD	R/W		XXXXXXXX _B
791B _H	Reload Register HD	PRLHD	R/W		XXXXXXXX _B
791C _H	Reload Register LE	PRLLE	R/W	16-bit Programmable Pulse Generator E/F	XXXXXXXX _B
791D _H	Reload Register HE	PRLHE	R/W		XXXXXXXX _B
791E _H	Reload Register LF	PRLLF	R/W		XXXXXXXX _B
791F _H	Reload Register HF	PRLHF	R/W		XXXXXXXX _B
7920 _H	Input Capture Register 0	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
7921 _H	Input Capture Register 0	IPCP0	R		XXXXXXXX _B
7922 _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
7923 _H	Input Capture Register 1	IPCP1	R		XXXXXXXX _B
7924 _H to 7927 _H	Reserved				
7928 _H	Input Capture Register 4	IPCP4	R	Input Capture 4/5	XXXXXXXX _B
7929 _H	Input Capture Register 4	IPCP4	R		XXXXXXXX _B
792A _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B
792B _H	Input Capture Register 5	IPCP5	R		XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
792C _H	Input Capture Register 6	IPCP6	R	Input Capture 6/7	XXXXXXXX _B
792D _H	Input Capture Register 6	IPCP6	R		XXXXXXXX _B
792E _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B
792F _H	Input Capture Register 7	IPCP7	R		XXXXXXXX _B
7930 _H to 7937 _H	Reserved				
7938 _H	Output Compare Register 4	OCCP4	R/W	Output Compare 4/5	XXXXXXXX _B
7939 _H	Output Compare Register 4	OCCP4	R/W		XXXXXXXX _B
793A _H	Output Compare Register 5	OCCP5	R/W		XXXXXXXX _B
793B _H	Output Compare Register 5	OCCP5	R/W		XXXXXXXX _B
793C _H	Output Compare Register 6	OCCP6	R/W	Output Compare 6/7	XXXXXXXX _B
793D _H	Output Compare Register 6	OCCP6	R/W		XXXXXXXX _B
793E _H	Output Compare Register 7	OCCP7	R/W		XXXXXXXX _B
793F _H	Output Compare Register 7	OCCP7	R/W		XXXXXXXX _B
7940 _H	Timer Data Register 0	TCDT0	R/W	I/O Timer 0	0000000 _B
7941 _H	Timer Data Register 0	TCDT0	R/W		0000000 _B
7942 _H	Timer Control Status Register 0	TCCSL0	R/W		0000000 _B
7943 _H	Timer Control Status Register 0	TCCSH0	R/W		0XXXXXXXX _B
7944 _H	Timer Data Register 1	TCDT1	R/W	I/O Timer 1	0000000 _B
7945 _H	Timer Data Register 1	TCDT1	R/W		0000000 _B
7946 _H	Timer Control Status Register 1	TCCSL1	R/W		0000000 _B
7947 _H	Timer Control Status Register 1	TCCSH1	R/W		0XXXXXXXX _B
7948 _H	Timer Register 0/Reload Register 0	TMR0/TMRL R0	R/W	16-bit Reload Timer 0	XXXXXXXX _B
7949 _H			R/W		XXXXXXXX _B
794A _H	Timer Register 1/Reload Register 1	TMR1/TMRL R1	R/W	16-bit Reload Timer 1	XXXXXXXX _B
794B _H			R/W		XXXXXXXX _B
794C _H	Timer Register 2/Reload Register 2	TMR2/TMRL R2	R/W	16-bit Reload Timer 2	XXXXXXXX _B
794D _H			R/W		XXXXXXXX _B
794E _H	Timer Register 3/Reload Register 3	TMR3/TMRL R3	R/W	16-bit Reload Timer 3	XXXXXXXX _B
794F _H			R/W		XXXXXXXX _B
7950 _H	Serial Mode Register 3	SMR3	W, R/W	UART3	0000000 _B
7951 _H	Serial Control Register 3	SCR3	W, R/W		0000000 _B
7952 _H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		0000000 _B
7953 _H	Serial Status Register 3	SSR3	R,R/W		0000100 _B
7954 _H	Extended Communication Control Register 3	ECCR3	R,W, R/W		000000XX _B
7955 _H	Extended Status/Control Register 3	ESCR3	R/W		00000100 _B
7956 _H	Baud Rate Generator Register 30	BGR30	R/W		0000000 _B
7957 _H	Baud Rate Generator Register 31	BGR31	R/W		0000000 _B
7958 _H , 7959 _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
7960 _H	Clock Monitor Function Control Register	CSVCR	R, R/W	Clock Monitor	00011100 _B
7961 _H to 796D _H	Reserved				
796E _H	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	XXXXXXXX0 _B
796F _H	Reserved				
7970 _H	I ² C Bus Status Register 0	IBSR0	R	I ² C Interface 0	00000000 _B
7971 _H	I ² C Bus Control Register 0	IBCR0	W,R/W		00000000 _B
7972 _H	I ² C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000 _B
7973 _H		ITBAH0	R/W		00000000 _B
7974 _H	I ² C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111 _B
7975 _H		ITMKH0	R/W		00111111 _B
7976 _H	I ² C 7-bit Slave Address Register 0	ISBA0	R/W		00000000 _B
7977 _H	I ² C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111 _B
7978 _H	I ² C data register 0	IDAR0	R/W		00000000 _B
7979 _H , 797A _H	Reserved				
797B _H	I ² C Clock Control Register 0	ICCR0	R/W	I ² C Interface 0	00011111 _B
797C _H to 79A1 _H	Reserved				
79A2 _H	Flash Write Control Register 0	FWR0	R/W	Dual Operation Flash	00000000 _B
79A3 _H	Flash Write Control Register 1	FWR1	R/W		00000000 _B
79A4 _H	Sector Change Setting Register	SSR0	R/W		00XXXXX0 _B
79A5 _H to 79C1 _H	Reserved				
79C2 _H	Setting Prohibited				
79C3 _H to 79DF _H	Reserved				
79E0 _H	Detect Address Setting Register 0	PADR0	R/W	Address Match Detection 0	XXXXXXXX _B
79E1 _H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXX _B
79E2 _H	Detect Address Setting Register 0	PADR0	R/W		XXXXXXXX _B
79E3 _H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXX _B
79E4 _H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXX _B
79E5 _H	Detect Address Setting Register 1	PADR1	R/W		XXXXXXXX _B
79E6 _H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXX _B
79E7 _H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXX _B
79E8 _H	Detect Address Setting Register 2	PADR2	R/W		XXXXXXXX _B
79E9 _H to 79EF _H	Reserved				

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Resource name	Initial value
79F0 _H	Detect Address Setting Register 3	PADR3	R/W	Address Match Detection 1	XXXXXXXX _B
79F1 _H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXX _B
79F2 _H	Detect Address Setting Register 3	PADR3	R/W		XXXXXXXX _B
79F3 _H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXX _B
79F4 _H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXX _B
79F5 _H	Detect Address Setting Register 4	PADR4	R/W		XXXXXXXX _B
79F6 _H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXX _B
79F7 _H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXX _B
79F8 _H	Detect Address Setting Register 5	PADR5	R/W		XXXXXXXX _B
79F9 _H to 7BFF _H	Reserved				
7C00 _H to 7CFF _H	Reserved for CAN Interface 1. Refer to “CAN Controllers”				
7D00 _H to 7DFF _H	Reserved for CAN Interface 1. Refer to “CAN Controllers”				
7E00 _H to 7FFF _H	Reserved				

Notes :

- Initial value of “X” represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results reading “X”.

13. CAN Controllers

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers

Address	Register	Abbreviation	Access	Initial Value
CAN1				
000080 _H	Message buffer enable register	BVALR	R/W	00000000 _B 00000000 _B
000081 _H				
000082 _H	Transmit request register	TREQR	R/W	00000000 _B 00000000 _B
000083 _H				
000084 _H	Transmit cancel register	TCANR	W	00000000 _B 00000000 _B
000085 _H				
000086 _H	Transmission complete register	TCR	R/W	00000000 _B 00000000 _B
000087 _H				
000088 _H	Receive complete register	RCR	R/W	00000000 _B 00000000 _B
000089 _H				
00008A _H	Remote request receiving register	RRTRR	R/W	00000000 _B 00000000 _B
00008B _H				
00008C _H	Receive overrun register	ROVRR	R/W	00000000 _B 00000000 _B
00008D _H				
00008E _H	Reception interrupt enable register	RIER	R/W	00000000 _B 00000000 _B
00008F _H				
007D00 _H	Control status register	CSR	R/W, W R/W, R	0XXXX0X1 _B 00XXX000 _B
007D01 _H				
007D02 _H	Last event indicator register	LEIR	R/W	00X0000 _B XXXXXXXX _B
007D03 _H				
007D04 _H	Receive/transmit error counter	RTEC	R	00000000 _B 00000000 _B
007D05 _H				
007D06 _H	Bit timing register	BTR	R/W	11111111 _B X1111111 _B
007D07 _H				
007D08 _H	IDE register	IDER	R/W	XXXXXXXX _B XXXXXXXX _B
007D09 _H				
007D0A _H	Transmit RTR register	TRTRR	R/W	00000000 _B 00000000 _B
007D0B _H				

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
CAN1				
007D0C _H	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX _B
007D0D _H				XXXXXXXX _B
007D0E _H	Transmit interrupt enable register	TIER	R/W	00000000 _B
007D0F _H				00000000 _B
007D10 _H	Acceptance mask select register	AMSR	R/W	XXXXXXXX _B
007D11 _H				XXXXXXXX _B
007D12 _H				XXXXXXXX _B
007D13 _H				XXXXXXXX _B
007D14 _H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX _B
007D15 _H				XXXXXXXX _B
007D16 _H				XXXXXXXX _B
007D17 _H				XXXXXXXX _B
007D18 _H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX _B
007D19 _H				XXXXXXXX _B
007D1A _H				XXXXXXXX _B
007D1B _H				XXXXXXXX _B

List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C00 _H to 007C1F _H	General-purpose RAM	—	R/W	XXXXXXXX _B to XXXXXXXX _B
007C20 _H	ID register 0	IDR0	R/W	XXXXXXXX _B XXXXXXXX _B
007C21 _H				XXXXXXXX _B XXXXXXXX _B
007C22 _H				
007C23 _H				
007C24 _H	ID register 1	IDR1	R/W	XXXXXXXX _B XXXXXXXX _B
007C25 _H				XXXXXXXX _B XXXXXXXX _B
007C26 _H				
007C27 _H				
007C28 _H	ID register 2	IDR2	R/W	XXXXXXXX _B XXXXXXXX _B
007C29 _H				XXXXXXXX _B XXXXXXXX _B
007C2A _H				
007C2B _H				
007C2C _H	ID register 3	IDR3	R/W	XXXXXXXX _B XXXXXXXX _B
007C2D _H				XXXXXXXX _B XXXXXXXX _B
007C2E _H				
007C2F _H				
007C30 _H	ID register 4	IDR4	R/W	XXXXXXXX _B XXXXXXXX _B
007C31 _H				XXXXXXXX _B XXXXXXXX _B
007C32 _H				
007C33 _H				
007C34 _H	ID register 5	IDR5	R/W	XXXXXXXX _B XXXXXXXX _B
007C35 _H				XXXXXXXX _B XXXXXXXX _B
007C36 _H				
007C37 _H				
007C38 _H	ID register 6	IDR6	R/W	XXXXXXXX _B XXXXXXXX _B
007C39 _H				XXXXXXXX _B XXXXXXXX _B
007C3A _H				
007C3B _H				
007C3C _H	ID register 7	IDR7	R/W	XXXXXXXX _B XXXXXXXX _B
007C3D _H				XXXXXXXX _B XXXXXXXX _B
007C3E _H				
007C3F _H				
007C40 _H	ID register 8	IDR8	R/W	XXXXXXXX _B XXXXXXXX _B
007C41 _H				XXXXXXXX _B XXXXXXXX _B
007C42 _H				
007C43 _H				

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C44 _H	ID register 9	IDR9	R/W	XXXXXXXX _B
007C45 _H				XXXXXXXX _B
007C46 _H				XXXXXXXX _B
007C47 _H				XXXXXXXX _B
007C48 _H	ID register 10	IDR10	R/W	XXXXXXXX _B
007C49 _H				XXXXXXXX _B
007C4A _H				XXXXXXXX _B
007C4B _H				XXXXXXXX _B
007C4C _H	ID register 11	IDR11	R/W	XXXXXXXX _B
007C4D _H				XXXXXXXX _B
007C4E _H				XXXXXXXX _B
007C4F _H				XXXXXXXX _B
007C50 _H	ID register 12	IDR12	R/W	XXXXXXXX _B
007C51 _H				XXXXXXXX _B
007C52 _H				XXXXXXXX _B
007C53 _H				XXXXXXXX _B
007C54 _H	ID register 13	IDR13	R/W	XXXXXXXX _B
007C55 _H				XXXXXXXX _B
007C56 _H				XXXXXXXX _B
007C57 _H				XXXXXXXX _B
007C58 _H	ID register 14	IDR14	R/W	XXXXXXXX _B
007C59 _H				XXXXXXXX _B
007C5A _H				XXXXXXXX _B
007C5B _H				XXXXXXXX _B
007C5C _H	ID register 15	IDR15	R/W	XXXXXXXX _B
007C5D _H				XXXXXXXX _B
007C5E _H				XXXXXXXX _B
007C5F _H				XXXXXXXX _B

List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C60 _H	DLC register 0	DLCR0	R/W	XXXXXXXX _B
007C61 _H				
007C62 _H	DLC register 1	DLCR1	R/W	XXXXXXXX _B
007C63 _H				
007C64 _H	DLC register 2	DLCR2	R/W	XXXXXXXX _B
007C65 _H				
007C66 _H	DLC register 3	DLCR3	R/W	XXXXXXXX _B
007C67 _H				
007C68 _H	DLC register 4	DLCR4	R/W	XXXXXXXX _B
007C69 _H				
007C6A _H	DLC register 5	DLCR5	R/W	XXXXXXXX _B
007C6B _H				
007C6C _H	DLC register 6	DLCR6	R/W	XXXXXXXX _B
007C6D _H				
007C6E _H	DLC register 7	DLCR7	R/W	XXXXXXXX _B
007C6F _H				
007C70 _H	DLC register 8	DLCR8	R/W	XXXXXXXX _B
007C71 _H				
007C72 _H	DLC register 9	DLCR9	R/W	XXXXXXXX _B
007C73 _H				
007C74 _H	DLC register 10	DLCR10	R/W	XXXXXXXX _B
007C75 _H				
007C76 _H	DLC register 11	DLCR11	R/W	XXXXXXXX _B
007C77 _H				
007C78 _H	DLC register 12	DLCR12	R/W	XXXXXXXX _B
007C79 _H				
007C7A _H	DLC register 13	DLCR13	R/W	XXXXXXXX _B
007C7B _H				
007C7C _H	DLC register 14	DLCR14	R/W	XXXXXXXX _B
007C7D _H				
007C7E _H	DLC register 15	DLCR15	R/W	XXXXXXXX _B
007C7F _H				
007C80 _H to 007C87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Initial Value
CAN1				
007C88 _H to 007C8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
007C90 _H to 007C97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
007C98 _H to 007C9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
007CA0 _H to 007CA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
007CA8 _H to 007CAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
007CB0 _H to 007CB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
007CB8 _H to 007CBF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
007CC0 _H to 007CC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
007CC8 _H to 007CCF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
007CD0 _H to 007CD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
007CD8 _H to 007CDF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
007CE0 _H to 007CE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
007CE8 _H to 007CEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
007CF0 _H to 007CF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
007CF8 _H to 007CFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

14. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt cause	EI ² OS corresponding	DMA ch number	Interrupt vector		Interrupt control register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC _H	—	—
INT9 instruction	N	—	#09	FFFFD8 _H	—	—
Exception	N	—	#10	FFFFD4 _H	—	—
Reserved	N	—	#11	FFFFD0 _H	ICR00	0000B0 _H
Reserved	N	—	#12	FFFFCC _H		
CAN 1 RX / Input Capture 6	Y1	—	#13	FFFFC8 _H	ICR01	0000B1 _H
CAN 1 TX/NS / Input Capture 7	Y1	—	#14	FFFFC4 _H		
I ² C	N	—	#15	FFFFC0 _H	ICR02	0000B2 _H
Reserved	N	—	#16	FFFFBC _H		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8 _H	ICR03	0000B3 _H
16-bit Reload Timer 1	Y1	1	#18	FFFFB4 _H		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0 _H	ICR04	0000B4 _H
16-bit Reload Timer 3	Y1	—	#20	FFFFAC _H		
PPG 4/5	N	—	#21	FFFFA8 _H	ICR05	0000B5 _H
PPG 6/7	N	—	#22	FFFFA4 _H		
PPG 8/9/C/D	N	—	#23	FFFFA0 _H	ICR06	0000B6 _H
PPG A/B/E/F	N	—	#24	FFFF9C _H		
Timebase Timer	N	—	#25	FFFF98 _H	ICR07	0000B7 _H
External Interrupt 8 to 11	Y1	3	#26	FFFF94 _H		
Watch Timer	N	—	#27	FFFF90 _H	ICR08	0000B8 _H
External Interrupt 12 to 15	Y1	4	#28	FFFF8C _H		
A/D Converter	Y1	5	#29	FFFF88 _H	ICR09	0000B9 _H
I/O Timer 0 / I/O Timer 1	N	—	#30	FFFF84 _H		
Input Capture 4/5	Y1	6	#31	FFFF80 _H	ICR10	0000BA _H
Output Compare 4/5	Y1	7	#32	FFFF7C _H		
Input Capture 0/1	Y1	8	#33	FFFF78 _H	ICR11	0000BB _H
Output Compare 6/7	Y1	9	#34	FFFF74 _H		
Reserved	N	10	#35	FFFF70 _H	ICR12	0000BC _H
Reserved	N	11	#36	FFFF6C _H		
UART 3 RX	Y2	12	#37	FFFF68 _H	ICR13	0000BD _H
UART 3 TX	Y1	13	#38	FFFF64 _H		
UART 2 RX	Y2	14	#39	FFFF60 _H	ICR14	0000BE _H
UART 2 TX	Y1	15	#40	FFFF5C _H		
Flash Memory	N	—	#41	FFFF58 _H	ICR15	0000BF _H
Delayed interrupt	N	—	#42	FFFF54 _H		

Y1 : Usable

Y2 : Usable, with EI²OS stop function

N : Unusable

Notes :

- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use EI²OSat a time.
- When either of the two peripheral resources sharing the ICR register specifies EI²OS, the other one cannot use interrupts.

15. Electrical Characteristics

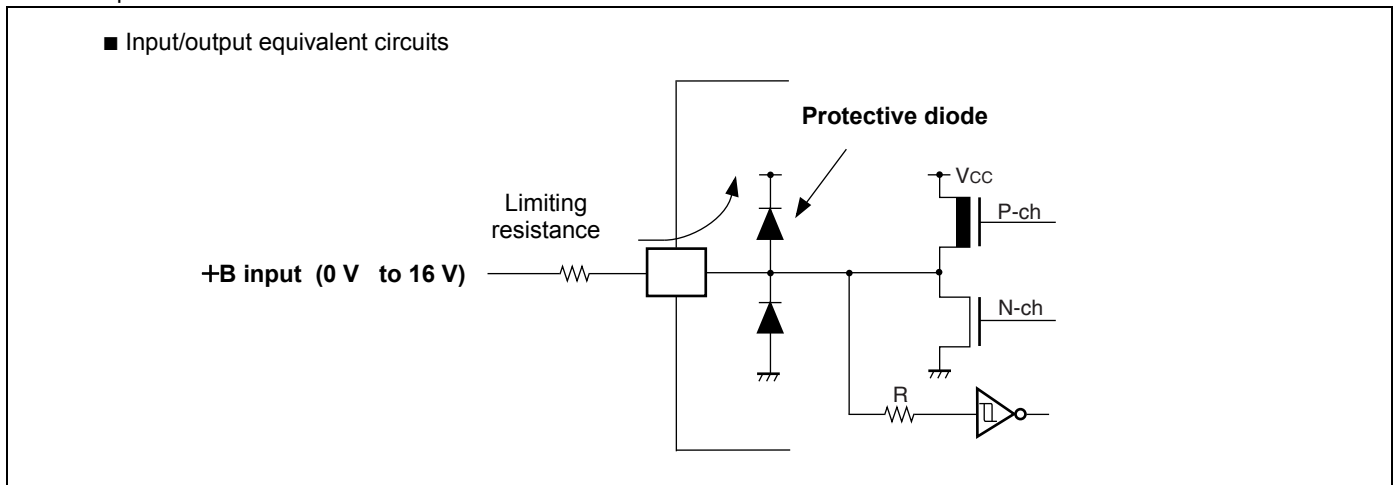
15.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$V_{CC} = AV_{CC}$ *2
	AVRH	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	$AV_{CC} \geq AVRH$ *2
Input voltage*1	V_I	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Output voltage*1	V_O	$V_{SS} - 0.3$	$V_{SS} + 6.0$	V	*3
Maximum Clamp Current	I_{CLAMP}	-4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\sum I_{CLAMP} $	—	40	mA	*5
"L" level maximum output current	I_{OL}	—	15	mA	*4
"L" level average output current	I_{OLAV}	—	4	mA	*4
"L" level maximum overall output current	$\sum I_{OL}$	—	100	mA	*4
"L" level average overall output current	$\sum I_{OLAV}$	—	50	mA	*4
"H" level maximum output current	I_{OH}	—	-15	mA	*4
"H" level average output current	I_{OHAV}	—	-4	mA	*4
"H" level maximum overall output current	$\sum I_{OH}$	—	-100	mA	*4
"H" level average overall output current	$\sum I_{OHAV}$	—	-50	mA	*4
Power consumption	P_D	—	240	mW	MB90F351(S), MB90F352(S) +105 °C < T_A ≤ +125 °C, Normal operation : maximum frequency 16 MHz
		—	320	mW	MB90F351(S), MB90F352(S) -40 °C < T_A ≤ +105 °C, Normal operation : maximum frequency 24 MHz
		—	320	mW	Device other than above
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*6
Storage temperature	T_{STG}	-55	+150	°C	

(Continued)

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- *1: This parameter is based on $V_{SS} = AV_{SS} = 0\text{ V}$
- *2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.
- *3: V_I and V_O should not exceed $V_{CC} + 0.3\text{ V}$. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.
- *4: Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56, P60 to P67
- *5:
 - Applicable to pins: P00 to P07, P10 to P17, P20 to P25, P30 to P37, P40 to P45, P50 to P56 (for evaluation device : P50 to P55) , P60 to P67
 - Use within recommended operating conditions.
 - Use at DC voltage (current)
 - The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
 - Care must be taken not to leave the +B input pin open.
 - Sample recommended circuits:



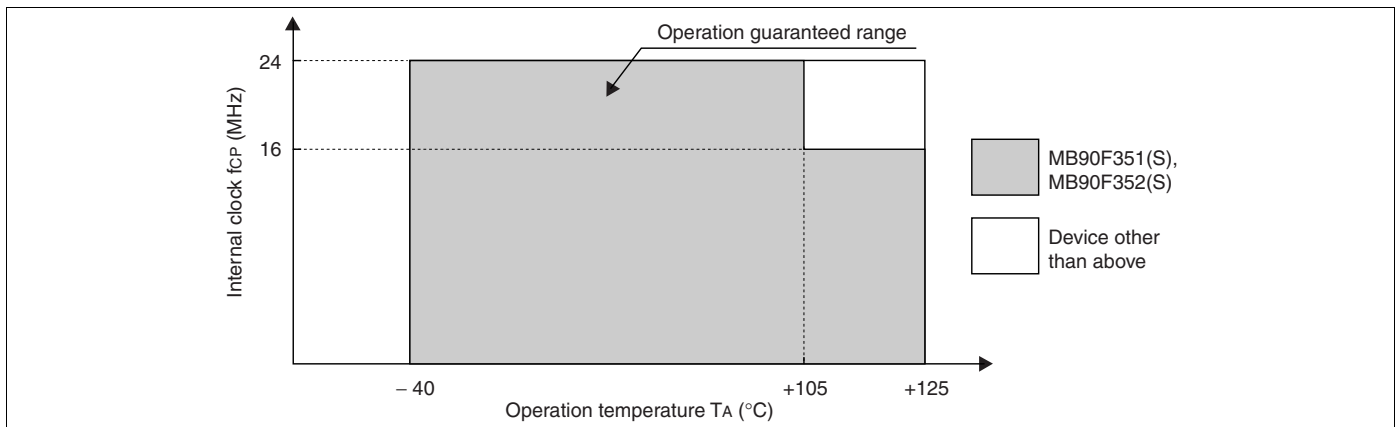
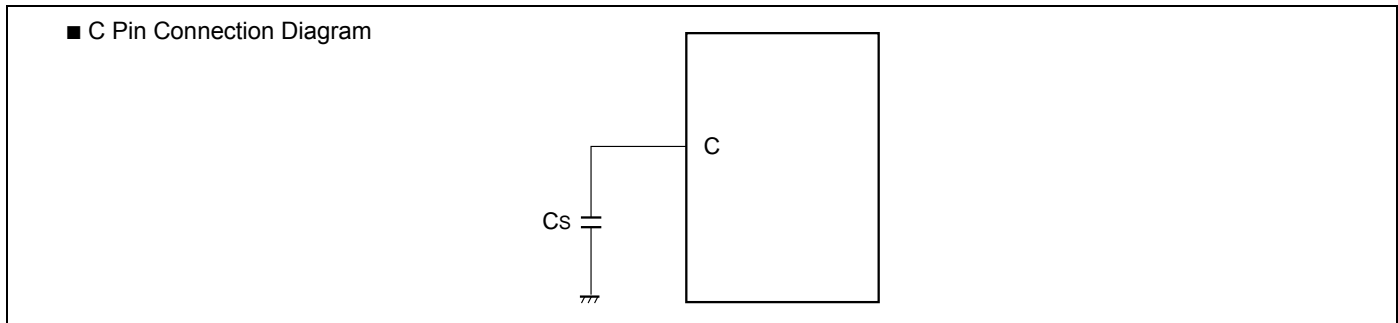
*6 : If used exceeding $T_A = +105\text{ }^\circ\text{C}$, be sure to contact sales for reliability limitations.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

15.2 Recommended Operating Conditions
 $(V_{SS} = AV_{SS} = 0\text{ V})$

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.0	5.0	5.5	V	Under normal operation
		3.5	5.0	5.5	V	Under normal operation, when not using the A/D converter and not Flash programming.
		4.5	5.0	5.5	V	When External bus is used.
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	C_S	0.1	—	1.0	μF	Use a ceramic capacitor or capacitor of better AC characteristics. Bypass capacitor at the V_{CC} pin should be greater than this capacitor.
Operating temperature	T_A	-40	—	+105	$^{\circ}\text{C}$	MB90F352(S) $f_{CP} \leq 24\text{MHz}$
		-40	—	+125	$^{\circ}\text{C}$	*, MB90F352(S) $f_{CP} \leq 16\text{MHz}$, Devices with A-suffix

* : If used exceeding $T_A = +105\text{ }^{\circ}\text{C}$, be sure to contact sales for reliability limitations.



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

15.3 DC Characteristics

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{IHS}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{IHA}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	Pin inputs if AUTOMOTIVE input levels are selected
	V_{IHT}	—	—	2.0	—	$V_{CC} + 0.3$	V	Pin inputs if TTL input levels are selected
	V_{IHS}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{IHI}	—	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{IHR}	—	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	RST input pin (CMOS hysteresis)
	V_{IHM}	—	—	$V_{CC} - 0.3$	—	$V_{CC} + 0.3$	V	MD input pin
Input L voltage (At $V_{CC} = 5\text{ V} \pm 10\%$)	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	Pin inputs if CMOS hysteresis input levels are selected (except P12, P15, P44, P45, P50)
	V_{ILA}	—	—	$V_{SS} - 0.3$	—	$0.5 V_{CC}$	V	Pin inputs if AUTOMOTIVE input levels are selected
	V_{ILT}	—	—	$V_{SS} - 0.3$	—	0.8	V	Pin inputs if TTL input levels are selected
	V_{ILS}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P12, P15, P50 inputs if CMOS input levels are selected
	V_{ILI}	—	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	P44, P45 inputs if CMOS hysteresis input levels are selected
	V_{ILR}	—	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	RST input pin (CMOS hysteresis)
	V_{ILM}	—	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	MD input pin
Output H voltage	V_{OH}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
Output H voltage	V_{OHI}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	

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(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output L voltage	V_{OL}	Normal outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
Output L voltage	V_{OL1}	I ² C current outputs	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 3.0\text{ mA}$	—	—	0.4	V	
Input leak current	I_{IL}	—	$V_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$	-1	—	1	μA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P25, P30 to P37, RST	—	25	50	100	k Ω	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	k Ω	Except Flash memory devices
Power supply current	I_{CC}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At normal operation.	—	48	60	mA	
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At writing FLASH memory.	—	53	65	mA	Flash memory devices
			$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At erasing FLASH memory.	—	58	70	mA	Flash memory devices
	I_{CCS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At Sleep mode.	—	25	35	mA	
	I_{CTS}		$V_{CC} = 5.0\text{ V}$, Internal frequency : 2 MHz, At Main Timer mode	—	0.3	0.8	mA	Devices without "T"-suffix
			—	—	0.4	1.0	mA	Devices with "T"-suffix
	$I_{CTSPLL6}$		$V_{CC} = 5.0\text{ V}$, Internal frequency : 24 MHz, At PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
I_{CCL}	$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During stopping clock monitor function, At sub clock operation $T_A = +25\text{ }^\circ\text{C}$	—	70	140	μA	MB90F351 MB90F352 MB90F351A MB90F352A MB90F356A MB90F357A MB90351A MB90352A MB90356A MB90357A		

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(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CCL}	V _{CC}	V _{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At sub clock operation T _A = +25°C	—	100	200	μA	MB90F356A MB90F357A MB90356A MB90357A
			V _{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T _A = +25°C	—	100	200	μA	MB90F356AS MB90F357AS MB90356AS MB90357AS
			V _{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At sub clock operation T _A = +25°C	—	120	240	μA	MB90F351TA MB90F352TA MB90F356TA MB90F357TA MB90351TA MB90352TA MB90356TA MB90357TA
			V _{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At sub clock operation T _A = +25°C	—	150	300	μA	MB90F356TA MB90F357TA MB90356TA MB90357TA
			V _{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub clock operation T _A = +25°C	—	150	300	μA	MB90F356TAS MB90F357TAS MB90356TAS MB90357TAS
	I _{CCLS}	V _{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At sub sleep T _A = +25°C	—	20	50	μA	MB90F351 MB90F352 MB90F351A MB90F352A MB90F356A MB90F357A MB90351A MB90352A MB90356A MB90357A	

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(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(Device other than above: $T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I _{CCLS}	V _{CC}	V _{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At sub sleep T _A = +25°C	—	60	200	μA	MB90F356A MB90F357A MB90356A MB90357A
			V _{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T _A = +25°C	—	60	200	μA	MB90F356AS MB90F357AS MB90356AS MB90357AS
			V _{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At sub sleep T _A = +25°C	—	70	150	μA	MB90F351TA MB90F352TA MB90F356TA MB90F357TA MB90351TA MB90352TA MB90356TA MB90357TA
			V _{CC} = 5.0 V, Internal frequency: 8 kHz, During operating clock monitor function, At sub sleep T _A = +25°C	—	110	300	μA	MB90F356TA MB90F357TA MB90356TA MB90357TA
	I _{CCT}		V _{CC} = 5.0 V, Internal CR oscillation/ 4 division, At sub sleep T _A = +25°C	—	110	300	μA	MB90F356TAS MB90F357TAS MB90356TAS MB90357TAS
			V _{CC} = 5.0 V, Internal frequency: 8 kHz, During stopping clock monitor function, At watch mode T _A = +25°C	—	10	35	μA	MB90F351 MB90F352 MB90F351A MB90F352A MB90F356A MB90F357A MB90351A MB90352A MB90356A MB90357A

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 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCT}	V_{CC}	$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During operating clock monitor function, At watch mode $T_A = +25\text{ }^\circ\text{C}$	—	25	150	μA	MB90F356A MB90F357A MB90356A MB90357A
			$V_{CC} = 5.0\text{ V}$, Internal CR oscillation/ 4 division, At watch mode $T_A = +25\text{ }^\circ\text{C}$	—	25	150	μA	MB90F356AS MB90F357AS MB90356AS MB90357AS
			$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During stopping clock monitor function, At watch mode $T_A = +25\text{ }^\circ\text{C}$	—	60	140	μA	MB90F351TA MB90F352TA MB90F356TA MB90F357TA MB90351TA MB90352TA MB90356TA MB90357TA
			$V_{CC} = 5.0\text{ V}$, Internal frequency: 8 kHz, During operating clock monitor function, At watch mode $T_A = +25\text{ }^\circ\text{C}$	—	80	250	μA	MB90F356TA MB90F357TA MB90356TA MB90357TA
			$V_{CC} = 5.0\text{ V}$, Internal CR oscillation/ 4 division, At watch mode $T_A = +25\text{ }^\circ\text{C}$	—	80	250	μA	MB90F356TAS MB90F357TAS MB90356TAS MB90357TAS
	I_{CCH}		$V_{CC} = 5.0\text{ V}$, At Stop mode, $T_A = +25\text{ }^\circ\text{C}$	—	7	25	μA	Devices without "T"-suffix
				—	60	130	μA	Devices with "T"-suffix
Input capacity	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, V_{CC} , V_{SS} ,	—	—	5	15	pF	

15.4 AC Characteristics
15.4.1 Clock Timing

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$

 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	16	MHz	1/2 (at PLL stop) When using an oscillation circuit
			4	—	16	MHz	1 multiplied PLL When using an oscillation circuit
			4	—	12	MHz	2 multiplied PLL When using an oscillation circuit
			4	—	8	MHz	3 multiplied PLL When using an oscillation circuit
			4	—	6	MHz	4 multiplied PLL When using an oscillation circuit
			—	—	4	MHz	6 multiplied PLL When using an oscillation circuit
		X0	3	—	24	MHz	1/2 (at PLL stop), When using an external clock
			4	—	24	MHz	1 multiplied PLL When using an external clock
			4	—	12	MHz	2 multiplied PLL When using an external clock
			4	—	8	MHz	3 multiplied PLL When using an external clock
			4	—	6	MHz	4 multiplied PLL When using an external clock
			—	—	4	MHz	6 multiplied PLL When using an external clock
	f_{CL}	X0A, X1A	—	32.768	100	kHz	
Clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using an oscillation circuit
		X0	41.67	—	333	ns	When using an external clock
	t_{CYLL}	X0A, X1A	10	30.5	—	μs	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30% to 70%.
	P_{WHL}, P_{WLL}	X0A	5	15.2	—	μs	
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using an external clock

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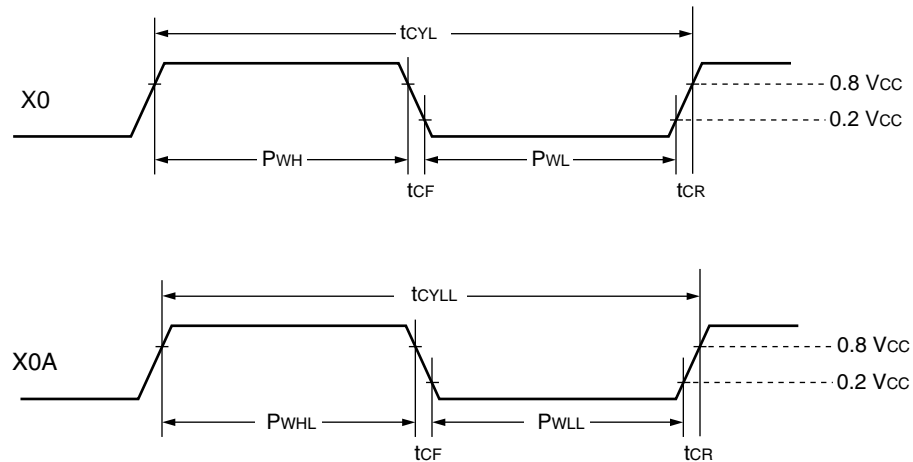
(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

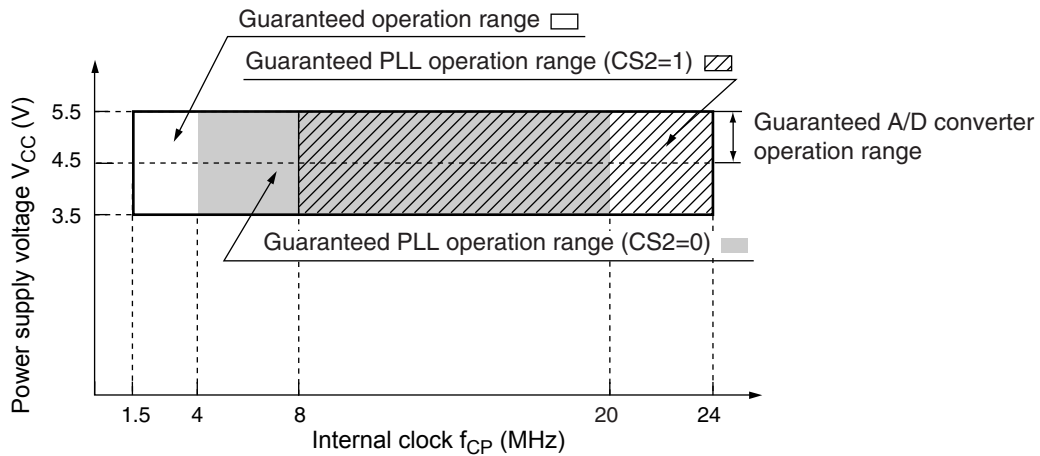
(Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Internal operating clock frequency (machine clock)	f_{CP}	—	1.5	—	24	MHz	MB90F352/(S), MB90F351/(S) When using main clock ($T_A \leq +105\text{ }^\circ\text{C}$)
					16		MB90F352/(S), MB90F351/(S) When using main clock ($T_A \leq +125\text{ }^\circ\text{C}$)
			1.5	—	24	MHz	Device other than above, When using main clock
	f_{CPL}	—	—	8.192	50	kHz	When using sub clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	41.67	—	666	ns	MB90F352/(S), MB90F351/(S) When using main clock ($T_A \leq +105\text{ }^\circ\text{C}$)
			62.5				MB90F352/(S), MB90F351/(S) When using main clock ($T_A \leq +125\text{ }^\circ\text{C}$)
			41.67	—	666	ns	Device other than above, When using main clock
	t_{CPL}	—	20	122.1	—	μs	When using sub clock

■ Clock Timing

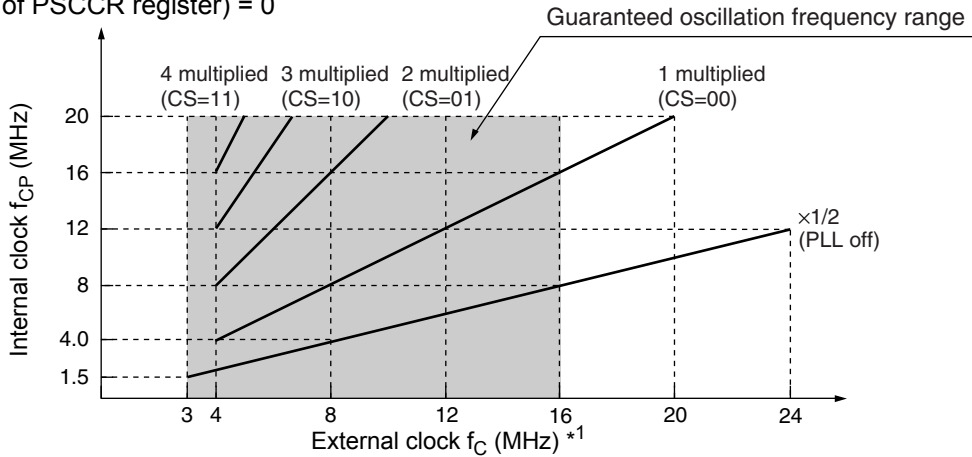


■ PLL guaranteed operation range

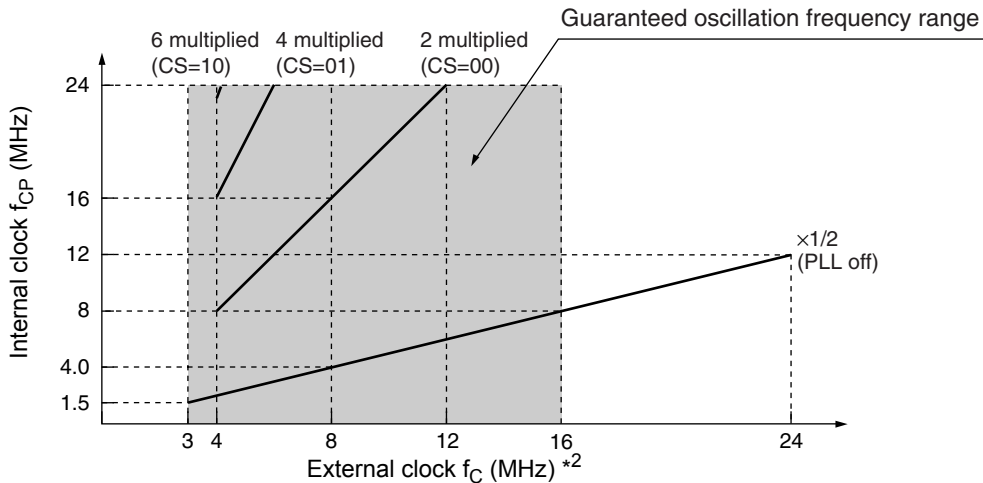


Guaranteed operation range of MB90350 series

CS2(bit0 of PSCCR register) = 0



CS2(bit0 of PSCCR register) = 1



*1 : Guaranteed 1 multiplied PLL operation range is 4.0 MHz to 20 MHz.

*2 : When using crystal oscillator or ceramic oscillator, the maximum clock frequency is 16 MHz.

External clock frequency and internal operation clock frequency

15.4.2 Reset Standby Input

(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

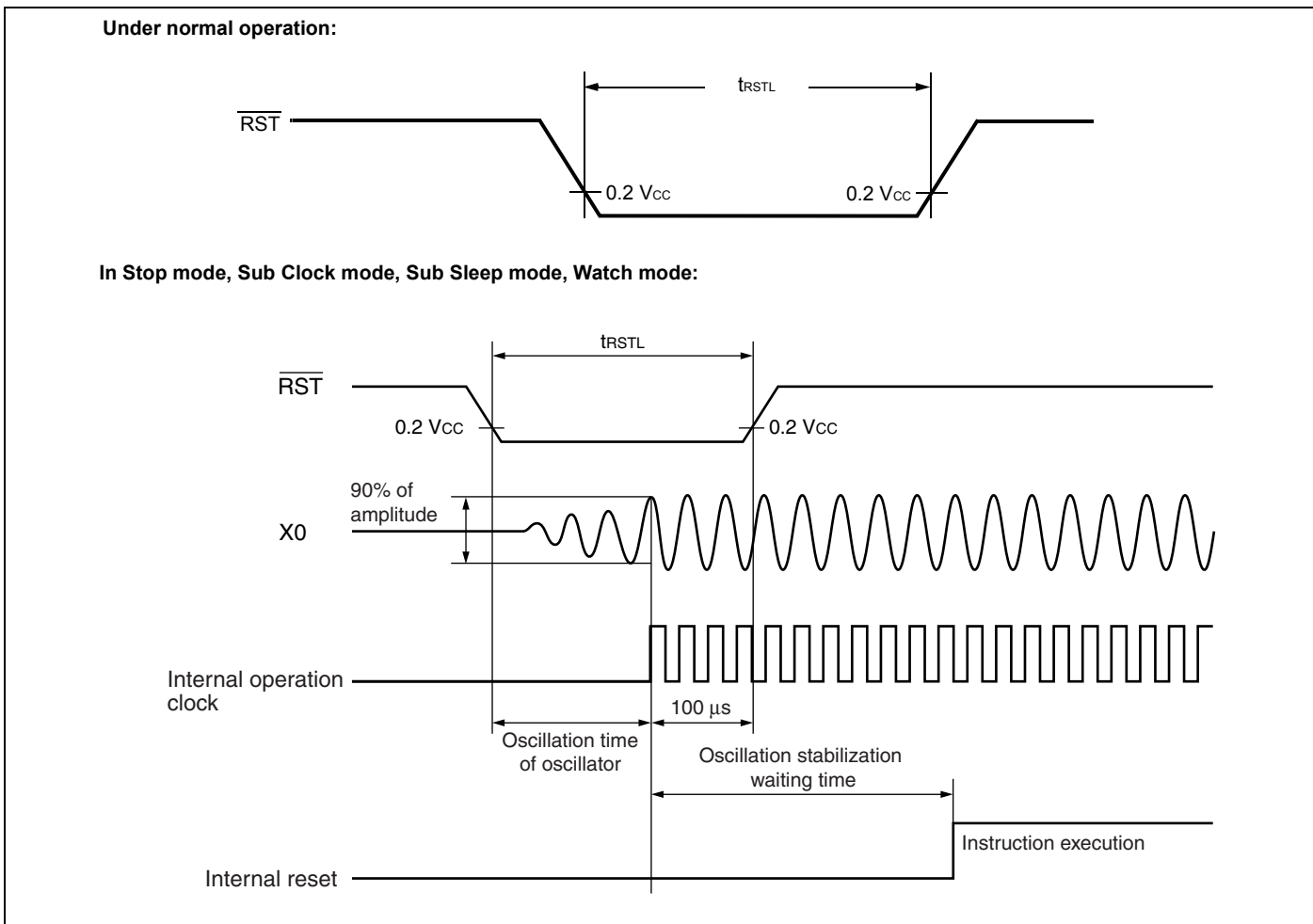
(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value		Unit	Remarks	
			Min	Max			
Reset input time	t_{RSTL}	\overline{RST}	500	—	ns	Under normal operation	
			Oscillation time of oscillator* + 100 μs		—	μs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
			100	—	μs	In Main timer mode and PLL timer mode	

* : Oscillation time of oscillator is the time that the amplitude reaches 90%.

In the crystal oscillator, the oscillation time is between several ms to tens of ms. In FAR / ceramic oscillators, the oscillation time is between hundreds of μs to several ms. With an external clock, the oscillation time is 0 ms.



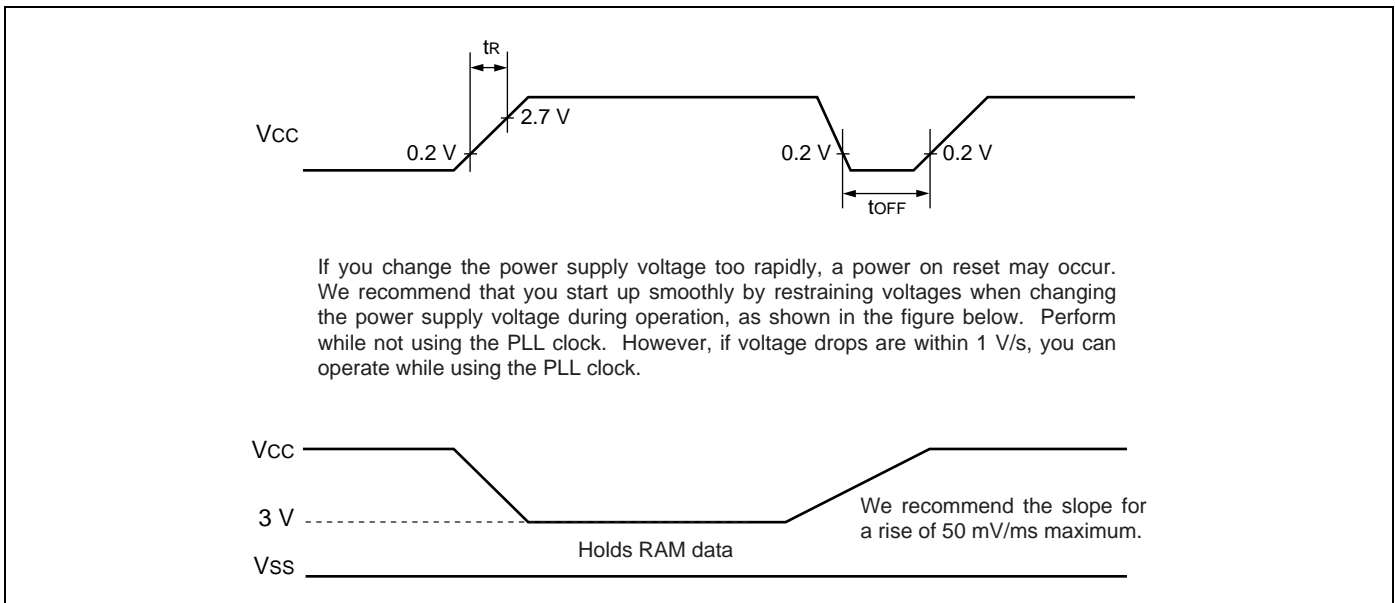
15.4.3 Power On Reset

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

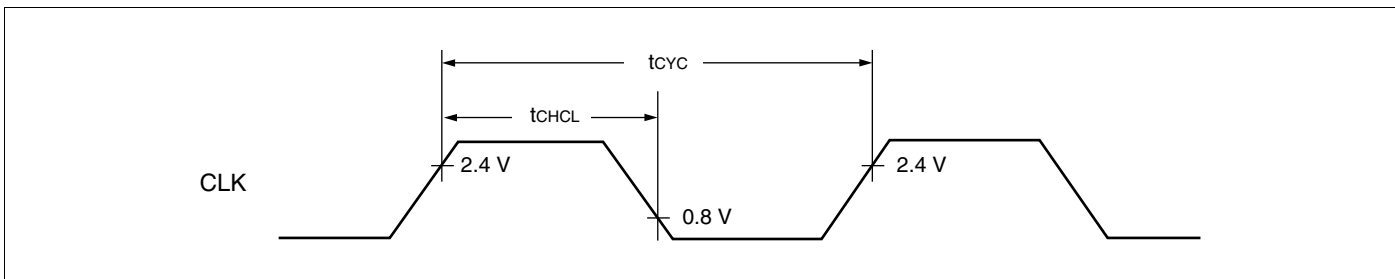
 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}	—	1	—	ms	Due to repetitive operation


15.4.4 Clock Output Timing

 ($T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	62.5	—	ns	$f_{CP} = 16\text{ MHz}$
				41.67	—	ns	$f_{CP} = 24\text{ MHz}$
CLK $\uparrow \rightarrow$ CLK \downarrow	t_{CHCL}	CLK	—	20	—	ns	$f_{CP} = 16\text{ MHz}$
				13	—	ns	$f_{CP} = 24\text{ MHz}$

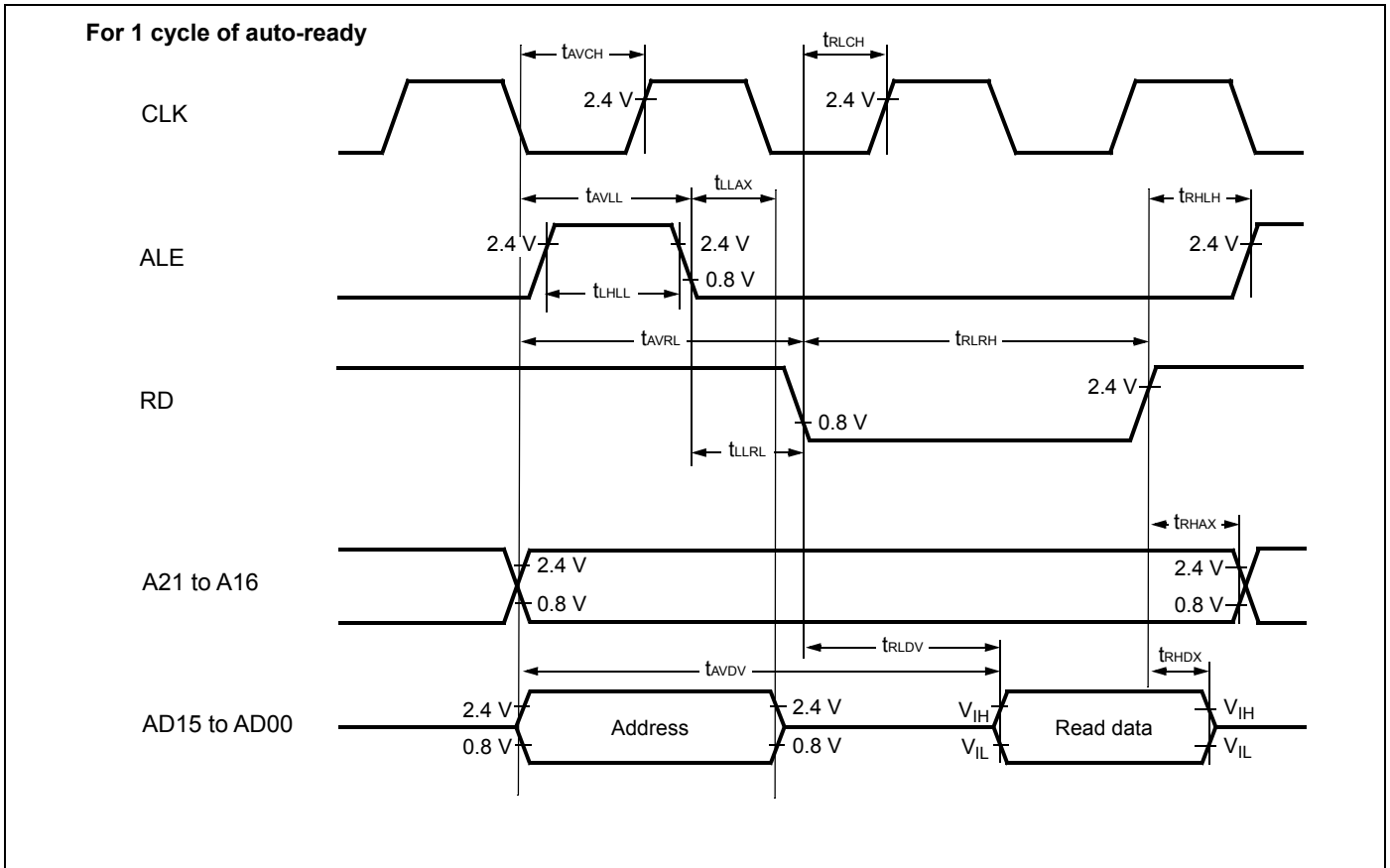


15.4.5 Bus Timing (Read)

 ($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	—	$t_{CP}/2 - 10$	—	ns	
Valid address \rightarrow ALE \downarrow time	t_{AVLL}	ALE, A21 to A16, AD15 to AD00		$t_{CP}/2 - 20$	—	ns	
ALE \downarrow \rightarrow Address valid time	t_{LLAX}	ALE, AD15 to AD00		$t_{CP}/2 - 15$	—	ns	
Valid address \rightarrow \overline{RD} \downarrow time	t_{AVRL}	A21 to A16, AD15 to AD00, RD		$t_{CP} - 15$	—	ns	
Valid address \rightarrow Valid data input	t_{AVDV}	A21 to A16, AD15 to AD00		—	$5 t_{CP}/2 - 60$	ns	
RD pulse width	t_{RLRH}	RD		$(n^*+3/2) t_{CP} - 20$	—	ns	
\overline{RD} \downarrow \rightarrow Valid data input	t_{RLDV}	RD, AD15 to AD00		—	$(n^*+3/2) t_{CP} - 50$	ns	
\overline{RD} \uparrow \rightarrow Data hold time	t_{RHDX}	RD, AD15 to AD00		0	—	ns	
RD \uparrow \rightarrow ALE \uparrow time	t_{RHLL}	RD, ALE		$t_{CP}/2 - 15$	—	ns	
RD \uparrow \rightarrow Address valid time	t_{RHAX}	RD, A21 to A16		$t_{CP}/2 - 10$	—	ns	
Valid address \rightarrow CLK \uparrow time	t_{AVCH}	A21 to A16, AD15 to AD00, CLK		$t_{CP}/2 - 16$	—	ns	
RD \downarrow \rightarrow CLK \uparrow time	t_{RLCH}	RD, CLK		$t_{CP}/2 - 15$	—	ns	
ALE \downarrow \rightarrow RD \downarrow time	t_{LLRL}	ALE, RD		$t_{CP}/2 - 15$	—	ns	

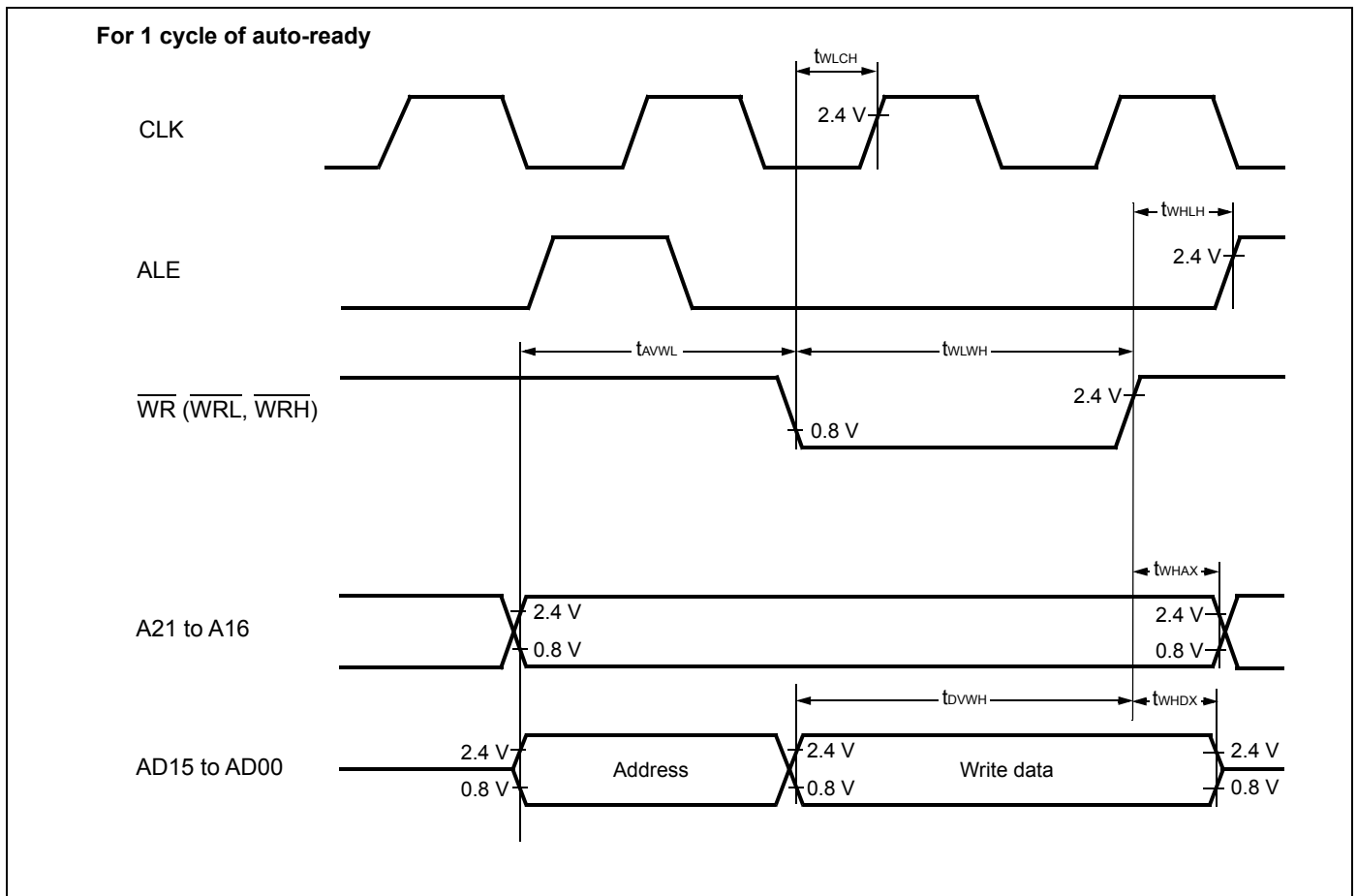
* : n: number of ready cycles



15.4.6 Bus Timing (Write)
 $(T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}, V_{CC} = 5.0\text{ V} \pm 10\%, V_{SS} = 0.0\text{ V}, f_{CP} \leq 24\text{ MHz})$

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Valid address $\rightarrow \overline{WR} \downarrow$ time	t_{AVWL}	A21 to A16, AD15 to AD00, \overline{WR}	—	$t_{CP} - 15$	—	ns	
\overline{WR} pulse width	t_{WLWH}	\overline{WR}		$(n^* + 3/2)t_{CP} - 20$	—	ns	
Valid data output $\rightarrow \overline{WR} \uparrow$ time	t_{DVWH}	AD15 to AD00, \overline{WR}		$(n^* + 3/2)t_{CP} - 20$	—	ns	
$\overline{WR} \uparrow \rightarrow$ Data hold time	t_{WHDX}	AD15 to AD00, \overline{WR}		15	—	ns	
$\overline{WR} \uparrow \rightarrow$ Address valid time	t_{WHAX}	A21 to A16, \overline{WR}		$t_{CP}/2 - 10$	—	ns	
$\overline{WR} \uparrow \rightarrow$ ALE \uparrow time	t_{WHLH}	\overline{WR} , ALE		$t_{CP}/2 - 15$	—	ns	
$\overline{WR} \downarrow \rightarrow$ CLK \uparrow time	t_{WLCH}	\overline{WR} , CLK		$t_{CP}/2 - 15$	—	ns	

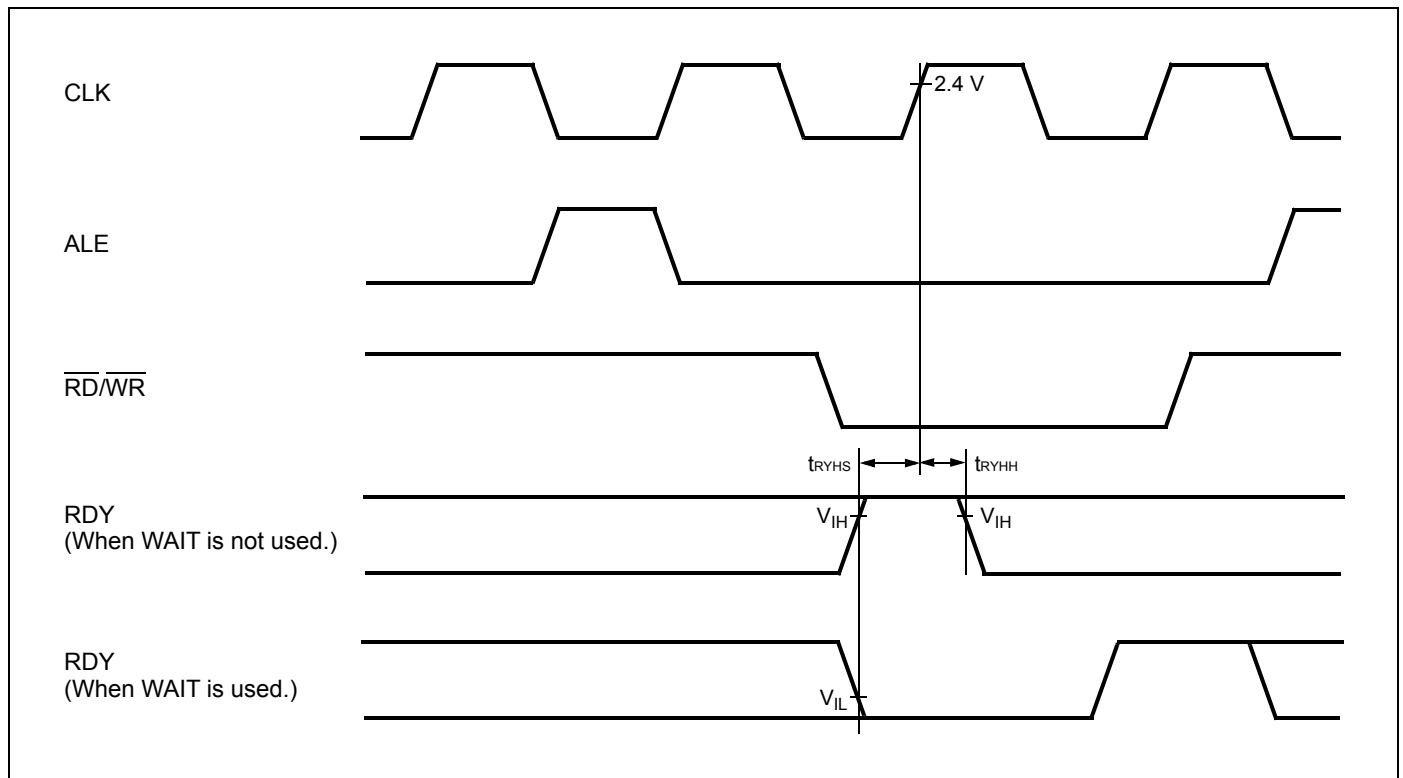
* : n: Number of ready cycles



15.4.7 Ready Input Timing

 (T_A = -40°C to +105°C, V_{CC} = 5.0 V ± 10 %, V_{SS} = 0.0 V, f_{CP} ≤ 24 MHz)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
RDY set-up time	t _{RYHS}	RDY	—	45	—	ns	f _{CP} = 16 MHz
				32	—	ns	f _{CP} = 24 MHz
RDY hold time	t _{RYHH}	RDY	—	0	—	ns	

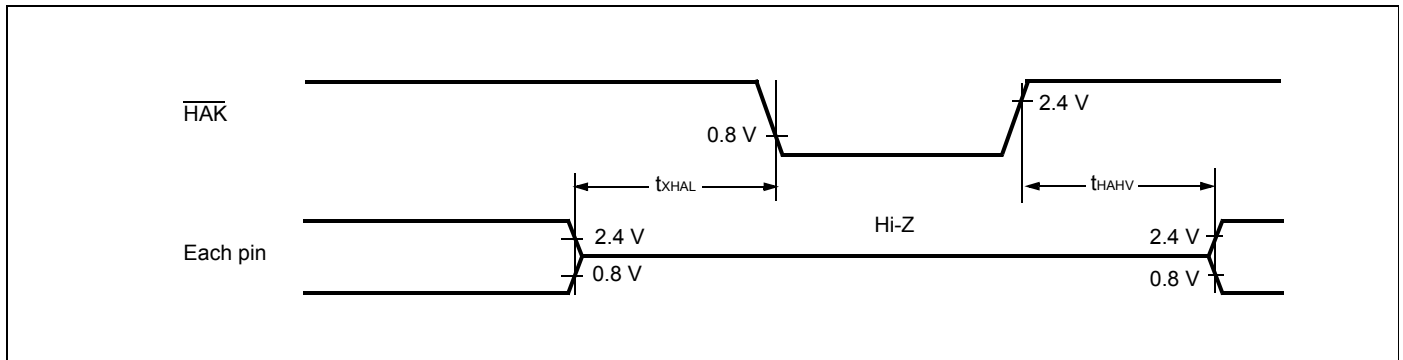
Note : If the RDY set-up time is insufficient, use the auto-ready function.


15.4.8 Hold Timing

($T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $f_{CP} \leq 24\text{ MHz}$)

Parameter	Symbol	Pin	Condition	Value		Units	Remarks
				Min	Max		
Pin floating \rightarrow $\overline{\text{HAK}}$ \downarrow time	$t_{X\text{HAL}}$	HAK	—	30	t_{CP}	ns	
$\overline{\text{HAK}}$ \uparrow time \rightarrow Pin valid time	t_{HAHV}	HAK		t_{CP}	$2 t_{CP}$	ns	

Note : There is more than 1 machine cycle from when HRQ pin reads in until the $\overline{\text{HAK}}$ is changed.



15.4.9 UART 2/3

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

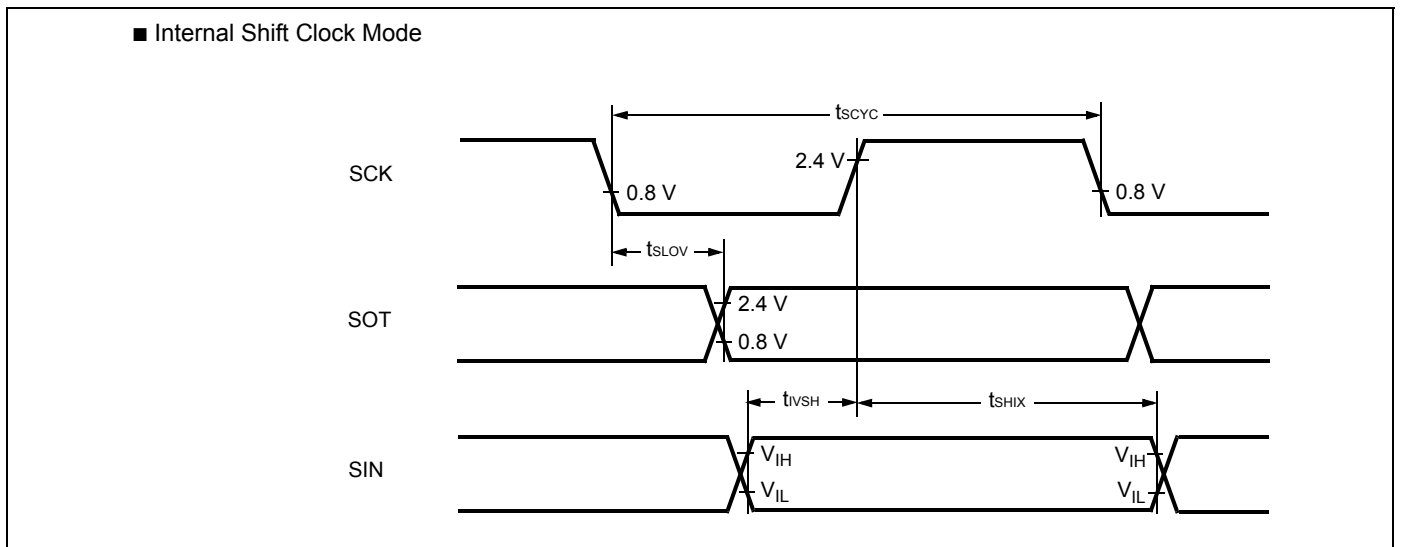
 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

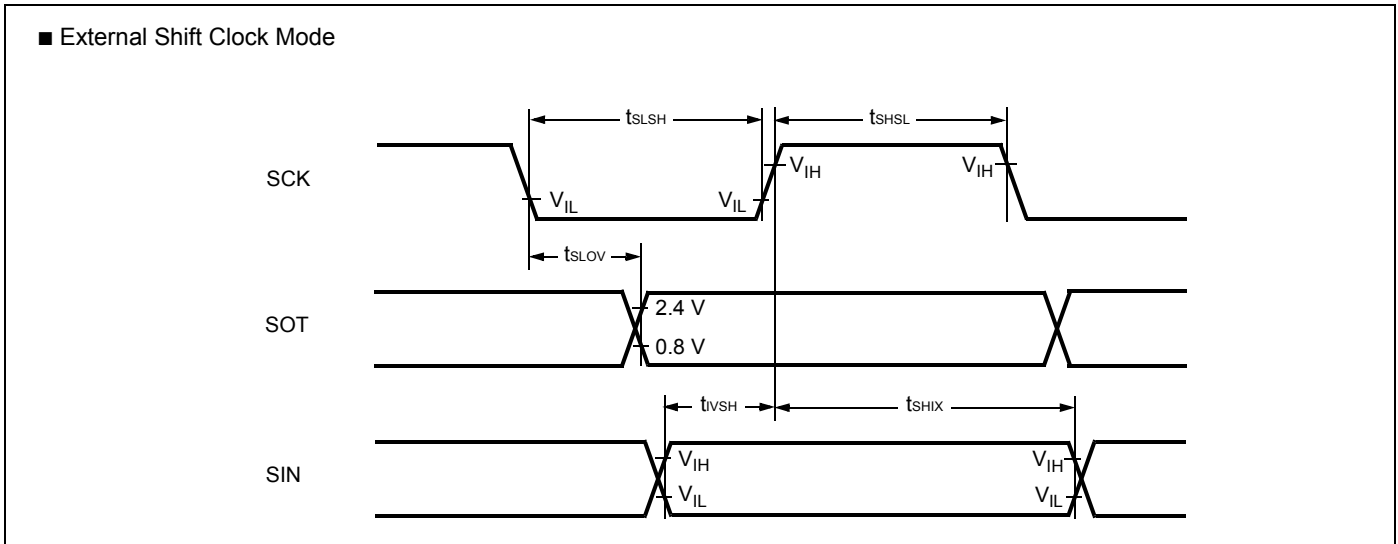
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2, SCK3	Internal shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$8 t_{CP}^*$	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK2, SCK3, SOT2, SOT3		-80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK2, SCK3, SIN2, SIN3		100	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK2, SCK3, SIN2, SIN3		60	—	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK2, SCK3	External shift clock mode output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$	$4 t_{CP}$	—	ns	
Serial clock "L" pulse width	t_{LSLH}	SCK2, SCK3		$4 t_{CP}$	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK2, SCK3, SOT2, SOT3		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK2, SCK3, SIN2, SIN3		60	—	ns	
SCK ↑ → Valid SIN hold time	t_{SHIX}	SCK2, SCK3, SIN2, SIN3		60	—	ns	

 * : Refer to " (1) Clock timing" rating for t_{CP} (internal operating clock cycle time).

Notes :

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.





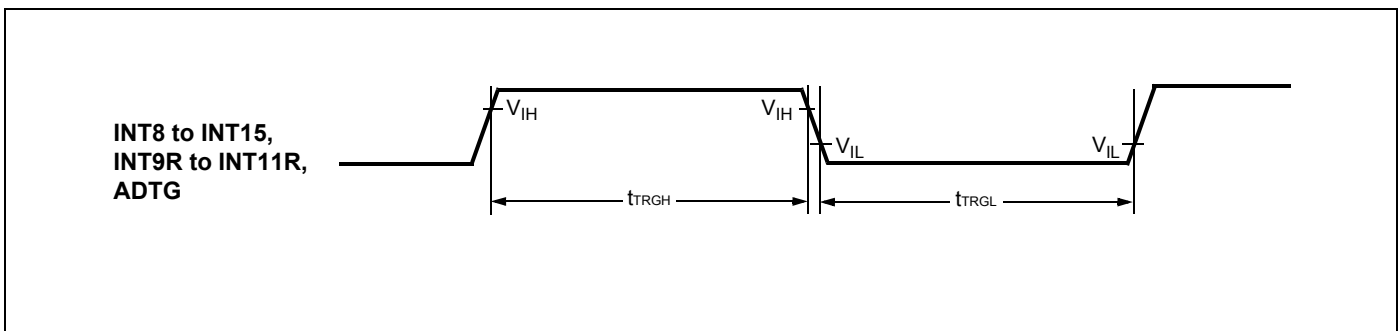
15.4.10 Trigger Input Timing

(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

(Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT8 to INT15, INT9R to INT11R, ADTG	—	$5 t_{CP}$	—	ns	



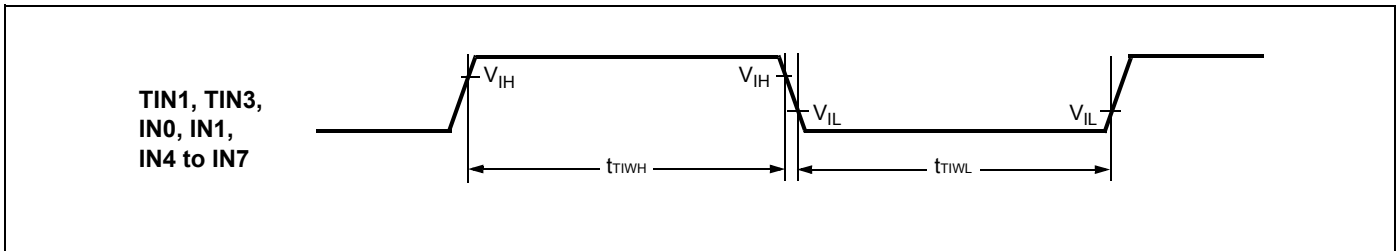
15.4.11 Timer Related Resource Input Timing

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN1, TIN3, IN0, IN1, IN4 to IN7	—	4 t_{CP}	—	ns	
	t_{TIWL}						

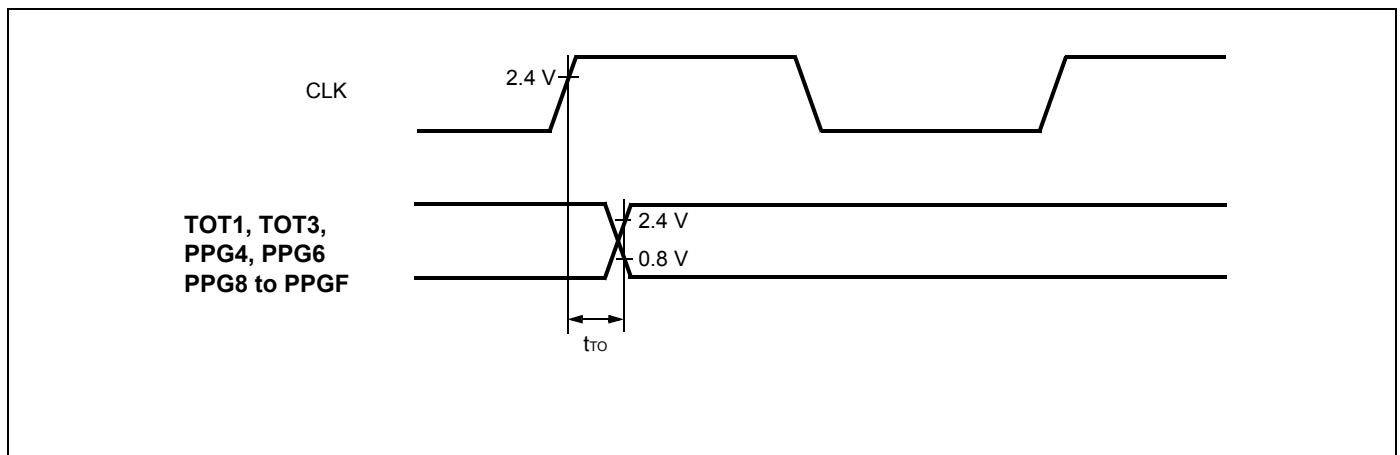

15.4.12 Timer Related Resource Output Timing

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min	Max		
CLK \uparrow \rightarrow T_{OUT} change time	t_{TO}	TOT1, TOT3, PPG4, PPG6, PPG8 to PPGF	—	30	—	ns	



15.4.13 I²C Timing

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = AV_{SS} = 0\text{ V}$)

Parameter	Symbol	Condition	Standard-mode		Fast-mode ^{*4}		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	$R = 1.7\text{ k}\Omega$ $C = 50\text{ pF}^{*1}$	0	100	0	400	kHz
Hold time for (repeated) START condition SDA \downarrow →SCL \downarrow	t_{HDSTA}		4.0	—	0.6	—	μs
“L” width of the SCL clock	t_{LOW}		4.7	—	1.3	—	μs
“H” width of the SCL clock	t_{HIGH}		4.0	—	0.6	—	μs
Set-up time for a repeated START condition SCL \uparrow →SDA \downarrow	t_{SUSTA}		4.7	—	0.6	—	μs
Data hold time SCL \downarrow →SDA \downarrow	t_{HDDAT}		0	3.45^{*2}	0	0.9^{*3}	μs
Data set-up time SDA \downarrow →SCL \uparrow	t_{SUDAT}		250^{*5}	—	100^{*5}	—	ns
Set-up time for STOP condition SCL \uparrow →SDA \uparrow	t_{SUSTO}		4.0	—	0.6	—	μs
Bus free time between STOP condition and START condition	t_{BUS}		4.7	—	1.3	—	μs

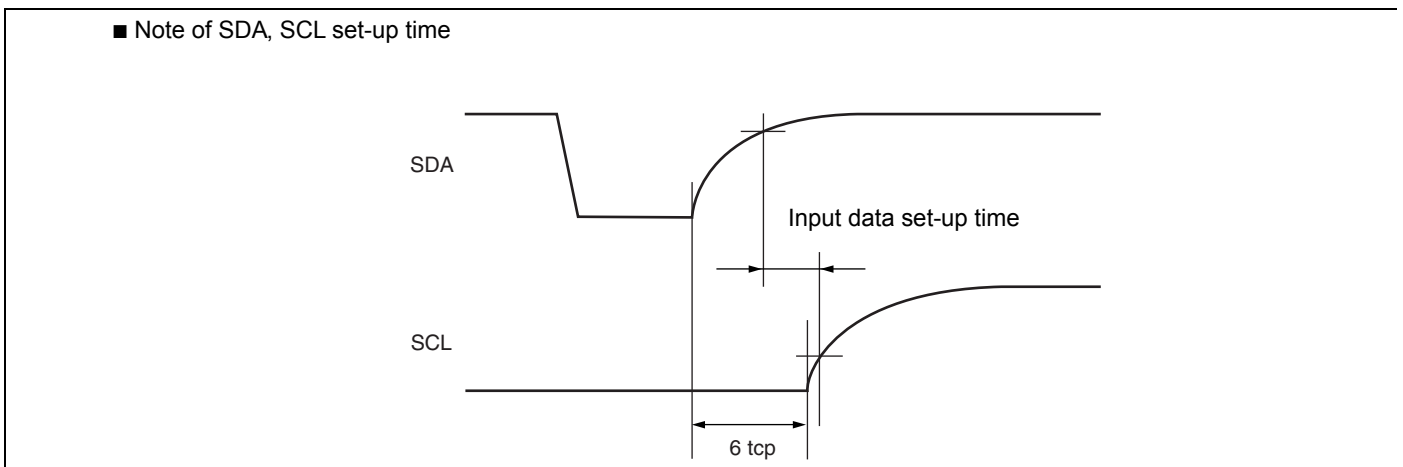
*1 : R,C : Pull-up resistor and load capacitor of the SCL and SDA lines.

*2 : The maximum t_{HDDAT} has only to be met if the device does not stretch the “L” width (t_{LOW}) of the SCL signal.

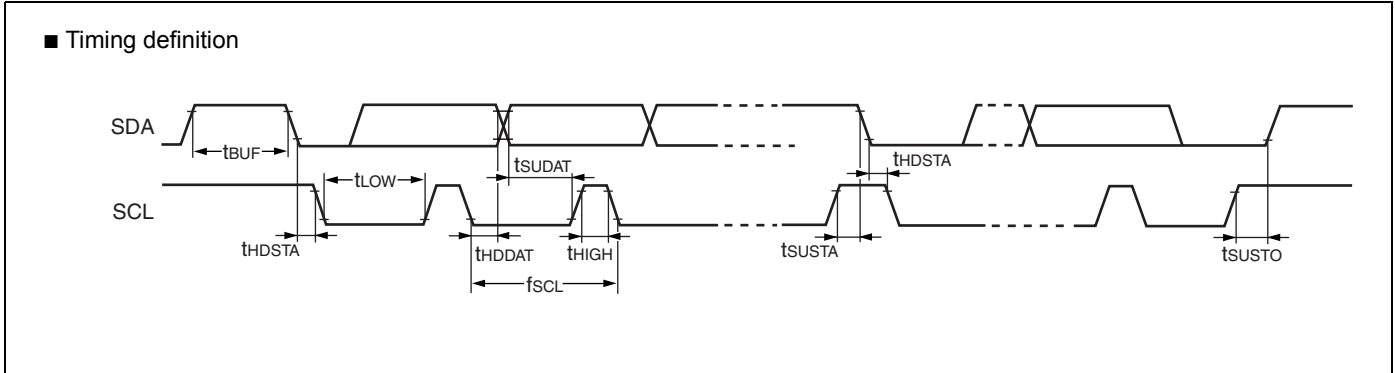
*3 : A Fast-mode I²C -bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SUDAT} \geq 250\text{ ns}$ must then be met.

*4 : For use at over 100 kHz, set the machine clock to at least 6 MHz.

*5 : Refer to “Note of SDA, SCL set-up time”.



Note : The rating of the input data set-up time in the device connected to the bus cannot be satisfied depending on the load capacitance or pull-up resistor.
 Be sure to adjust the pull-up resistor of SDA and SCL if the rating of the input data set-up time cannot be satisfied.



15.5 A/D Converter

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$, $3.0\text{ V} \leq \text{AVRH}$, $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = \text{AV}_{SS} = 0\text{ V}$)

 (MB90F352(S)/MB90F351(S): $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $3.0\text{ V} \leq \text{AVRH}$, $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 16\text{ MHz}$, $V_{SS} = \text{AV}_{SS} = 0\text{ V}$)

 (Device other than above: $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $3.0\text{ V} \leq \text{AVRH}$, $V_{CC} = \text{AV}_{CC} = 5.0\text{ V} \pm 10\%$, $f_{CP} \leq 24\text{ MHz}$, $V_{SS} = \text{AV}_{SS} = 0\text{ V}$)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential nonlinearity error	—	—	—	—	± 1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN14	$\text{AV}_{SS} - 1.5\text{ LSB}$	$\text{AV}_{SS} + 0.5\text{ LSB}$	$\text{AV}_{SS} + 2.5\text{ LSB}$	V	
Full scale reading voltage	V_{FST}	AN0 to AN14	$\text{AVRH} - 3.5\text{ LSB}$	$\text{AVRH} - 1.5\text{ LSB}$	$\text{AVRH} + 0.5\text{ LSB}$	V	
Compare time	—	—	1.0	—	16,500	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			2.0				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Sampling time	—	—	0.5	—	¥	μs	$4.5\text{ V} \leq \text{AV}_{CC} \leq 5.5\text{ V}$
			1.2				$4.0\text{ V} \leq \text{AV}_{CC} < 4.5\text{ V}$
Analog port input current	I_{AIN}	AN0 to AN14	-0.3	—	+0.3	μA	
Analog input voltage range	V_{AIN}	AN0 to AN14	AV_{SS}	—	AVRH	V	
Reference voltage range	—	AVRH	$\text{AV}_{SS} + 2.7$	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage supply current	I_R	AVRH	—	600	900	μA	
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN14	—	—	4	LSB	

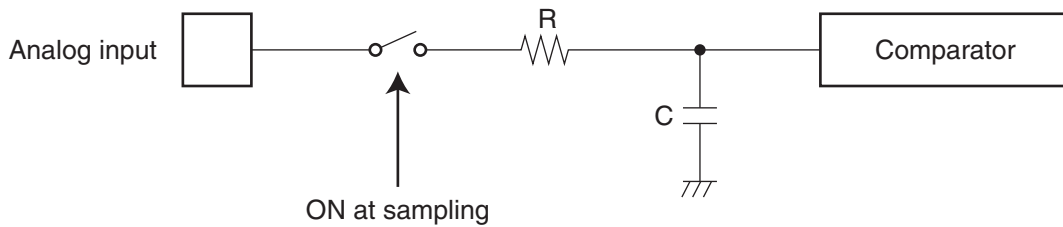
 * : If A/D converter is not operating, a current when CPU is stopped is applicable ($V_{CC} = \text{AV}_{CC} = \text{AVRH} = 5.0\text{ V}$) .

Notes on A/D Converter Section

■ About the external impedance of the analog input and its sampling time

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. Also if the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

· Analog input equivalence circuit



MB90F352(S), MB90F351A(S), MB90F352A(S), MB90F351TA(S), MB90F352TA(S),
 MB90F356A(S), MB90F357A(S), MB90F356TA(S), MB90F357TA(S),

	R	C
$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$	2.0 k Ω (Max)	16.0 pF (Max)
$4.0\text{ V} \leq AV_{CC} \leq 4.5\text{ V}$	8.2 k Ω (Max)	16.0 pF (Max)

MB90V340A-101/102/103/104, MB90351A(S), MB90352A(S), MB90351TA(S), MB90352TA(S),
 MB90356A(S), MB90357A(S), MB90356TA(S), MB90357TA(S),

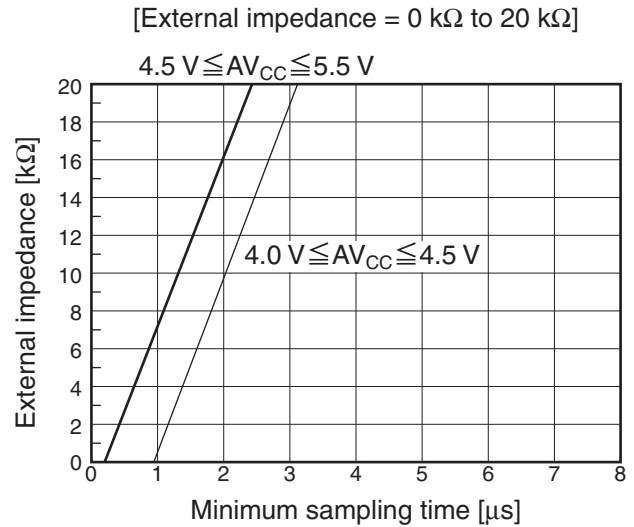
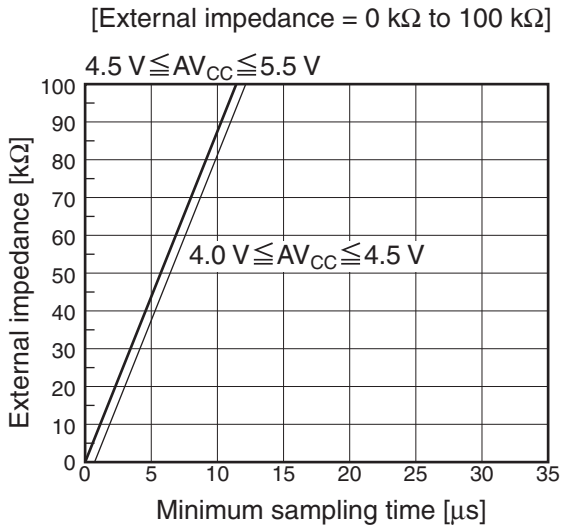
	R	C
$4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$	2.0 k Ω (Max)	14.4 pF (Max)
$4.0\text{ V} \leq AV_{CC} \leq 4.5\text{ V}$	8.2 k Ω (Max)	14.4 pF (Max)

Note : The value is reference value.

Flash memory device

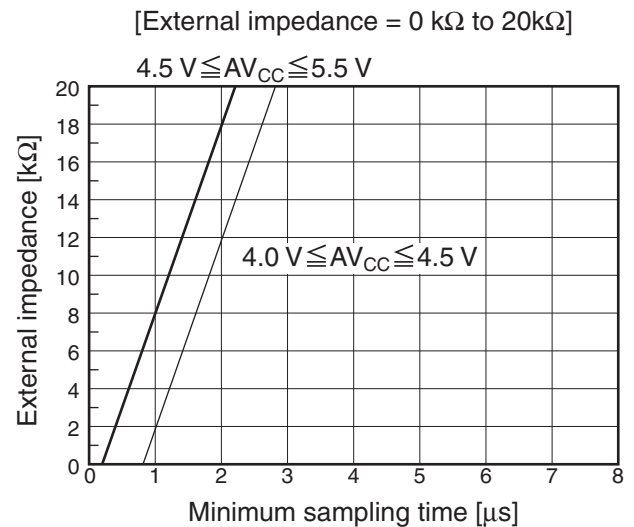
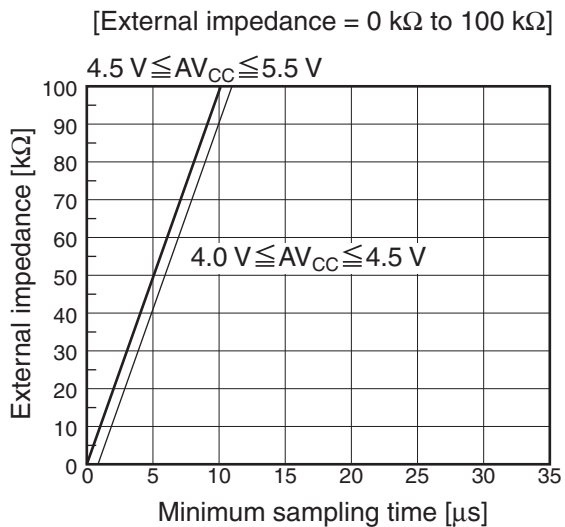
· Relation between External impedance and minimum sampling time

(MB90F352(S), MB90F351A(S), MB90F352A(S), MB90F351TA(S), MB90F352TA(S), MB90F356A(S), MB90F357A(S), MB90F356TA(S), MB90F357TA(S))


MASK ROM device

· Relation between External impedance and minimum sampling time

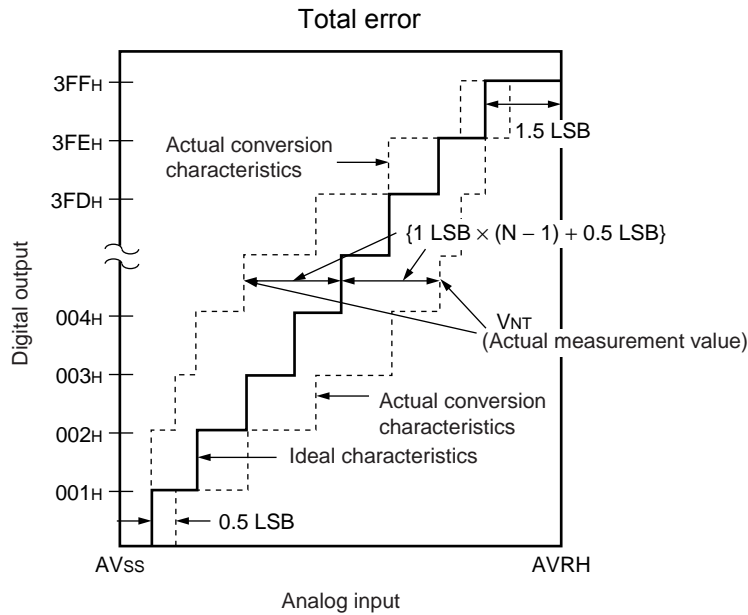
(MB90V340A-101/102/103/104, MB90351A(S), MB90352A(S), MB90351TA(S), MB90352TA(S), MB90356A(S), MB90357A(S), MB90356TA(S), MB90357TA(S))


About the error

Values of relative errors grow larger, as $|AV_{RH} - AV_{SS}|$ becomes smaller.

15.6 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Non linearity error : Deviation between a line across zero-transition line ("00 0000 0000" ← → "00 0000 0001") and full-scale transition line ("11 1111 1110" ← → "11 1111 1111") and actual conversion characteristics.
- Differential linearity error : Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
- Total error : Difference between an actual value and a theoretical value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output "N"} = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB} = (\text{Ideal value}) \frac{AVRH - AV_{SS}}{1024} \quad [\text{V}]$$

N : A/D converter digital output value

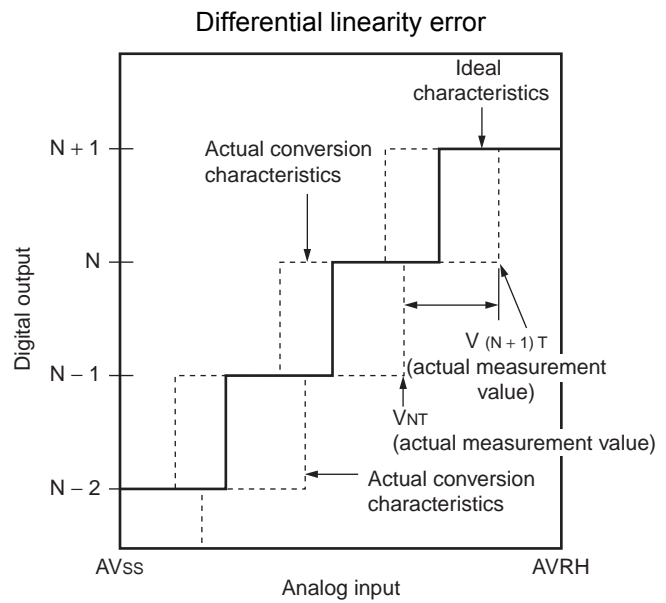
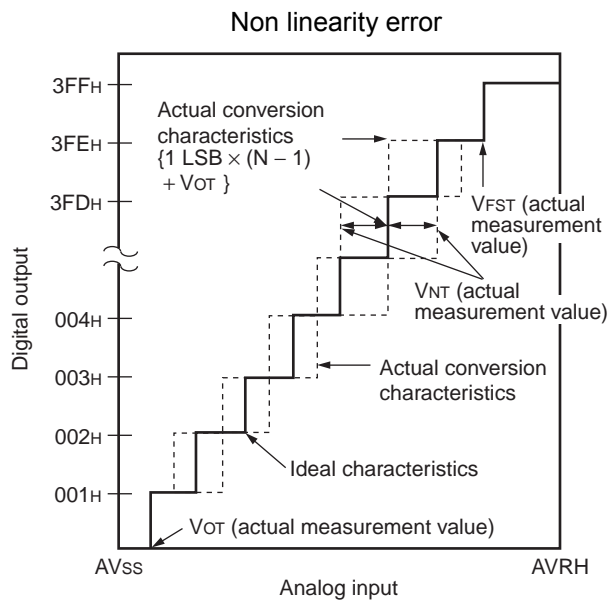
V_{OT} (Ideal value) = $AV_{SS} + 0.5 \text{ LSB}$ [V]

V_{FST} (Ideal value) = $AVRH - 1.5 \text{ LSB}$ [V]

V_{NT} : A voltage at which digital output transits from (N - 1) to N.

(Continued)

(Continued)



$$\text{Non linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ LSB [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”

V_{FST} : Voltage at which digital output transits from “3FE_H” to “3FF_H.”

15.7 Flash Memory Program/Erase Characteristics

Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$	—	1	15	s	Excludes programming prior to erasure
Chip erase time		—	9	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	16	3,600	μs	Except for the overhead time of the system level
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Memory Data Retention Time	Average $T_A = +85\text{ }^\circ\text{C}$	20	—	—	year	*

* : This value comes from the technology qualification.

(Using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

Dual Operation Flash Memory

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 Kbytes sector)	$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 5.0\text{ V}$	—	0.2	0.5	s	Excludes programming prior to erasure
Sector erase time (16 Kbytes sector)		—	0.5	7.5	s	Excludes programming prior to erasure
Chip erase time		—	4.6	—	s	Excludes programming prior to erasure
Word (16-bit width) programming time		—	64	3,600	μs	Except for the overhead time of the system level
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Memory Data Retention Time	Average $T_A = +85\text{ }^\circ\text{C}$	20	—	—	year	*

* : This value comes from the technology qualification.

(Using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C)

16. Ordering Information

Part number	Package	Remarks
MB90F351PMC	64-pin plastic LQFP FPT-64P-M23 12mm, 0.65mm pitch	Flash memory products (64 Kbytes)
MB90F351SPMC		
MB90F352PMC		Flash memory products (128 Kbytes)
MB90F352SPMC		
MB90F351APMC	64-pin plastic LQFP FPT-64P-M23 12mm, 0.65mm pitch	Dual operation Flash memory products (64 Kbytes)
MB90F351ASPMC		
MB90F351TAPMC		
MB90F351TASPMC		
MB90F356APMC		
MB90F356ASPMC		
MB90F356TAPMC		
MB90F356TASPMC		
MB90F352APMC	64-pin plastic LQFP FPT-64P-M23 12mm, 0.65mm pitch	Dual operation Flash memory products (128 Kbytes)
MB90F352ASPMC		
MB90F352TAPMC		
MB90F352TASPMC		
MB90F357APMC		
MB90F357ASPMC		
MB90F357TAPMC		
MB90F357TASPMC		
MB90351APMC	64-pin plastic LQFP FPT-64P-M23 12mm, 0.65mm pitch	MASK ROM products (64 Kbytes)
MB90351ASPMC		
MB90351TAPMC		
MB90351TASPMC		
MB90356APMC		
MB90356ASPMC		
MB90356TAPMC		
MB90356TASPMC		
MB90352APMC	64-pin plastic LQFP FPT-64P-M23 12mm, 0.65mm pitch	MASK ROM products (128 Kbytes)
MB90352ASPMC		
MB90352TAPMC		
MB90352TASPMC		
MB90357APMC		
MB90357ASPMC		
MB90357TAPMC		
MB90357TASPMC		

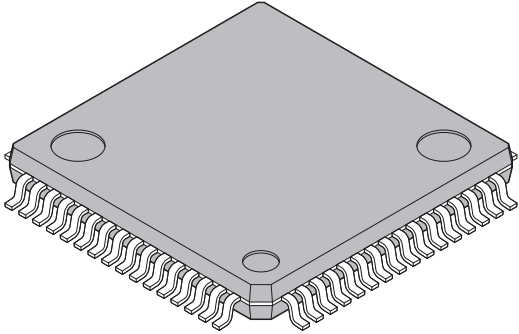
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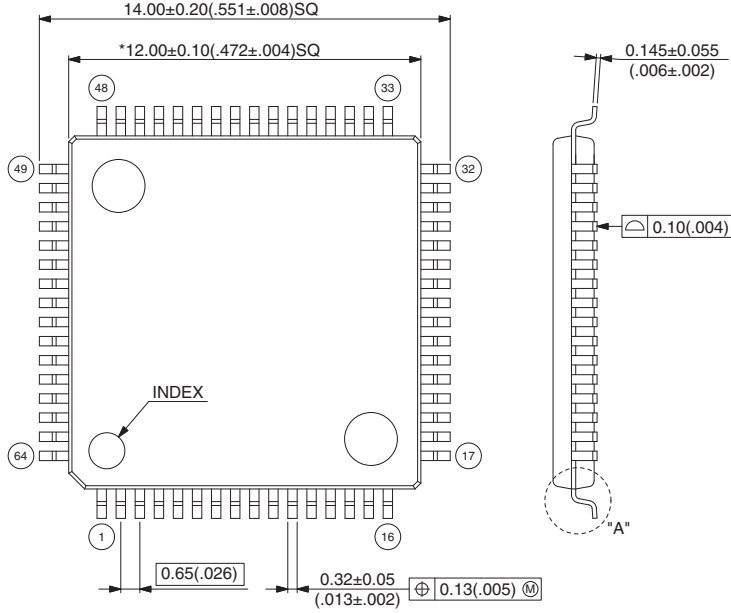
Part number	Package	Remarks
MB90F351APMC1	64-pin plastic LQFP FPT-64P-M24 10 mm , 0.50 mm pitch	Dual operation Flash memory products* (64 Kbytes)
MB90F351ASPMC1		
MB90F351TAPMC1		
MB90F351TASPMC1		
MB90F356APMC1		
MB90F356ASPMC1		
MB90F356TAPMC1		
MB90F356TASPMC1		
MB90F352APMC1	64-pin plastic LQFP FPT-64P-M24 10 mm , 0.50 mm pitch	Dual operation Flash memory products* (128 Kbytes)
MB90F352ASPMC1		
MB90F352TAPMC1		
MB90F352TASPMC1		
MB90F357APMC1		
MB90F357ASPMC1		
MB90F357TAPMC1		
MB90F357TASPMC1		
MB90351APMC1	64-pin plastic LQFP FPT-64P-M24 10 mm , 0.50 mm pitch	MASK ROM products* (64 Kbytes)
MB90351ASPMC1		
MB90351TAPMC1		
MB90351TASPMC1		
MB90356APMC1		
MB90356ASPMC1		
MB90356TAPMC1		
MB90356TASPMC1		
MB90352APMC1	64-pin plastic LQFP FPT-64P-M24 10 mm , 0.50 mm pitch	MASK ROM products* (128 Kbytes)
MB90352ASPMC1		
MB90352TAPMC1		
MB90352TASPMC1		
MB90357APMC1		
MB90357ASPMC1		
MB90357TAPMC1		
MB90357TASPMC1		
MB90V340A-101	299-pin ceramic PGA PGA-299C-A01	Device for evaluation
MB90V340A-102		
MB90V340A-103		
MB90V340A-104		

* : These devices are under development.

17. Package Dimensions

<p style="text-align: center;">64-pin plastic LQFP</p>  <p style="text-align: center;">(FPT-64P-M23)</p>	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
	Code (Reference)	P-LQFP64-12×12-0.65

64-pin plastic LQFP
(FPT-64P-M23)



14.00±0.20(.551±.008)SQ
*12.00±0.10(.472±.004)SQ

INDEX

0.65(.026) 0.32±0.05 (.013±.002) ⊕ 0.13(.005) M

0.145±0.055 (.006±.002)

0.10(.004)

Note 1) * : These dimensions do not include resin protrusion.
 Note 2) Pins width and pins thickness include plating thickness.
 Note 3) Pins width do not include tie bar cutting remainder.

Details of "A" part

1.50^{+0.20}/_{-0.10} (.059^{+0.008}/_{-.004}) (Mounting height)

0.25(.010)

0-8°

0.50±0.20 (.020±.008) 0.10±0.10 (.004±.004) (Stand off)

0.60±0.15 (.024±.006)

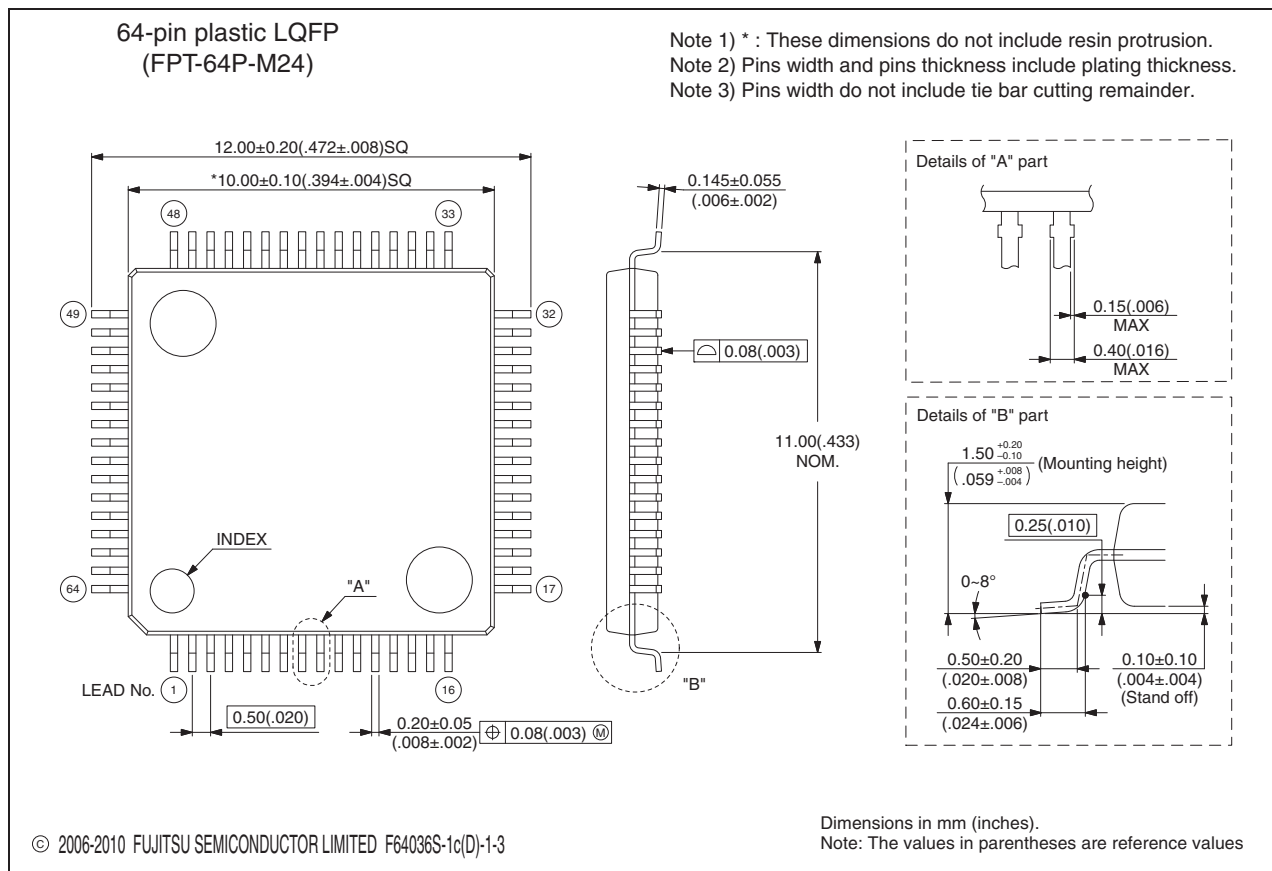
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Dimensions in mm (inches).
Note: The values in parentheses are reference values

(Continued)

(Continued)

<p style="text-align: center;">64-pin plastic LQFP</p> <p style="text-align: center;">(FPT-64P-M24)</p>	Lead pitch	0.50 mm	
	Package width × package length	10.0 mm × 10.0 mm	
	Lead shape	Gullwing	
	Sealing method	Plastic mold	
	Code (Reference)	P-LFQFP64-10×10-0.50	



18. Major Changes

Spansion Publication Number: DS07-13737-6E

Page	Section	Change Results
—	—	Deleted the following package. FPT-64P-M09
13	5. Packages and Product Correspondence	Changed the correspondence package for MB90F351, MB90F351S, MB90F352 and MB90F352S. FPT-64P-M09 → FPT-64P-M23
26	9. Handling Devices	Corrected a typo in number 10. “is used” → “is not used”
64	15. Electrical Characteristics 15.4. AC Characteristics 15.4.4. Clock Output Timing	Changed the Minimum value of cycle time. 41.76 → 41.67
75	15.5. A/D Converter	Changed the notation of “Zero reading voltage” and “Full scale reading voltage”.
81	16. Ordering Information	Changed the part numbers and the package. MB90F351PFM → MB90F351PMC MB90F351SPFM → MB90F351SPMC MB90F352PFM → MB90F352PMC MB90F352SPFM → MB90F352SPMC FPT-64P-M09 → FPT-64P-M23

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90350 Series F²MC-16LX 16-bit Microcontroller				
Document Number: 002-07872				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKFU	09/29/2003	Migrated to Cypress and assigned document number 002-07872. No change to document contents or format.
*A	5755299	AKFU	05/31/2017	Updated to Cypress format.

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