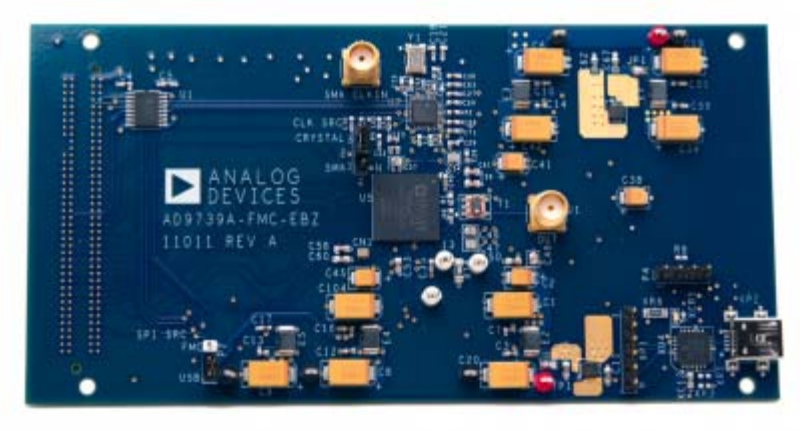
AD9739A Native FMC Card / Xilinx Reference Designs

Introduction

The AD9739A [http://www.analog.com/AD9739A] is a 14-bit, 2.5 GSPS high performance RF DAC capable of synthesizing wideband signals with up to 1.25GHz of bandwidth. This reference design includes a single tone sine generator (DDS) and allows programming the device and monitoring it's internal status registers. It also programs the ADF4350 [http://www.analog.com/ADF4350] clock chip which can generate a 1.6GHz to 2.5GHz clock for the AD9739A from the on-board 25MHz crystal. An alternate clock path using an ADCLK914 [http://www.analog.com/ADCLK914] is available for driving the clock externally.



HW Platform(s): Virtex-6 ML605 (Xilinx) [http://www.xilinx.com/products/boards-and-kits/EK-V6-ML605-G.htm], Kintex-7 KC705 (Xilinx) [http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm] or Virtex-7 VC707 (Xilinx) [http://www.xilinx.com/products/boards-and-kits/EK-V7-VC707-G.htm] and AD9739A-FMC-EBZ [http://www.analog.com/en/digital-to-analog-converters/da-converters/ad9739a/products/EVAL-AD9739A/eb.html] (ADI)
System: Microblaze, AXI, UART

This reference design is based on KC705 IES (rev.C) board.

The AD9739A FMC Card is not fully ANSI/VITA 57.1 compatible:

- does not meet the mechanical form factor (too tall, too long),
- does not include the I2C EEPROM as specified in Rule 5.69,
- Also see “bugs” below.

It was designed, and meets the needs of prototyping platforms, and will work with FPGA Development systems which include an FMC connector. It may not mechanically fit on other ANSI/VITA 57.1 carrier cards.

Quick Start Guide

The reference design has been tested on ML605(Virtex-6), KC705(Kintex-7) and VC707(Virtex-7) boards. The notes below refer to ML605, however the procedure is same for the other boards. Please make sure that you have downloaded and are using the correct design files for your board. The bit file provided combines the FPGA bit file and the SDK elf files. It may be used for a quick check on the system. All you need is the hardware and a PC running a UART terminal and the programmer (IMPACT).

Required Hardware

- ML605/KC705/VC707 board (use the corresponding design file).
- AD9739A-FMC-EBZ board
- Spectrum Analyzer

Required Software

- Xilinx ISE (Programmer (IMPACT) is sufficient for the demo and is available on Webpack). Use the latest version or the one used in the reference design.
- A UART terminal (Tera Term/Hyperterminal), Baud rate 57600.

Bit file

- Download the gzip file and extract the sw/cf_ad9739a_mb.bit file.

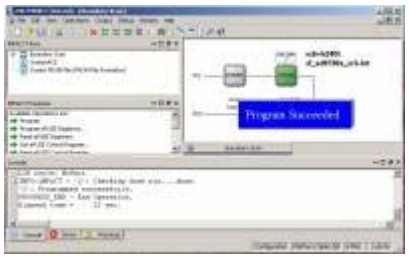
Running Demo (SDK) Program

If you are not familiar with ML605 and/or Xilix tools, please visit
http://www.xilinx.com/products/boards/ml605/reference_designs.htm
[http://www.xilinx.com/products/boards/ml605/reference_designs.htm] for details.

To begin, connect the AD9739A-FMC-EBZ board to the FMC-LPC connector of ML605 board (see image below). If using KC705 use FMC-LPC, if using VC707 use FMC1-HPC. Connect power and two USB cables from the PC to the *JTAG* and *UART* USB connectors on the edge of the ML605. A spectrum analyzer should be connected to the output SMA jack (OUT/J1). This quick start program uses a 2.5GHz DAC clock and generates a 300MHz tone. Adjust your spectrum analyzer accordingly. On the AD9739A-FMC board, ensure that the SPI source jumper (SPI SRC/P2) is set

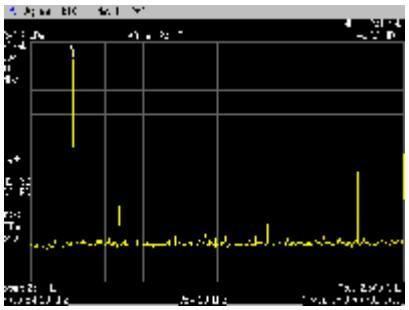
to FMC and the clock source jumper (CLK SRC/P3) is set to crystal (XTAL). The USB connection on the AD9739A-FMC-EBZ and the SMA Clock Input (SMA CLKIN/J3) are not used in this example. After the hardware setup, turn the power on to the ML605.

Start IMPACT, and initialze the JTAG chain. The program should recognize the Virtex 6 device for ML605 (see screenshot below). Start a UART terminal (set to 57600 baud rate) and then program the device.



If programming was successful, you should be seeing messages appear on the terminal as shown in figure below. After programming the AD9739A and ADF4350, the program continously monitors the MU Controller and LVDS Receiver lock status. If either of them are out of lock, the program quits itself with an error. You may also quit the program by pressing 'q' and then the 'Enter' key.

The specturm analyzer output is shown below.



DOCSIS Results

Data Over Cable Service Interface Specification [http://en.wikipedia.org/wiki/DOCSIS] is an international telecommunications standard that permits the addition of high-speed data transfer to an existing cable TV (CATV) system. It is employed by many cable television operators to provide data access over their existing infrastructure. It has many specification, certification, and testing criteria. Below are example ACLR and spur measurements for this card with the AD9739A running at 2.5GHz with carrier(s) centered at 980MHz.

Adjacent Channel Leakage Ratio (ACLR) is the ratio of the reconstructed signal power to the power measured in an adjacent channel measured in dB. This is critical in many applications, and can be used to determine the performance of the subsystem in many applications, including DOCSIS.

Click on any picture, to make it bigger, and see the measurement results.

Single Channel

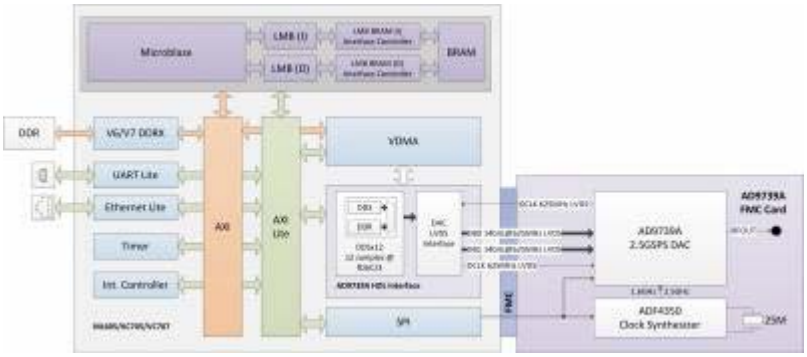
Four Channel

Eight Channel

Using the reference design

Functional description

The reference design consists of two functional modules, a DDS/LVDS interface and a SPI interface. It is part of an AXI based microblaze system as shown in the block diagram below. It is designed to support linux running on microblaze. All other peripherals are available from Xilinx as IP cores.



The DDS consists of a Xilinx DDS IP core and a DDR based data generator. The core generates 6 samples at every fDAC/3 clock cycles for each port of AD9739A. The frequency of the DDS as well as the LUT entries are programmable via SDK.

The SPI interface allows programming the ADF4350 and/or AD9739A. The provided SDK software shows the initial setup required for both the devices for a 2.5GHz DAC clock with a 300MHz single tone DDS.

Registers

QW Address[1]	Bits	Name	Description
0x00	31	version	32'h00_01_00_61
0x01	18	select	Data select DDS (0x0) or DDR (0x1).
	17	interpolate	DDR data interpolate 4x (0x1) or disabled (0x0).
	16	enable	DDS enable (0x1) or disable (0x0).
	15:0	phasecnt	DDS phase count.
0x09	1	vdma-ovf	DMA overflow (W1C).
	0	vdma-unf	DMA underflow (W1C).
1. For AXI-Lite byte addresses, multiply by 4.			
2. Registers defaults to 0x0 unless otherwise specified.			

Notes

In order to fully use the reference design, you will need to generate all the Xilinx IP's used by the reference design yourself. The following two files are missing from the gzip file.

pcores/cf_ad9739a_core_v1_00_a/netlist/cf_ddsx_1.ngc
pcores/cf_ad9739a_core_v1_00_a/hdl/verilog/cf_ddsx_1.v

You must generate these two files using coregen. The reference design uses the following parameters:

amplitude_mode=Full_Range
channels=1
noise_shaping=Taylor_Series_Corrected
output_selection=Sine
output_width=16
partspresent=SIN_COS_LUT_only
phase_increment=Fixed
phase_offset=None
phase_width=16

The above list is partial and only lists the key parameters for reference.

Hardware Reference

There are several hardware options available on the AD9739A-FMC-EBZ:

Clock Selection

Two clock paths are availabe to drive the clock input on the AD9739A-FMC-EBZ. The factory default option connects the ADF4350 [http://www.analog.com/ADF4350] to the AD9739A [http://www.analog.com/AD9739A]. The ADF4350 [http://www.analog.com/ADF4350] is able to synthesize a clock over the entire specified range of the AD9739A [http://www.analog.com/AD9739A] (1.6GHz to 2.5GHz).

Alternatively, an external clock can be provided via the SMA CLKIN (J3) jack. To enable this clock path, jumper CLK SRC (P3) must be moved to the SMA 1 position. C102 and C99 on the back of the board also need to be removed from their default position, and then soldered into the vertical position from the large square pad they were previously soldered to and the narrow pads closer to the ADCLK914 [http://www.analog.com/ADCLK914] (U3). Observe the orientation of the caps before removing them; they must be soldered with their narrow edge against the PCB, and not the wide side as is common with most components.

SPI Source Selection

There are two options for driving the SPI port of the AD9739A [http://www.analog.com/AD9739A] and ADF4350 [http://www.analog.com/ADF4350]. The first, which is used in the quick start guide above, is to have all the SPI lines driven by the FPGA. In this case, jumper SPI SRC (P2) is set to FMC. A level transltor (ADG3308 [http://www.analog.com/ADG3308] U1) is used to translate the 2.5V logic from the FPGA to the 3.3V logic required by the parts on the board.

The other option for driving the SPI is to use on the on-board USB microcontroller. In this case, the data path is still connected to the FMC connector, but the SPI lines are driven by the microcontroller. This allows the use of the graphical interface PC software which is included with the standard Analog Devices evaluation boards. This option makes it easier to experiment with various settings on the parts before programming the parts from the FPGA.

For the highest performance (noise floor below -105dBm), do not power the USB microcontroller while taking measurements. After configuring the part over USB, remove jumper P2. This does not apply to the FMC SPI option, in which case the USB microcontroller is already powered down

ADF4350 USB SPI Software

The software for controlling the ADF4350 clock chip is installed to the start menu at Start > Programs > Analog Devices > AD9739A > ADF4350 SPI for AD9739A-FMC-EBZ. Once open, select File…Open Setup File. Browse for the file 2_5GHz for AD9739A.ini, which is located in Analog Devices\HSDAC\AD9739A inside your Program Files directory (usually C:\Program Files or C:\Program Files(x86)). This will setup the clock chip to provide a 2.5GHz clock to the AD9739A.

AD9739A USB SPI Software

The SPI software is broken up into numerous sections. Several of them are described here, as they pertain to the evaluation board. For complete descriptions of each SPI register, see the AD9739A datasheet. In the interest of continuous quality improvements, the images below may not exactly match your version of the software.

SPI Settings and Powerdown/Reset

These bits (shown in Figure 12) control the operation of the SPI port on the AD9739A, as well as the master reset and individual power-down bits. Changing the SDIO DIR or DATADIR bits will cause the SPI application to stop functioning correctly. Do not change these bits. The Reset button is “sticky”, that is, the part will stay in reset for as long as the button is enabled. To reset the part, set this bit, run the SPI application, then unset this bit and run the application again.

Controller Clock Controls and Analog FS controls

The Controller Clock controls enable the Mu Controller and LVDS controllers. For normal operation, both of these should be enabled. The Clock GEN PD switch powers down the clocking structure, and should be left disabled for normal use.

The DAC current ouput has an adjustable full-scale value. The FSC Set option allows for this adjustment. After running the SPI application, the full-scale current in miliamps will be displayed here.

Mu Controller Clock Enable: Register 0x02 Bit 0 LVDS Controller Clock Enable: Register 0x02 Bit 1 Analog Full-Scale Setting (10 bit Gain DAC 10-30mA adjustment): Register 0x06 bit 0:8, Register 0x07 bits 0,1

Decoder Controller and IRQ Controls

Decoder Mode: Register 0x08 Bits 0,1 0x0 – Normal Mode 0x1 – Return to zero (RZ) Mode 0x2 – Mix Mode

Cross Control

CLKP Offset Setting: Register 0x24 Bits 0-3 CLKP Direction Bit: Register 0x24 Bit 4 CLKP Offset Setting: Register 0x25 Bits 0-3 CLKP Direction Bit: Register 0x25 Bit 4 Damp: Register 0x25 Bits 7

Mu Controller

Mu Controller Enable: Register 0x26 Bit 0 (Set to 1 to enable the controller)

Mu Controller Gain: Register 0x26 Bits 1,2 (Optimal Setting is a Gain of 1) MU Desired Phase: Desired Phase Value for Phase to Voltage Converter to Optimize Mu Controller. The optimal setting is negative 6 (max of 16) . Register 0x27 bits 0-4 Slope: Slope the mu contoller will lock onto Register 0x26 bit 6 (Optimal setting is Negative slope set bit to 0) MU_DEL_Manual: Register 0x28 bits 0-7 and 0x27 bits 6,7: Sets the point where the Mu Controller begins to search. It is best to set it to the middle of the delay line . The maximum Mu delay is 432, so set these bits to approximately 220. Mode: Register: 0x26 Bits 4, 5 Sets the Mode in which the Controller searches:

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0x00 – Search and Track (Optimal Setting)
0x01 – Track Only
0x10 – Search Only
0x11 – Invalid
```

Search Mode: 0x27 – Bits 5, 6 Sets the Mode in which the search for the optimal phase is performed

```
0x00 – Down
0x01 – Up
0x10 – Up/Down (Optimal Setting)
0x11 – Invalid
```

Search GB: sets a GB from the beginning and end of the Mu Delay line in which the Mu controller will not enter into unless it does not find a valid phase outside the GB. Register 0x29 bits 0-4. Optimal value is Decimal 11. Tolerance: Sets the Tolerance of the phase search. Register 0x29 bit 7

```
0 – Not Exact. Can find a phase within 2 phases of the desired phase
1- Exact. Finds the exact phase you are targeting (Optimal Setting)
```

ContRST: Controls whether the controller will reset or continue if it does not find the desired phase

```
0 – Continue (Optimal Setting)
1 – Reset
```

Phase Detector Enable: Register 0x24 bit 5. Enables the Phase Detector (Set to 1 to enable the Phase Detector) Phase Detector Comparator Boost: Optimizes the bias to the Phase Detector (Set to 1 to enable) Bias: Register 0x24 Bits 0-3: Manual Control of the bias if the Boost control is not enabled Duty Cycle Fix: Register 0x25 Bit 7 Enables the duty cycle correction in the Mu Controller. Recommended to always enable (Set to 1 to enable) Direction: Register 0x25 Bit 6 Sets the direction that the duty cycle will be corrected

```
0 – Negative (Optimal Setting)
1 - Positive
```

Offset: Register Register 0x25 Bit 0-5 Sets the Duty Cycle Correction manually if Fix is not enabled

The status read back bits for the mu controller are as follows: MU_LCK: Register 0x2A bit 0 (value of 1 means the controller is locked) LST_LCK: Register 0x2A bit 1 (Value of 1 means the control lost lock)

In order to read back the present MU Delay and phase value, it is necessary to set the Read bit high and then low before the values can be read back: Read: Register 0x26 Bit 3 Mu Delay Readback: Register 0x28 bits 0-7 and 0x27 bits 6,7 (Total of 9 bits in the read back the maximum Mu delay value is d432 or x1B0) MUD_PH_Readback: Register 0x27 bits 0-4 – Phase the controller locked to. In order to use the Mu controller in manual mode the following bits are utilized:

`Mu Controller Enable: Register 0x26 Bit 0 (Set to 0 to disable the controller)`

MU_DEL_Manual: Register 0x28 bits 0-7 and 0x27 bits 7,8. (Total of 9 bits the maximum Mu delay value is d432 or x1B0)

LVDS Receiver Controls

Downloads

Design Files

- ML605 Reference Design Source Code
- KC705 Reference Design Source Code
- VC707 Reference Design Source Code
- Download the AD9739A USB SPI Software and Drivers [http://www.analog.com/en/digital-to-analog-converters/da-converters/ad9739a/products/EVAL-AD9739A/eb.html]

Design

- AD9739A-FMC-EBZ Schematic
- AD9739A-FMC-EBZ Gerber Files
- AD9739A-FMC-EBZ Layout

Rev A and Rev B of this board mistakenly do not follow Rule 5.62 on the ANSI/VITA 57.1 spec - *"The FMC module shall connect TDI to TDO, if the module does not use the JTAG interface."* This may cause some FMC platforms (like the VC707 and KC705) to loose JTAG communication when this card is plugged in. It's normally a simple matter to short D30 and D31 on the development system (sorry, this will be fixed shortly)

Third Party Bitstreams

Below is a list of hardware, IP Cores, or reference designs. While this content is believed to be reliable, many have not been validated, verified or reviewed by Analog Devices. These boards/platforms may or may not be suitable for end product integration or development, and may not meet datasheet specifications. Since many of these platforms or IP Cores are not

designed or reviewed by Analog Devices, care should be taken to ensure that these will meet your needs before purchase. While ADI will always provide chip level support on the EngineerZone™ [http://ez.analog.com/], board level, or reference design support is given by the manufacture or creator of the specific materials.

References to manufacturer or third party software, websites, or to any specific commercial or non-commercial products are suggestions only and do not necessarily constitute or imply an endorsement, recommendation, or favoring by Analog Devices.

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- 4 x independent DVB-T channels, RF output (0 to 1.250 GHz) from MVD Cores [http://www.mvd-fpga.com/cores/en/digilent_AD9739A_xilinx_eval.html]
- 4 x independent ATSC channels, RF output (0 to 1.250 GHz)from MVD Cores [http://www.mvd-fpga.com/cores/en/digilent_AD9739A_xilinx_eval.html]
- 4 x independent J.83B channels, RF output (0 to 1.250 GHz) from MVD Cores [http://www.mvd-fpga.com/cores/en/digilent_AD9739A_xilinx_eval.html]
- 4 x independent DVB-C J.83A/C channels, RF output (0 to 1.250 GHz) from MVD Cores [http://www.mvd-fpga.com/cores/en/digilent_AD9739A_xilinx_eval.html]

Tar file contents

The tar file contains, in most cases, the following files and/or directories. To rebuild the reference design simply double click the XMP file and run the tool. To build SDK, select a workspace and use the C file to build the elf file. Please refer to Xilinx EDK documentation [http://www.xilinx.com/support/documentation/dt_edk_edk13-2.htm] for details.

license.txt	ADI license & copyright information.
system.bsb	BSB wizard file.
system.mhs	MHS file.
system.xmp	XMP file (use this file to build the reference design).
data/	UCF file and/or DDR MIG project files.
docs/	Documentation files (Please note that this wiki page is the documentation for the reference design).
ise/	ISE project file(s) (for stand alone build) and/or simulation.
pcores/	Reference design core file(s) (Xilinx EDK).
scripts/	Individual scripts for platgen, xst, xflow etc. for command line run.
sw/	Software (Xilinx SDK) & bit file(s).
tb/	Test bench source file(s).

More information

- Purchase AD9739A-FMC-EBZ [http://www.analog.com/en/digital-to-analog-converters/da-converters/ad9739a/products/EVAL-AD9739A/eb.html]
- VITA's FMC info [http://www.vita.com/fmc.html]
- ask questions about the FPGA reference design [http://ez.analog.com/community/fpga]
- ask questions about the AD9739A [http://ez.analog.com/community/data_converters/high-speed_dacs]