ST2S06A33
ST2S06B - ST2S06D33

Dual synchronous rectification with reset or inhibit, 0.5 A, 1.5 MHz adjustable step-down switching regulator

Features

- Step-down current mode PWM (1.5 MHz) DC-DC converter
- Fixed or adjustable output voltage from 0.8 V
- 2% DC output voltage tolerance
- Synchronous rectification
- Reset function for A and D versions
- Inhibit function for B version
- Internal soft start for start-up current limitation and power ON delay of 50-100 µs
- Typical efficiency: > 90%
- 0.5 A output current capability
- Non-switching quiescent current: max 1 mA over temperature range
- $R_{DS(ON)}$ 150 mΩ (typ.)
- Uses tiny capacitors and inductors
- Available in QFN12L (4x4 mm)

QFN12L (4x4 mm)

Description

The ST2S06 is a dual step-down DC-DC converter optimized for powering low-voltage digital cores in ODD applications and, generally, to replace the high current linear solution when the power dissipation may cause a high heating of the application environment. It provides up to 0.5 A over an input voltage range of 2.5 V to 5.5 V.

A high switching frequency of 1.5 MHz allows the use of tiny surface-mount components as well as a resistor divider to set the output voltage value. Only an inductor and two capacitors are required. A low output ripple is guaranteed by the current mode PWM topology and the utilization of low ESR SMD ceramic capacitors. The device is thermally protected and current limited to prevent damage due to accidental short circuit. The ST2S06 series is available in the QFN12L (4x4 mm) package.

Table 1. Device summary

Order code	Package	Packaging
ST2S06APQR(1)	QFN12L (4x4 mm)	Tape and reel
ST2S06A33PQR	QFN12L (4x4 mm)	Tape and reel
ST2S06D33PQR	QFN12L (4x4 mm)	Tape and reel
ST2S06BPQR	QFN12L (4x4 mm)	Tape and reel

1. Available on request.

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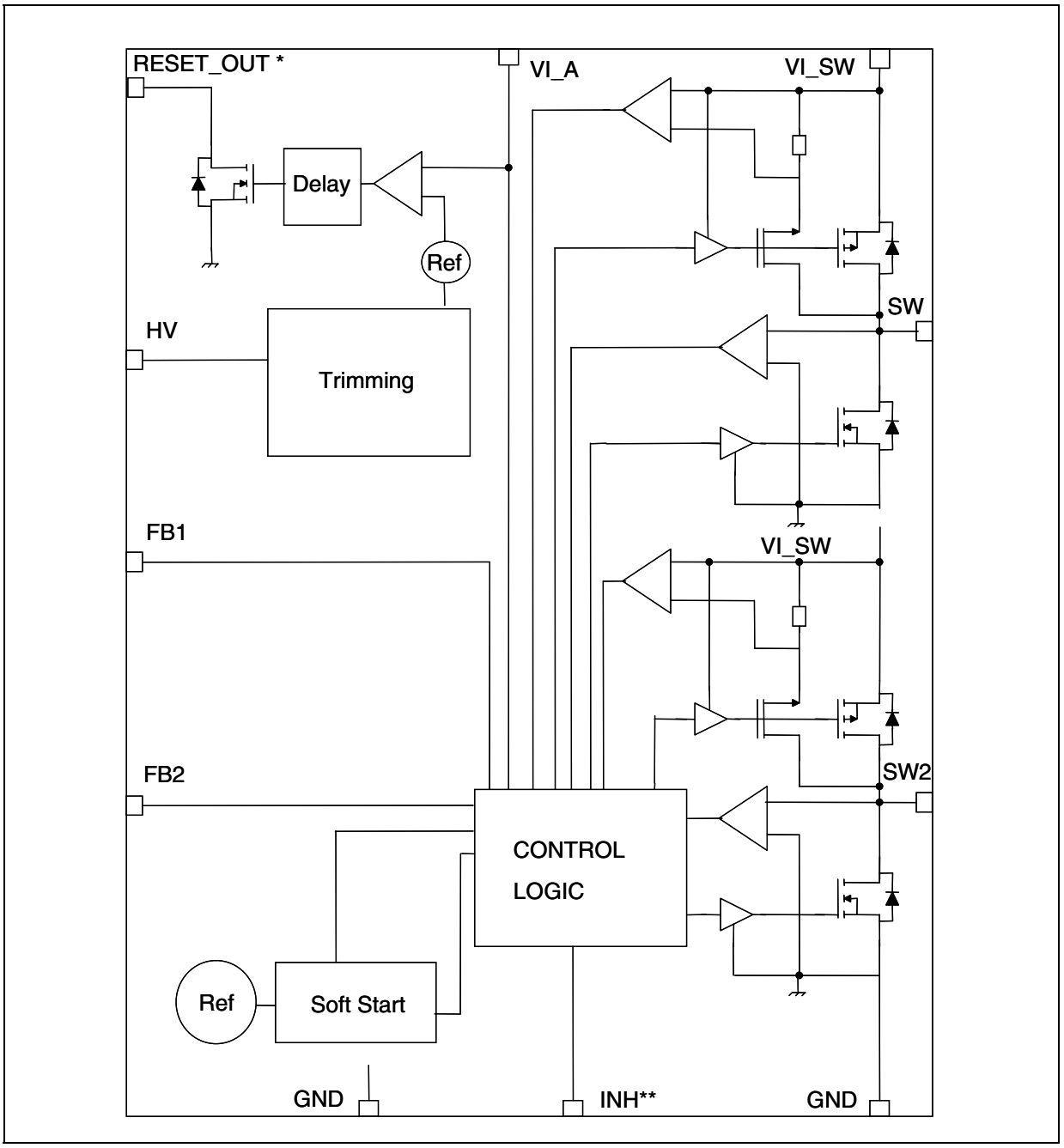
1 Diagram

Figure 1. Schematic diagram



* ST2S06A/D

** ST2S06B

2 Pin configuration

Figure 2. Pin connections (top view)

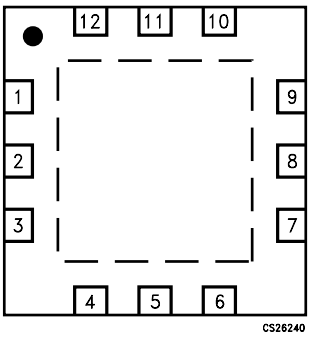


Table 2. Pin description

Pin n°	ST2S06A/D	ST2S06B	Name and function
1	HV	HV	Programing pin. It must be floating or connected to GND.
2	FB2	FB2	Feedback voltage
3	GND2	GND2	Power ground
4	SW2	SW2	Switching pin
5	VIN_SW	VIN_SW	Power input voltage pin
6	SW1	SW1	Switching pin
7	GND1	GND1	Power ground
8	FB1/OUT1	FB1	Feedback voltage / output voltage
9	Reset_out	NC	Reset out pin
10	NC	INH	Inhibit pin
11	VIN_A	VIN_A	Supply for analog circuit
12	GND_A	GND_A	System ground

3 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_SW}	Positive power supply voltage	-0.3 to 7	V
V_{IN_A}	Positive power supply voltage	-0.3 to 7	V
V_{INH}	Inhibit voltage	-0.3 to 7	V
SWITCH voltage	Max. voltage of output pin	-0.3 to 7	V
$V_{FB1,2}/V_{O1}$	Feedback voltage/output voltage	-0.3 to 2.5	V
V_{O1}	Output voltage (for V_O > 1.6 V)	-0.3 to 5	V
Current into VFB pin	Common mode input voltage	+1 to -1	mA
T_J	Max junction temperature	150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{LEAD}	Lead temperature (soldering) 10 sec.	300	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	10	°C/W
R_{thJA}	Thermal resistance junction-ambient	60	°C/W

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM-DH11C	4	kV

4 Electrical characteristics

Table 6. Electrical characteristics for ST2S06A (V_{IN_SW} = V_{IN_A} = 5 V, $V_{O1,2}$ = 1.2 V, C_1 = 4.7 µF, C_2 = C_3 = 22 µF, L1 = L2 = 3.3 µH, T_J = -30 to 125 °C unless otherwise specified. Typical values are referred to 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$FB_{1,2}$	Feedback voltage		784	800	816	mV
$I_{FB1,2}$	V_{FB} pin bias current	V_{FB} = 1 V			600	nA
I_Q	Quiescent current	V_{FB} = 1 V			1.2	mA
$I_{O1,2}$	Output current	V_{IN} = 2.5 to 5.5 V (1)		0.8		A
I_{MIN}	Minimum output current		1			mA
$\%V_{O1,2}/\Delta V_{IN}$	Reference line regulation	2.5 V < V_{IN} < 5.5 V		0.032		$\%V_O/V_{IN}$
$\Delta V_{O1,2}$	Reference load regulation	10 mA < I_O < 0.5 A		5.5	15	mV
PWM f_S	PWM switching frequency	V_{FB} = 0.7 V, T_A = 25°C	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0.7 V, T_A = 25°C	85	94		%
I_{SWL}	Switching current limitation		1	1.2		A
I_{LKN}	NMOS leakage current	V_{FB} = 0.9 V, T_A = 25°C		0.1		µA
I_{LKP}	PMOS leakage current	V_{FB} = 0.9 V, T_A = 25°C		0.1		µA
R_{DSon}-N	NMOS switch on resistance	I_{SW} = 250 mA		0.15	0.3	Ω
R_{DSon}-P	PMOS switch on resistance	I_{SW} = 250 mA		0.2	0.4	Ω
η	Efficiency	I_O = 20 mA to 100 mA		75		%
		I_O = 100 mA to 0.5 A		90		%
T_{SHDN}	Thermal shut down (2)		130	150		°C
T_{HYS}	Thermal shut down hysteresis (2)			15		°C
$\Delta V_{O1,2}/\Delta I_O$	Load transient response (2)	100 mA < I_O < 500 mA, t_R = t_F => 100 ns, T_A = 25°C	-5		+5	$\%V_O$
Reset section						
t_{DEL}	Delay time	T_A = 25°C	80	85		ms
V_{RES}	Reset in threshold measured on input pin	V_{IN_A} Rising	4.5	4.6	4.75	V
		V_{IN_A} Falling	4.12	4.2	4.28	

1. V_O = 90% of nominal value.
2. Guaranteed by design, but not tested in production.

Table 7. Electrical characteristics for ST2S06A33 (V_{IN_SW} = V_{IN_A} = 5 V, V_{01} = 3.3 V, V_{O2} = 1.2 V, C_1 = 4.7 µF, C_2 = C_3 = 22 µF, L1 = L2 = 3.3 µH, T_J = -30 to 125 °C unless otherwise specified. Typical values are referred to 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OUT_1	Output feedback pin		3.23	3.3	3.37	V
FB_2	Feedback voltage		784	800	816	mV
I_{O1}	I_{O1} pin bias current	V_O = 3.5 V		15	20	µA
I_{FB2}	V_{FB} pin bias current	V_{FB} = 1 V			600	nA
I_Q	Quiescent current	V_{FB} = 1 V			1.2	mA
$I_{O1,2}$	Output current	V_{IN} = 4 to 5.5 V (1)		0.8		A
I_{MIN}	Minimum output current		1			mA
$\%V_{O1,2}/\Delta V_{IN}$	Reference line regulation	4V < V_{IN} < 5.5 V		0.032		$\%V_O/V_{IN}$
$\Delta V_{O1,2}$	Reference load regulation	10mA < I_O < 0.5 A		5.5	15	mV
PWM f_S	PWM switching frequency(1)	V_{FB} = 0.7 V, T_A = 25°C	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0.7 V, T_A = 25°C	85	94		%
I_{SWL}	Switching current limitation		1	1.2		A
I_{LKN}	NMOS leakage current	V_{FB} = 0.9 V, T_A = 25°C		0.1		µA
I_{LKP}	PMOS leakage current	V_{FB} = 0.9 V, T_A = 25°C		0.1		µA
R_{DSon}-N	NMOS switch on resistance	I_{SW} = 250 mA		0.15	0.3	Ω
R_{DSon}-P	PMOS switch on resistance	I_{SW} = 250 mA		0.2	0.4	Ω
η	Efficiency	I_O = 20 mA to 100 mA		75		%
		I_O = 100 mA to 0.5 A		90		%
T_{SHDN}	Thermal shut down (2)		130	150		°C
T_{HYS}	Thermal shut down hysteresis (2)			15		°C
$\Delta V_{O1,2}/\Delta I_O$	Load transient response (2)	100 mA < I_O < 500 mA t_R = t_F => 100 ns, T_A = 25°C	-5		+5	$\%V_O$
Reset section						
t_{DEL}	Delay time	T_A = 25°C	80	85		ms
V_{RES}	Reset in threshold measured on input pin	V_{IN_A} Rising	4.5	4.6	4.75	V
		V_{IN_A} Falling	4.12	4.2	4.28	

1. V_O= 90% of nominal value.
2. Guaranteed by design, but not tested in production.

Table 8. Electrical characteristics for ST2S06D33 (V_{IN_SW} = V_{IN_A} = 5 V, V_{01} = 3.3 V, V_{O2} = 1.2 V, C_1 = 4.7 µF, C_2 = C_3 = 22 µF, L1 = L2 = 3.3 µH, T_J = -30 to 125 °C unless otherwise specified. Typical values are referred to 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OUT_1	Output feedback pin		3.23	3.3	3.37	V
FB_2	Feedback voltage		784	800	816	mV
I_{O1}	I_{O1} pin bias current	V_O = 3.5 V		15	20	µA
I_{FB2}	V_{FB} pin bias current	V_{FB} = 1 V			600	nA
I_Q	Quiescent current	V_{FB} = 1 V			1.2	mA
$I_{O1,2}$	Output current	V_{IN} = 4 to 5.5 V (1)		0.8		A
I_{MIN}	Minimum output current		1			mA
$\%V_{O1,2}/\Delta V_{IN}$	Reference line regulation	4V < V_{IN} < 5.5 V		0.032		$\%V_O/V_{IN}$
$\Delta V_{O1,2}$	Reference load regulation	10mA < I_O < 0.5 A		5.5	15	mV
PWM f_S	PWM switching frequency(1)	V_{FB} = 0.7 V, T_A = 25°C	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0.7 V, T_A = 25°C	85	94		%
I_{SWL}	Switching current limitation		1	1.2		A
I_{LKN}	NMOS leakage current	V_{FB} = 0.9 V, T_A = 25°C		0.1		µA
I_{LKP}	PMOS leakage current	V_{FB} = 0.9 V, T_A = 25°C		0.1		µA
R_{DSon}-N	NMOS switch on resistance	I_{SW} = 250 mA		0.15	0.3	Ω
R_{DSon}-P	PMOS switch on resistance	I_{SW} = 250 mA		0.2	0.4	Ω
η	Efficiency	I_O = 20 mA to 100 mA		75		%
		I_O = 100 mA to 0.5 A		90		%
T_{SHDN}	Thermal shut down (2)		130	150		°C
T_{HYS}	Thermal shut down hysteresis (2)			15		°C
$\Delta V_{O1,2}/\Delta I_O$	Load transient response (2)	100 mA < I_O < 500 mA t_R = t_F => 100 ns, T_A = 25°C	-5		+5	$\%V_O$
Reset section						
t_{DEL}	Delay time	T_A = 25°C	52	65	78	ms
V_{RES}	Reset in threshold measured on input pin	V_{IN_A} Rising			4.55	V
		V_{IN_A} Falling	3.625	3.7	3.775	

1. V_O= 90% of nominal value.
2. Guaranteed by design, but not tested in production.

Table 9. Electrical characteristics for ST2S06B (V_{IN_SW} = V_{IN_A} = 5 V, $V_{O1,2}$ =1.2 V, C_1= 4.7 µF, C_2 = C_3 = 22 µF, L1 = L2 = 3.3 µH, T_J = -30 to 125 °C unless otherwise specified. Typical values are referred to 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$FB_{1,2}$	Feedback voltage		784	800	816	mV
$I_{FB1,2}$	V_{FB} pin bias current	V_{FB} = 1 V			600	nA
I_Q	Quiescent current	V_{INH} > 1.2 V, V_{FB} = 1 V			1	mA
		V_{INH} < 0.4 V			1	µA
$I_{O1,2}$	Output current	V_{IN} = 2.5 to 5.5 V (1)		0.8		A
I_{MIN}	Minimum output current		1			mA
V_{INH}	Inhibit threshold	2.5V < V_{IN} < 5 V	1.2			V
		2.5V < V_{IN} < 5.5 V	1.3			
		Device OFF			0.4	
$I_{INH1,2}$	Inhibit pin current				2	µA
$\%V_{O1,2}/\Delta V_{IN}$	Reference line regulation	2.5V < V_{IN} < 5.5 V		0.032		$\%V_O/V_{IN}$
$\Delta V_{O1,2}$	Reference load regulation	10 mA < I_O < 0.5 A		5.5	15	mV
PWM f_S	PWM switching frequency(1)	V_{FB} = 0.7 V, T_A = 25°C	1.2	1.5	1.8	MHz
D_{MAX}	Maximum duty cycle	V_{FB} = 0.7 V, T_A = 25°C	85	94		%
I_{SWL}	Switching current limitation		1	1.2		A
I_{LKN}	NMOS leakage current	V_{FB} = 0.9 V, T_A = 25°C		0.1		µA
I_{LKP}	PMOS leakage current	V_{FB} = 0.9 V, T_A = 25°C		0.1		µA
R_{DSon}-N	NMOS switch on resistance	I_{SW} = 250 mA		0.15	0.3	Ω
R_{DSon}-P	PMOS switch on resistance	I_{SW} = 250 mA		0.2	0.4	Ω
η	Efficiency	I_O = 20 mA to 100 mA		75		%
		I_O = 100 mA to 0.5 A		90		%
T_{SHDN}	Thermal shut down (2)		130	150		°C
T_{HYS}	Thermal shut down hysteresis (1)			15		°C
$\Delta V_{O1,2}/\Delta I_O$	Load transient response (1)	100 mA < I_O < 500 mA, t_R = t_F1 => 100 ns, T_A = 25°C	-5		+5	$\%V_O$

1. V_O= 90% of nominal value.
2. Guaranteed by design, but not tested in production.

5 Typical performance characteristics

Figure 3. Feedback voltage 1 vs. temperature (ST2S06B)

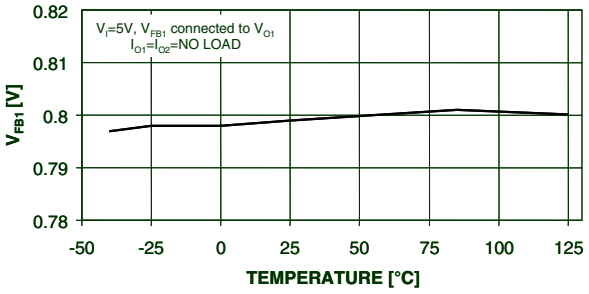


Figure 4. Feedback voltage 2 vs. temperature (ST2S06B)

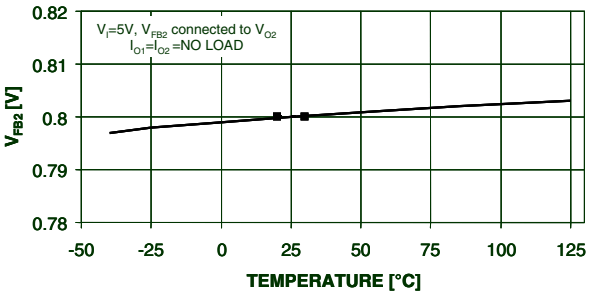


Figure 5. Efficiency vs. output current 1

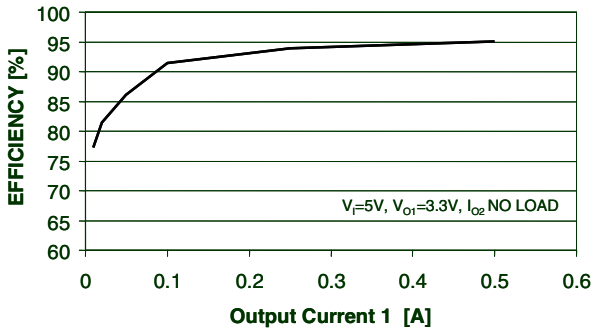


Figure 6. Efficiency vs. output current 2

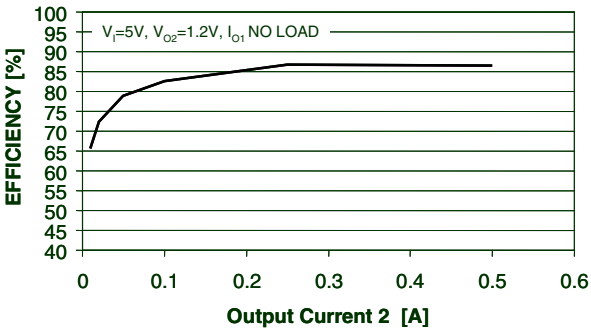


Figure 7. Switching frequency vs. temperature (ST2S06A)

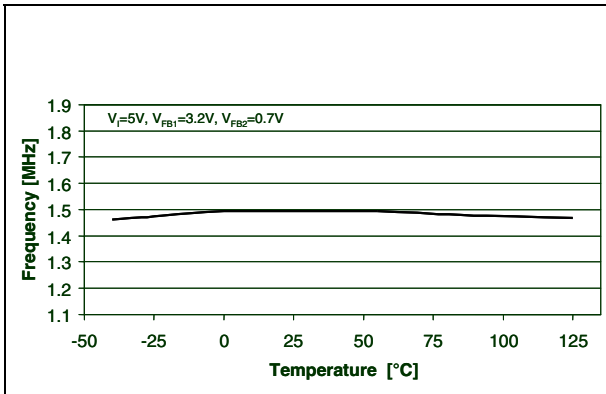


Figure 8. Duty cycle vs. temperature (ST2S06A)

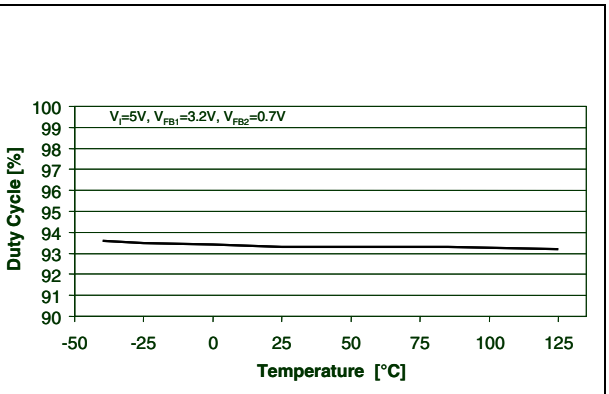


Figure 9. Switching frequency vs. temperature (ST2S06B)

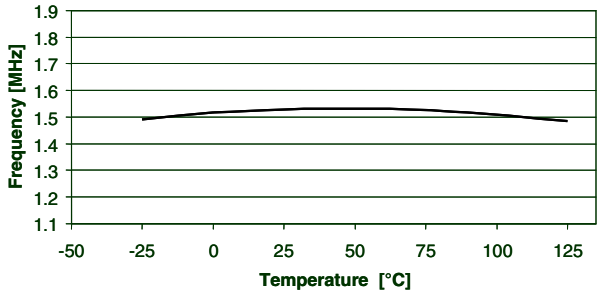


Figure 10. Inhibit threshold vs. temperature (ST2S06B)

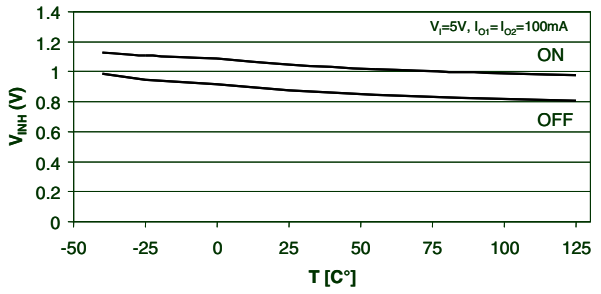


Figure 11. Switching current limitation vs. input voltage (ST2S06A)

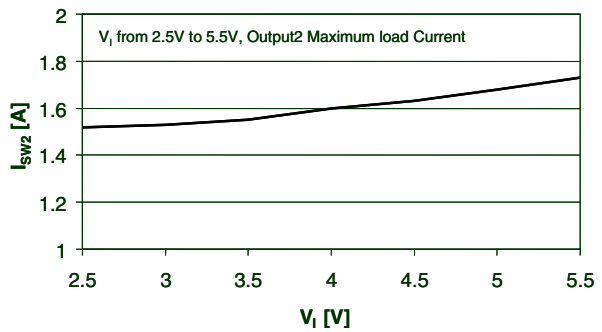


Figure 12. PMOS switch on resistance vs. temperature

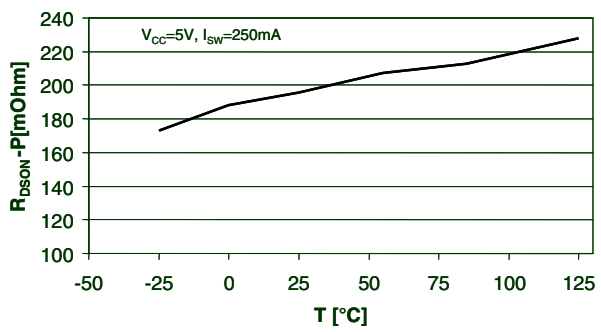


Figure 13. NMOS switch on resistance vs. temperature

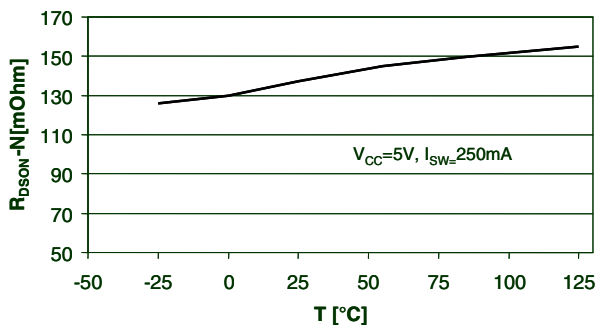
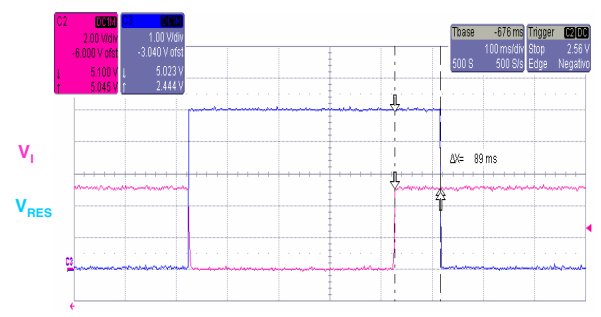


Figure 14. Delay time vs. temperature (ST2S06A)



V_I Rising from 0V to 5V, Delay from V_{RES} threshold and reset pin below 0V.

Figure 15. Delay time vs. temperature (ST2S06A)

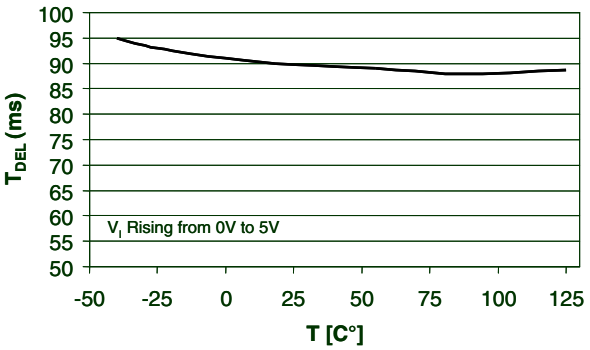


Figure 16. Reset in threshold vs. temperature (ST2S06A)

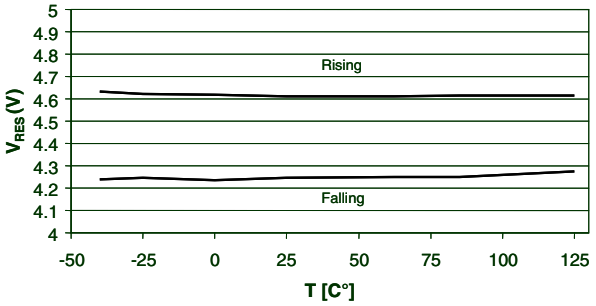


Figure 17. Reset in threshold vs. temperature (ST2S06D)

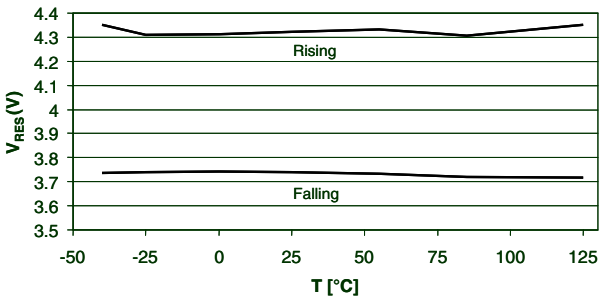


Figure 18. Delay time vs. temperature (ST2S06D)

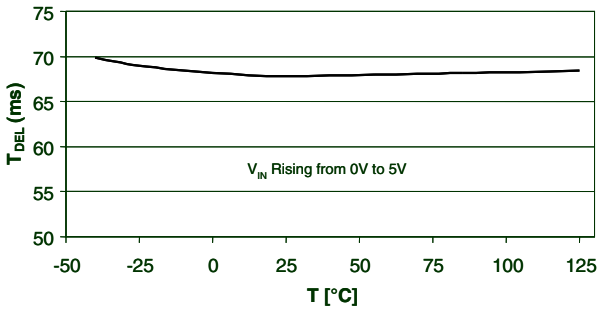
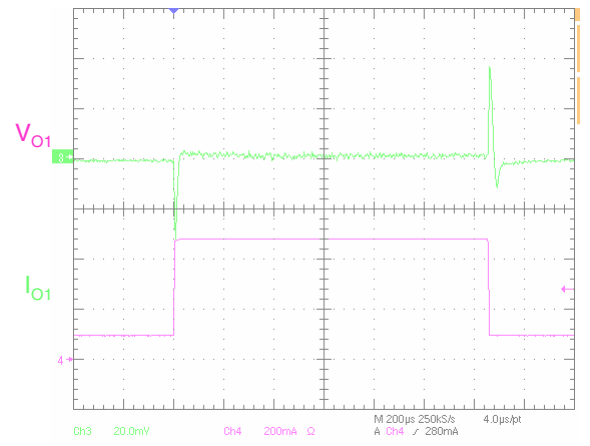
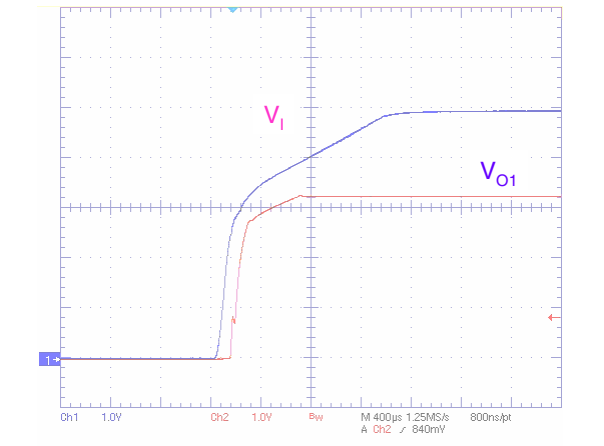


Figure 19. Load transient response (ST2S06A)



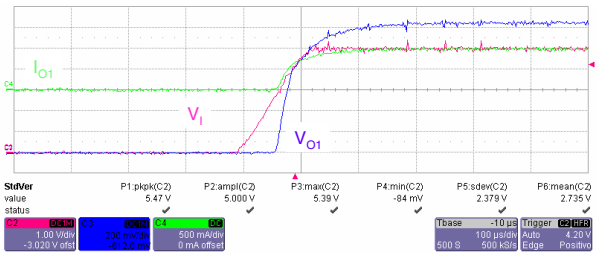
V_I= 5V, I_{O1} from 100mA to 500mA

Figure 20. Start-up transient (ST2S06A)



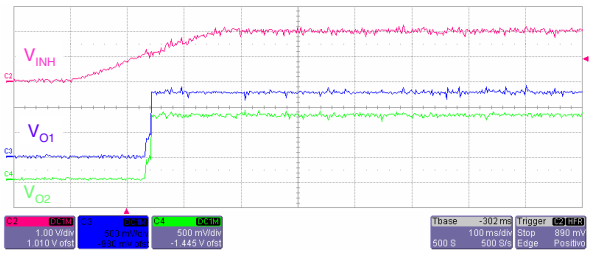
V_I= from 0V to 5V, I_{O1}=500mA, Output Voltage=3.3V

Figure 21. Start-up transient (ST2S06B)



V_I= from 0V to 5V, I_{O1} =1A, Output Voltage=1.2V

Figure 22. Inhibit transient (ST2S06B)



V_{INH}= from 0V to 2V, V_I=5V, I_{O1}=I_{O2}=1A

6 Typical application

Figure 23. Application circuit for ST2S06A/D

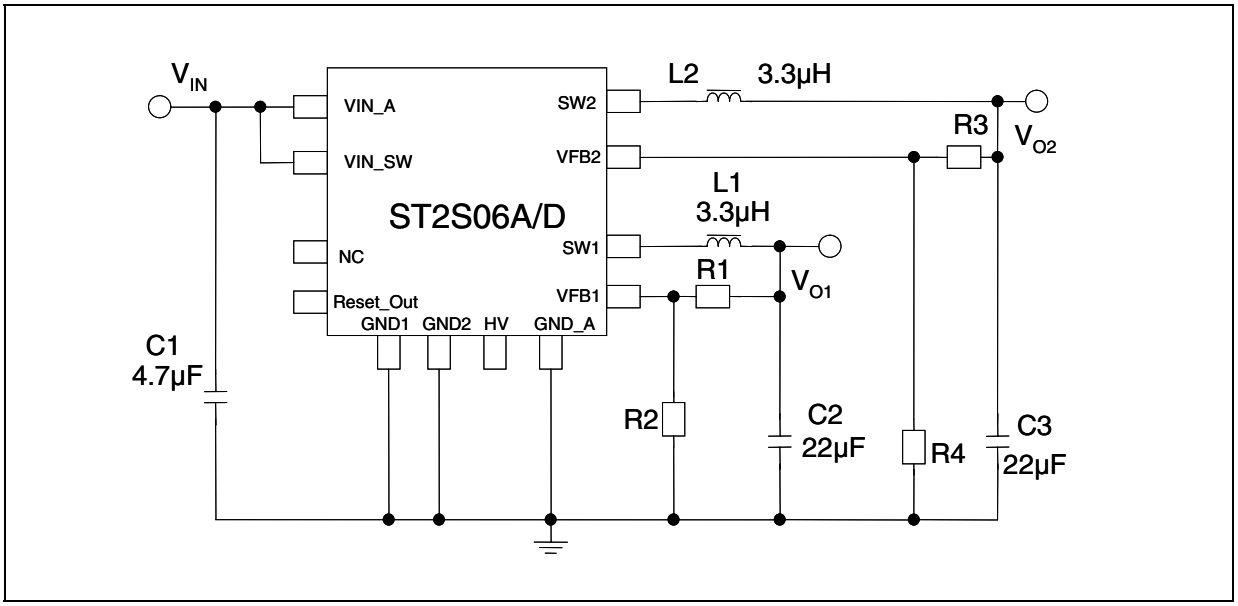
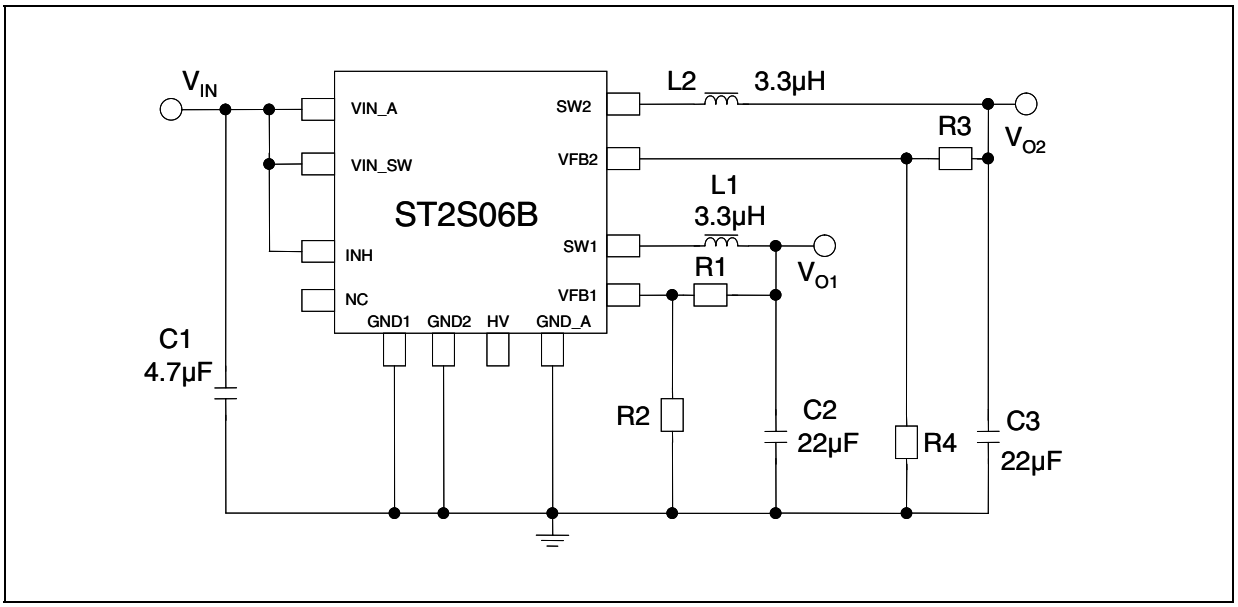


Figure 24. Application circuit for ST2S06B



7 Application information

The ST2S06 represents a series of dual adjustable current mode PWM step-down DC-DC converters with an internal 0.5 A power switch, packaged in a QFN12L (4x4 mm).

It is a complete 0.5 A switching regulator with internal compensation that eliminates the need for additional components.

The constant frequency, current mode, PWM architecture and stable operation with ceramic capacitors results in low, predictable output ripple.

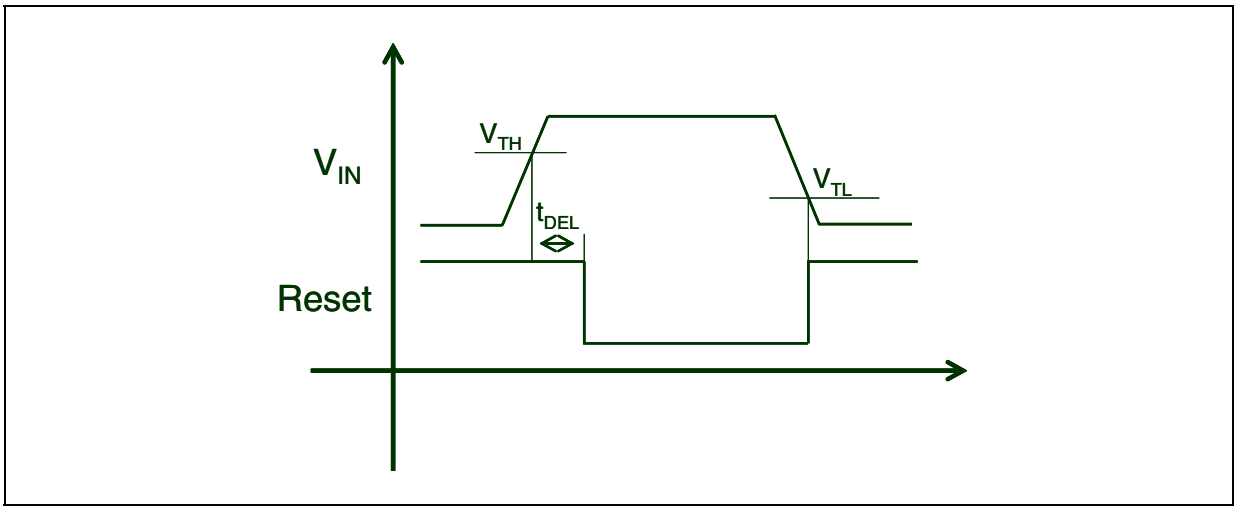
To clamp the error amplifier reference voltage a Soft Start control block generating a voltage ramp has been implemented. Other circuits fitted to the device protection are the Thermal Shut-down block, which turns off the regulator when the junction temperature exceeds 150 °C (typ.), and the cycle-by-cycle current limiting that provides protection against shorted outputs.

Because the ST2S06 is an adjustable regulator, the output voltage is determined by an external resistor divider. The desired value is given by the following equation:

$V_O = V_{FB} [1+R1/R2]$

Operation of the device requires few components: 2 inductors, 3 capacitors and a resistor divider. The chosen inductor must be capable of not saturating at the peak current level. Its value should be selected keeping in mind that a large inductor value increases the efficiency at low output current and reduces output voltage ripple, while a smaller inductor can be chosen when it is important to reduce package size and total application cost. Finally, the ST2S06 has been designed to work properly with X5R or X7R SMD ceramic capacitors both at the input and at the output. These types of capacitors, due to their very low series resistance (ESR), minimize the output voltage ripple. Other low ESR capacitors can be used according to the need of the application without compromising the correct functionality of the device. Due to the high switching frequency and peak current, it is important to optimize the application environment by reducing the length of the PCB traces and placing all the external components near the device.

Figure 25. Reset function

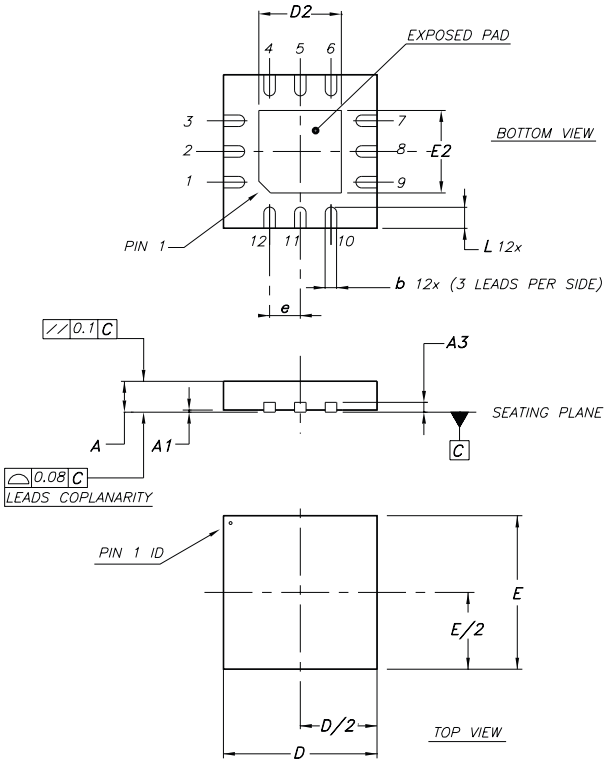


8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

QFN12L (4x4) mechanical data

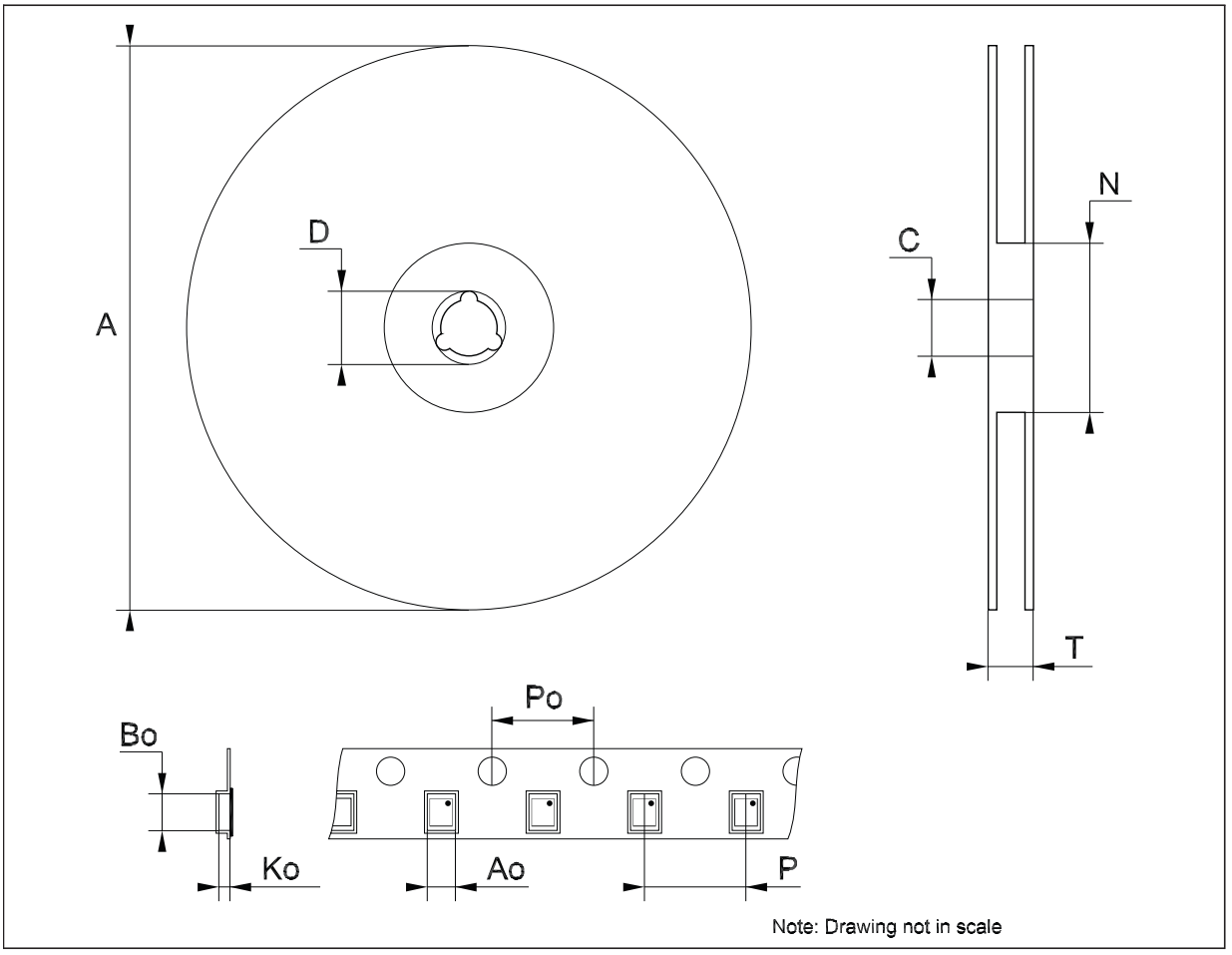
Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1		0.02	0.05		0.001	0.002
A3		0.20			0.008	
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.90	4.00	4.10	0.154	0.157	0.161
D2	2.00	2.15	2.25	0.079	0.085	0.089
E	3.90	4.00	4.10	0.154	0.157	0.161
E2	2.00	2.15	2.25	0.079	0.085	0.089
e		0.80			0.031	
L	0.45	0.55	0.65	0.018	0.022	0.026



7936361B

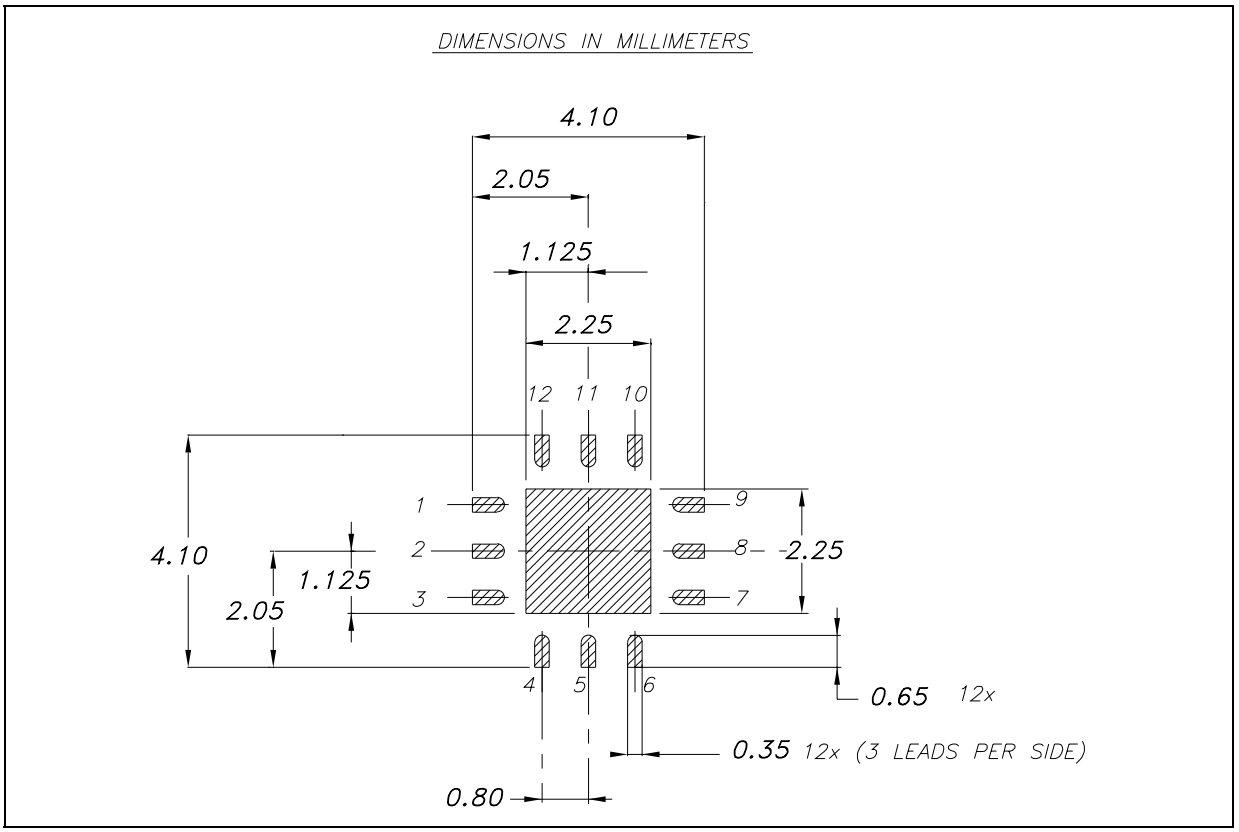
Tape & reel QFNxx/DFNxx (4x4) mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	99		101	3.898		3.976
T			14.4			0.567
Ao		4.35			0.171	
Bo		4.35			0.171	
Ko		1.1			0.043	
Po		4			0.157	
P		8			0.315	



Note: Drawing not in scale

Figure 26. QFN12L (4x4 mm) footprint recommended data



9 Revision history

Table 10. Document revision history

Date	Revision	Changes
3-Sep-2007	1	Initial release.
21-Jan-2008	2	Added root part number ST2S06D33.
18-Mar-2008	3	Modified: *Table 2 on page 4*.

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