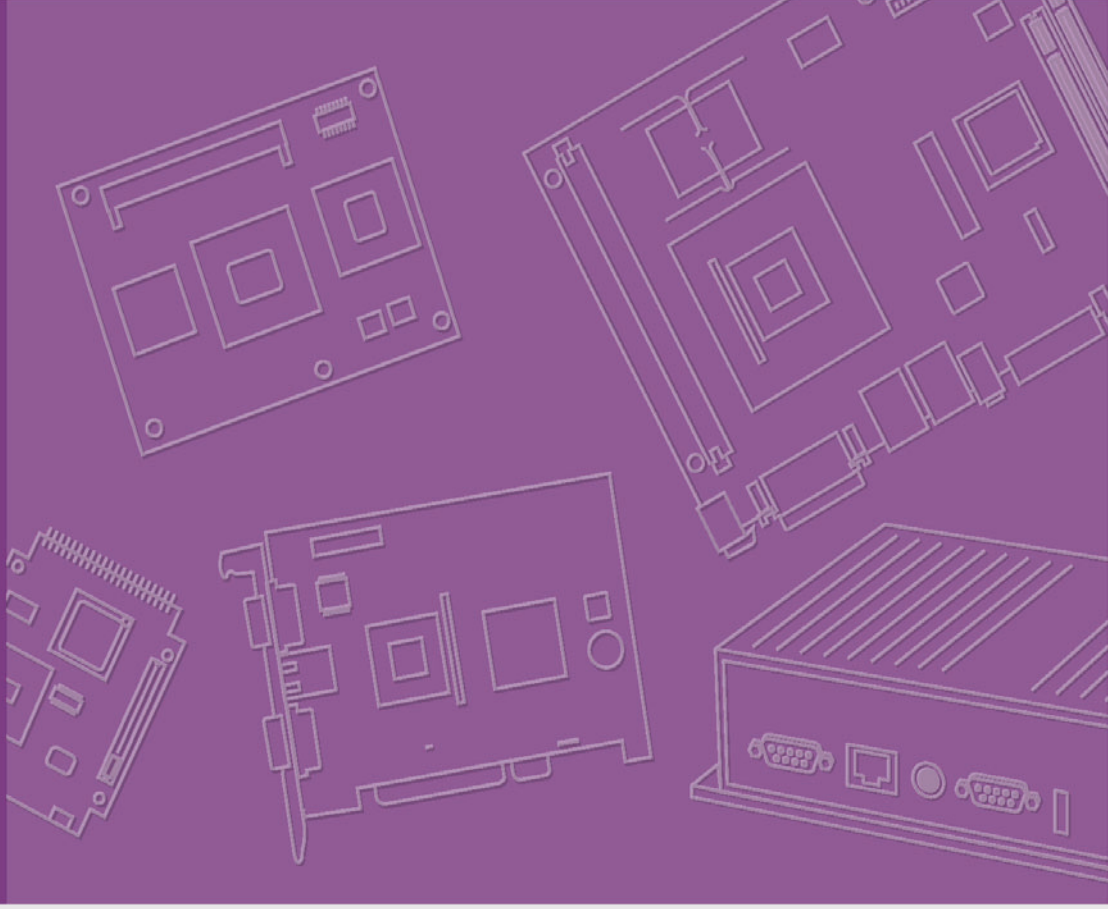

User Manual

PCM-9363

3.5" Biscuit with Intel® Atom™ N455/D525, DDR3, 24-bit LVDS, CRT or HDMI, 2 Giga LAN, Mini PCIe, 3 COM

Trusted ePlatform Services

ADVANTECH

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Technical Support and Assistance

1. Visit the Advantech web site at www.advantech.com/support where you can find the latest information about the product.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Packing List

Before installation, please ensure the following items have been shipped:

Item Part Number

- 1 PCM-9363 SBC
- 1 Startup manual
- 1 Utility CD
- 1 mini jumper pack
- Cables

Part Number	Description
1700008941	SATA cable 7P w/ Lock 32cm
1703060191	Keyboard/mouse cable 1*6P-2.0/M-DIN 6P(F)*2 19 cm
1700018839	Audio Cable 2*5P-2.0/JACK*3 20cm
1701140201	COM2 cable 14P-2.0/D-SUB 9P(M)*2 20 cm
1703100121	USB 2 PORT cable 2*5P-2.0/USB-A(F)*2 12 cm W/BKT F/10
1700260250	LPT cable 26P-2.0/D-SUB 25P(F) 25 cm
1703150102	SATA power cable B4P-5.08/SATA 15P 10 cm
1700100250	COM PORT cable 10P-2.0/D-SUB 9P(M) 25 cm

Ordering information

Model Number	Description
PCM-9363N-S6A1E	Atom N455, fanless, VGA, LVDS, 2 Giga LAN, Mini PCIe, 12 V
PCM-9363D-S8A1E	Atom D525, VGA, LVDS, 2 Giga LAN, Mini PCIe, 12 V
PCM-9363DH-S8A1E	Atom D525, HDMI, LVDS, 2 Giga LAN, Mini PCIe, 12 V

Optional accessories

Part No.	Description
1960047470N001	Heat Spreader (97 x 75 x 18.5 mm)

Certification and Safety Instructions

This device complies with the requirements in part 15 of the FCC rules: Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this device in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense. The user is advised that any equipment changes or modifications not expressly approved by the party responsible for compliance would void the compliance to FCC regulations and therefore, the user's authority to operate the equipment.

Caution! *There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

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Chapter 1

General Introduction

This chapter gives background information on the PCM-9363.

Sections include:

- Introduction
- Product feature
- Specifications

1.1 Introduction

PCM-9363 is a 3.5" SBC (Single Board Computer) with Embedded Intel® Atom™ N455 1.66 GHz/D525 1.8 GHz Processor. The PCM-9363 can support DDR3 memory up to 4 GB for D525, has six USB 2.0 compatible ports, two Giga-LAN (1000Mbps) interface, LVDS and VGA support, with HDMI (optional), HD (High Definition) audio, and one Mini-PCIe expansion slot. In addition, PCM-9363 also supports two SATA drives, three COM ports and one CF slot.

1.2 Product Feature

General

- **CPU:** Intel® Atom™ processor N455 1.66 GHz/D525 1.8 GHz
- **System Chipset** Intel® Atom™ N455/D525 + ICH8M
- **BIOS:** AMI 16 Mbit Flash BIOS
- **System Memory:** DDR3 800 MHz N455 up to 2 GB, D525 up to 4 GB
- **CFC:** Supports CompactFlash® Card TYPE I/II
- **Watchdog Timer:** Single chip Watchdog 255-level interval timer, setup by software
- **Expansion Interface:** Supports 1 x Mini-PCIe device
- **Battery:** Lithium 3 V/220 mAH

I/O

- **I/O Interface:** 2 x SATA (300 MB/S), 1 x KB/mouse (internal), 2 x RS232, 1 x RS232/422/485, 1 x LPT
- **USB:** 6 x USB 2.0 compliant Ports
- **Audio:** High Definition Audio (HD), Line-in, Line out, Mic-in
- **GPIO:** 8-bit general purpose input/output

Ethernet

- **Chipset:** LAN1 Intel® 82567V, LAN2 Intel 82583V
- **Speed:** 1000 Mbps
- **Interface:** 2 x RJ45
- **Standard:** Compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3x, IEEE 8023y, IEEE 802.ab.

Display

- **Chipset:** Embedded Gen3.5+ GFX Core
- **Memory Size:** Up to 224 MB of dynamic video memory allocation
- **Resolution:**
  - CRT: Intel® Atom™ N455 up to 1400 x 1050 (SXGA), D525 up to 2048 x 1536
  - LVDS: Single channel 24-bit LVDS up to WXGA 1366 x 768
  - HDMI: 1080P and scale function, support Hot Plug Detection (HPD)
- **LVDS LCD:** Supports 18 or 24-bit LVDS LCD
- **Dual Display:**
  - CRT + LVDS (18 or 24 bit)

1.3 Specifications

1.3.1 Functional Specification

Processor

Processor	■ Intel® Atom™ Processor N455/D525 ■ Intel® Atom™ N455 at 1.66 GHz with 512KB L2 cache / D525 at 1.8 GHz with 1MB L2 cache ■ Manufacturing Technology:45 nm

Chipset (Intel® N455/D525)

Memory	■ Intel® N455/D525 ■ Supports DDR3 800 MHz up to 2 GB for N455, D525 up to 4 GB ■ SODIMM Socket: 204-pin SODIMM socket type *1
Graphic and Video Controllers	Intel 3.5 Gen Integrated Graphic Engine + GFX core ■ DVMT 3.0 (Dynamic Video Memory Technology) ■ Directx* 9 compliant Pixel Shader 2.0 ■ 2 display ports: LVDS and RGB ■ Intel® Clear Video Technology

Chipset (ICH8M)

IDE Interface	■ ICH8M ■ Supports one CF device
H.D. Codec ALC892 I/F	ICH8M supports: ■ Support for HD codec ■ Up to 2.1 channel of PCM audio output ■ Connectors: Line-out, Line-in, Mic-in: Pin header 2*5P (M) 2.0 mm
Concurrent PCI/PCIe Bus Controller	ICH8M chip supports: ■ PCI 2.3 ■ Support one mini PCIe connector
SATA Connector	ICH8M supports: ■ Independent DMA operation on two ports ■ Data transfer rates of up to 3.0 Gb/s (300 MB/s) ■ Operation of AHCI using memory space ■ Several optional sections of the Serial ATA II ■ SATA connectors: ■ Connector: Serial ATA II 7 pins 1.27 mm x 2
USB Interface	ICH8M supports: ■ 6 USB 2.0 ports which are high-speed, full- speed, and low-speed capable ■ USB Connector:(USB1~4) 2 set 5 x 2-pin Hirose DF13 type
Power Management	■ Full ACPI (Advanced Configuration and Power Interface) 2.0 ■ Supports S0, S1, S3,S4, S5
BIOS	AMI 16Mb Flash BIOS via SPI

Other Chipset

Graphic and Video Controllers	Intel 3.5 Gen Integrated Graphic Engine + GFX core ■ CRT: Intel Atom N455 up to 1400 x 1050 (SXGA) Intel Atom D525 up to 2048 x 1536 ■ LVDS: Single channel 24-bit LVDS up to WXGA 1366 x 768 LVDS connector: Hirose DF13 type 20 pin CRT connector: D-SUB15 at coastline ■ HDMI: 1080P and scale function, support Hot Plug Detection (HPD)
LAN	LAN1 Intel 82567V, LAN2 Intel 82583V ■ Compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3x, IEEE 8023y, IEEE 802.ab. ■ Support 1000Mbps. Connectors: Phone Jack RJ45 8P 90D(F)
Serial ports	SMSC SCH 3114 support ■ 3 full function serial ports by SMSC SCH 3114. ■ High Speed NS16C550A Compatible UARTs with Data rates to 1.5Mbps. ■ Support IRQ Sharing among serial ports. Connectors: COM1: (RS-232) 1x DB9 at coastline, 1 x 2.0 mm box header COM2: (RS-232/422/485) 1 x 2.0 mm box header
Keyboard/Mouse connectors	SMSC SCH 3114 support PS/2 Keyboard and Mouse interface. Connector: Box header 6P 2.0 mm
GPIO	SMSC SCH 3114 support ■ 8 I/O Pins. ■ 5V tolerance I/Os. Connectors: 10 pins 2.0mm pin header.
Battery backup	2 pin wafer box for external Battery on board

1.3.2 Mechanical Specifications

1.3.2.1 Dimensions (mm)

AT/ATX: L146.00 mm * W102 mm

1.3.2.2 Height on top (mm)

24.4 mm (heatsink with fan for D525 SKU)

20 mm (heatsink without fan for N455 SKU)

1.3.2.3 Height under bottom (mm)

9.00 mm (CF Socket)

1.3.2.4 Weight (g) with Heatsink

110 g (heatsink with fan for D525 SKU)

88 g (heatsink without fan for N455 SKU)

1.3.3 Electrical Specifications

1.3.3.1 Power supply Voltage

AT/ATX: +12 V_{DC} ± 5%

1.3.3.2 Power Supply Current

- **Typical in XP mode:**
  N455/DDR3 1GB : 0.74 A, 12 V
  D525/DDR3 1GB : 0.86 A, 12 V
- **Max in HCT:**
  N455/DDR3 1GB : 0.86 A, 12 V
  D525/DDR3 1GB : 1.18 A, 12 V

1.3.3.3 RTC Battery

- **Typical Voltage:** 3.0 V
- **Normal discharge capacity:** 220 mAh

1.4 Environmental Specifications

1.4.1 Operating Humidity

- **Operating humidity:**10% ~ 90% Relative Humidity, non-condensing

1.4.2 Operating Temperature

- **Operating temperature:** 0 ~ 60° C (32~140°F)

1.4.3 Storage Humidity

Standard products (0 ~ 60° C)

- **Relative humidity:** 95% @ 60° C

1.4.4 Storage Temperature

Standard products (0 ~ 60° C)

- **Storage temperature:** -20~70° C

Chapter 2

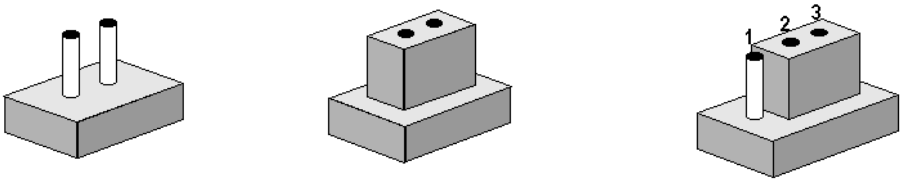
H/W Installation

This chapter explains the setup procedures of the PCM-9363 hardware, including instructions on setting jumpers and connecting peripherals, as well as switches, indicators and mechanical drawings. Be sure to read all safety precautions before you begin the installation procedure.

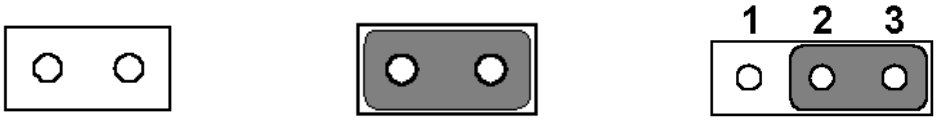
2.1 Jumpers

2.1.1 Jumper Description

Cards can be configured by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To close a jumper, you connect the pins with the clip. To open a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2, or 2 and 3.



The jumper settings are schematically depicted in this manual as follows.



A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

Generally, you simply need a standard cable to make most connections.

Warning! *To avoid damaging the computer, always turn off the power supply before setting jumpers. When clearing CMOS, before turning on the power supply, set the jumper back to 3.0 V Battery On.*

2.1.2 Jumper list

Table 2.1: Jumper List	
J2	COM2 Setting
J3	AT / ATX Power SEL
J4	Clear CMOS
J5	Panel Voltage SEL

2.1.3 Jumper Settings

Table 2.2: J2: COM2 Setting	
Part Number	1653003260
Footprint	HD_3x2P_79
Description	PIN HEADER 3*2P 180D(M) 2.0mm SMD SOUARE PIN
Setting	**Function**
(1-2) (default)	RS232
(3-4)	RS485
(5-6)	RS422

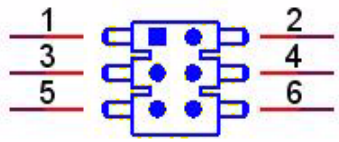


Table 2.3: J3: AT / ATX Power SEL	
Part Number	1653002101
Footprint	HD_2x1P_79_D
Description	PIN HEADER 2*1P 180D(M)SQUARE 2.0mm DIP W/O Pb
Setting	**Function**
(1-2) (default)	AT Power SEL
EMPTY	ATX Power

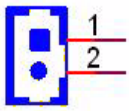


Table 2.4: J4: Clear CMOS	
Part Number	1653003101
Footprint	HD_3x1P_79_D
Description	PIN HEADER 3*1P 180D(M) 2.0mm DIP SQUARE W/O Pb
Setting	**Function**
(1-2) (default)	Normal
(2-3)	Clear CMOS

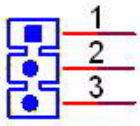
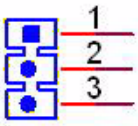


Table 2.5: J5: PAN VOL SEL	
Part Number	1653003101
Footprint	HD_3x1P_79_D
Description	PIN HEADER 3*1P 180D(M) 2.0mm DIP SQUARE W/O Pb
Setting	**Function**
(1-2)	+5V
(2-3) (default)	+3V



2.2 Connectors

2.2.1 Connector list

Table 2.6: Connector list	
CN1	Audio
CN2	SATA
CN3	SATA
CN4	GPIO
CN5	HDD & PWR LED
CN6	12 V Power Input
CN8	COM3
CN10	PS2
CN11	SMBus
CN12	COM2
CN13	Inverter Power Output
CN14	Internal USB
CN15	Internal USB
CN16	18 or 24 bits LVDS Panel
CN17	Single LAN (Optional to replace Dual LAN)
CN18	LAN1
CN19	LAN2
CN20	Power Switch (Low Active)
CN21	LPT
CN22	HDMI (Optional)
CN23	Reset
CN24	External USB
CN25	External USB
CN26	COM1
CN27	VGA
CN28	Mini PCIE lock
CN29	Mini PCIE slot
CN30	DDR3 SODIMM
CN31	BIOS Socket
CN32	CF
CN36	SATA Power

2.2.2 Connector Settings

2.2.2.1 Audio Interface (CN1)

Audio Port Connectors

One 5 x 2 pin box header for Audio connector. These audio connectors are used for audio devices. The audio jacks are differentiated by color for different audio sound effects.

2.2.2.2 SATA Connector (CN2, CN3)

PCM-9363 supports Serial ATA via two connectors (CN2, CN3). Data transfer rates up to 300 MB/s are possible, enabling very fast data and file transfer, and independent DMA operation on two ports.

2.2.2.3 GPIO (General Purpose Input Output) (CN4)

The board supports 8-bit GPIO through GPIO connector. The 8 digital in and out-puts can be programmed to read or control devices, with input or out- put defined. The default setting is 4 bits input and 4 bits output.

2.2.2.4 Power & HDD LED Indicator (CN5)

The HDD LED indicator for hard disk access is an active low signal (24 mA sink rate). Power supply activity LED indicator.

2.2.2.5 Power Reset Button (CN23)

Momentarily pressing the reset button will activate a reset. The switch should be rated for 10 mA, 5 V.

2.2.2.6 Power Connectors

Main power connector (CN6)

PCM-9363 supports single 12 V input.

2.2.2.7 COM Port Connector (CN8, CN12,CN26)

The PCM-9363 provides 3 serial ports (COM1 & COM3: RS-232; COM2: RS-232/422/485) in one DB-9 connector (CN26) for COM1 and one 7*2P pin header (CN12) for COM2 and one 5*2P pin header (CN8) for COM3. It provides connections for serial devices (a mouse, etc.) or a communication network. You can find the pin assignments for the COM port connector in Appendix A.

COM RS-232/422/485 setting (J2)

COM2 can be configured to operate in RS-232, RS-422, or RS-485 mode.

This is done via J2.

J2	COM2 Setting
Setting	**Function**
(1-2) (default)	RS232
(3-4)	RS485
(5-6)	RS422

2.2.2.8 Keyboard and PS/2 Mouse Connector (CN10)

The board provides a keyboard connector that supports both a keyboard and a PS/2 style mouse. In most cases, especially in embedded applications, a keyboard is not used. If the keyboard is not present, the standard PC/AT BIOS will report an error or fail during power-on self-test (POST) after a reset. The product's BIOS standard setup menu allows you to select "All, But Keyboard" under the "Halt On" selection.

This allows no-keyboard operation in embedded system applications, without the system halting under POST.

2.2.2.9 SMBus Connector (CN11)

The System Management Bus (abbreviated to SMBus or SMB) is a simple two-wire bus, derived from I^2C and used for communication with low-bandwidth devices on a motherboard, especially power related chips such as a laptop's rechargeable battery subsystem (see Smart Battery Data). Other devices might include temperature, fan or voltage sensors, lid switches and clock chips. PCI add-in cards may connect to a SMBus segment.

The SMBus was defined by Intel in 1995. It carries clock, data, and instructions and is based on Philips' I^2C serial bus protocol. Its clock frequency range is 10 kHz to 100kHz. Its voltage levels and timings are more strictly defined than those of I^2C, but devices belonging to the two systems are often successfully mixed on the same bus.

2.2.2.10 Inverter Power Connector (CN13)

PCM-9363 can provide +5 V and +12 V and signal to LCD inverter board via CN13.

2.2.2.11 USB Connectors (CN14, CN15, CN24, CN25)

The board provides up to six USB (Universal Serial Bus) ports. This gives complete Plug and Play, and hot attach/detach for up to 127 external devices. The USB interfaces comply with USB specification Rev. 2.0 which supports 480 Mbps transfer rate, and are fuse protected.

There are 5 x 2 pin 180D (M) connectors for internal use, 4 x USB ports at CN14, CN15 and two external USB port at CN24,CN25. You will need an adapter cable if you use a standard USB connector. On one end the adapter cable has a 5 x 2-pin connector with a foolproof connection to prevent it from being plugged in the wrong way and on the other end a USB connector.

2.2.2.12 VGA/LCD/LVDS Interface Connections

The board's PCI VGA interface can drive conventional CRT displays and is capable of driving a wide range of flat panel displays, including passive LCD and active LCD displays. The board has connectors to support these displays: one for standard CRT VGA monitors and one for flat panel displays

CRT display connector (CN27)

The CRT display connector is a box header connector used for conventional CRT displays.

LVDS LCD panel connector (CN16)

The board supports 18 or 24 bit LVDS LCD panel displays. Users can connect to a 18 or 24 bit LVDS LCD on it.

HDMI panel connector (CN22)

HDMI panel connector is optional for PCM-9363DH-S8A1E. It supports FHD resolution 1080P LCD panel.

2.2.2.13 Ethernet Configuration (CN18, CN19)

10/100/1000 Mbps connections are made via RJ-45 connectors.

The board is equipped with 2 high performance PCI Ethernet interface which is fully compliant with IEEE 802.3u 100Base-T & IEEE 802.3ab 1000Base-T. It is supported by all major network operating systems.

2.2.2.14 Power Switch Connector (CN20)

One 2 x 1 pin wafer box (CN20) for power switch. If for ATX using, please remove J3 jumper and connect to power button via CN20.

2.2.2.15 LPT Connector (CN21)

PCM-9363 can support LPT via CN21. LPT (Line Print Terminal) is the original, yet still common, name of the parallel port interface on IBM PC-compatible computers. It was designed to operate a text printer that used IBM's 8-bit extended ASCII character set.

2.2.2.16 Mini PCIe Connector (CN28,CN29)

PCI Express Mini Card (also known as Mini PCI Express, Mini PCIe, and Mini PCI-E) is a replacement for the Mini PCI form factor based on PCI Express. It is developed by the PCI-SIG. The host device supports both PCI Express and USB 2.0 connectivity, and each card uses whichever the designer feels most appropriate to the task.

PCM-9363 support a Mini PCIe slot.

2.2.2.17 DDRIII DIMM Socket (CN30)

One 204-pin/H6.5 mm DDRIII DIMM socket (CN30) supports DDRIII 800 MHz up to 2 GB for N455, and D525 up to 4 GB.

2.2.2.18 CompactFlash (CN32)

PCM-9363 provides a CompactFlash card type I/II socket.

The CompactFlash card shares a secondary IDE channel which can be enabled/disabled via the BIOS settings.

Compact Flash set as fix master mode.

2.2.2.19 SATA Power (CN36)

SATA Power supports 5 V and 12 V output, 500 mA each.

2.3 Mechanical

2.3.1 Jumper and Connector Locations

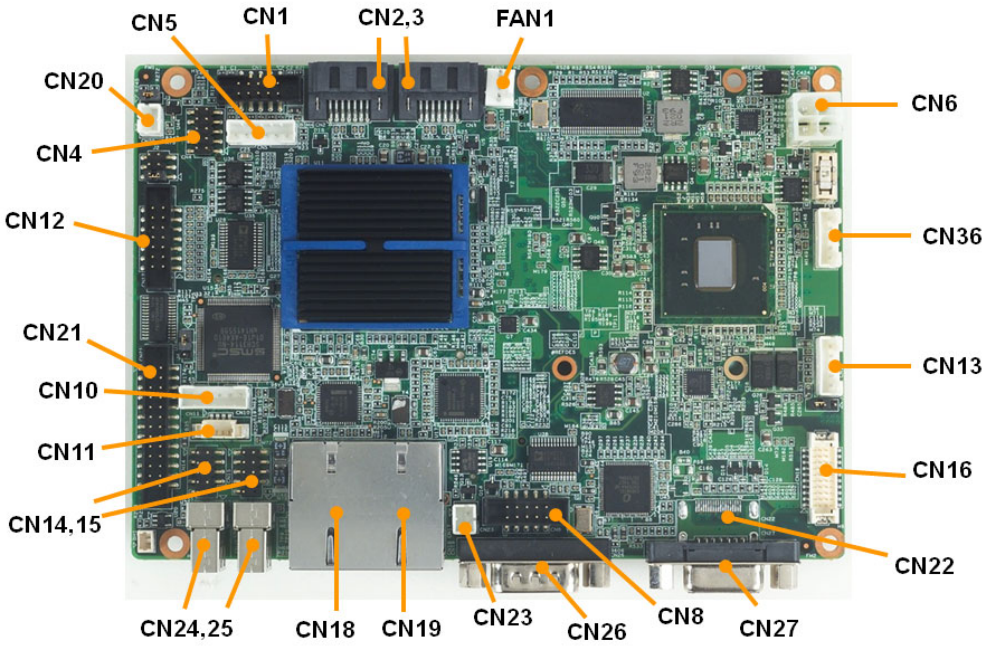


Figure 2.1 Jumper and Connector layout (component side)

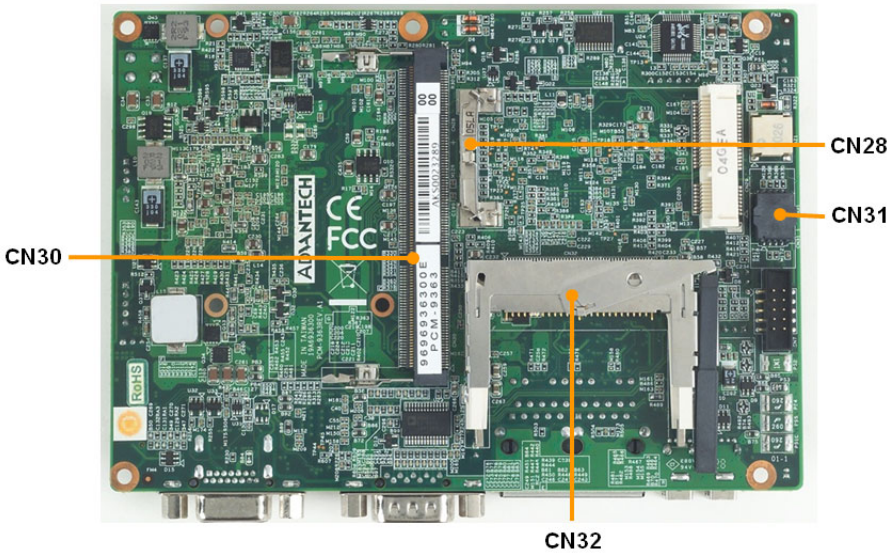


Figure 2.2 Jumper and connector layout (solder side)

2.3.2 Board Dimensions

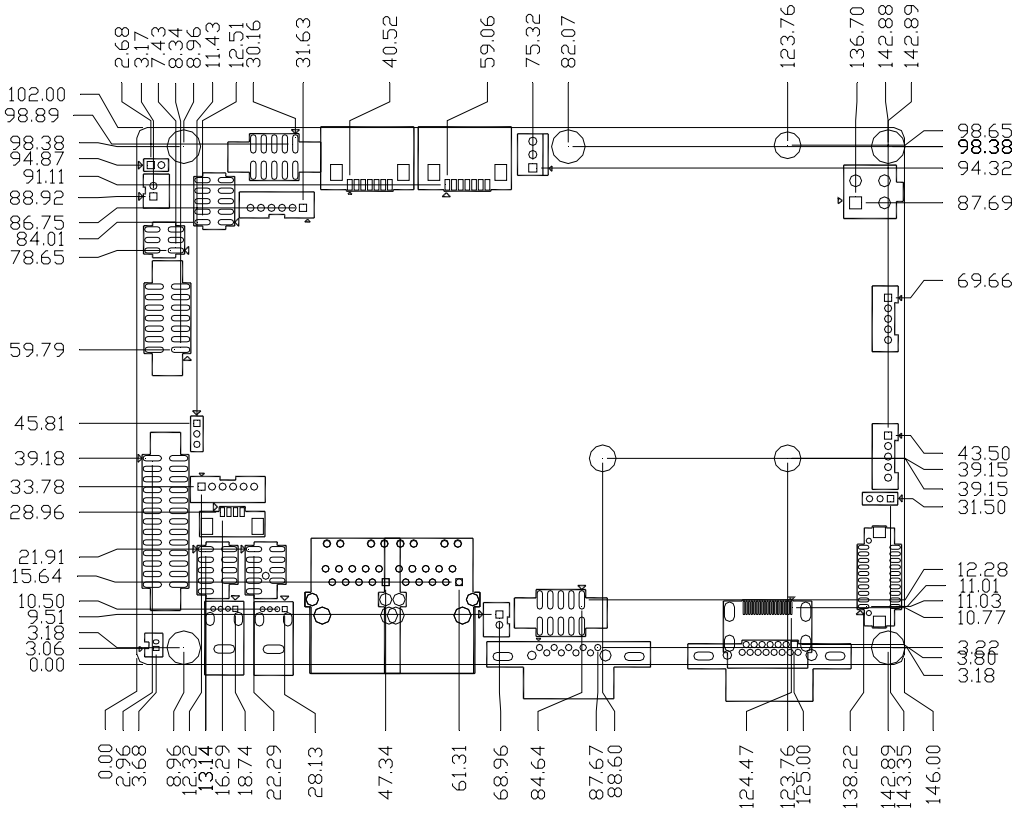


Figure 2.3 Board dimension layout (component side)

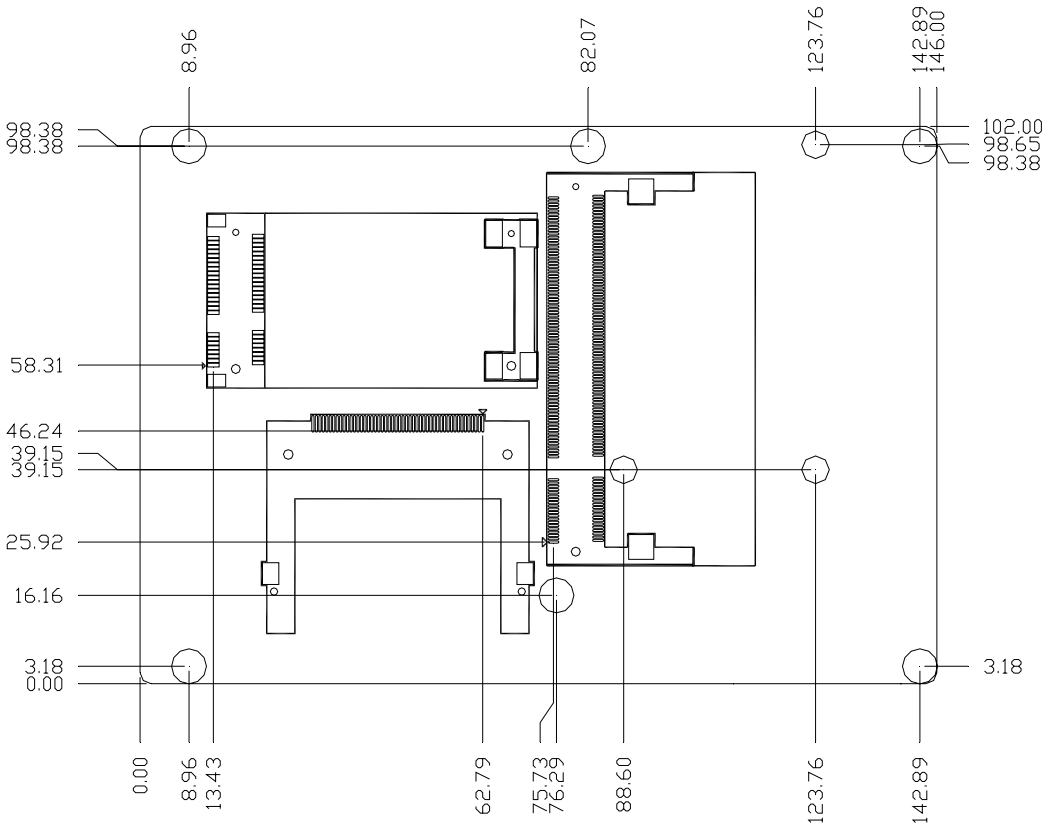


Figure 2.4 Board dimension layout (solder side)

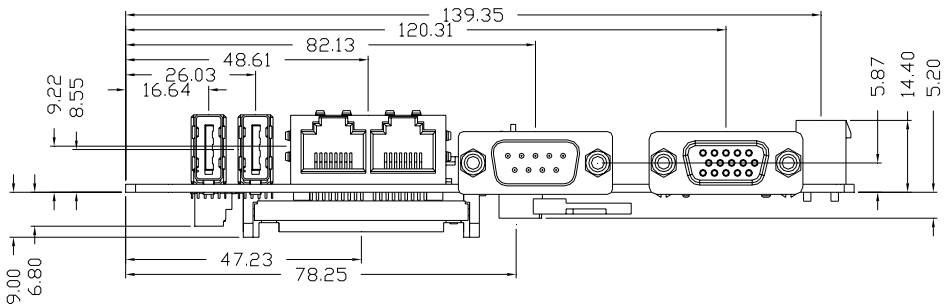


Figure 2.5 Board dimension layout (coastline)

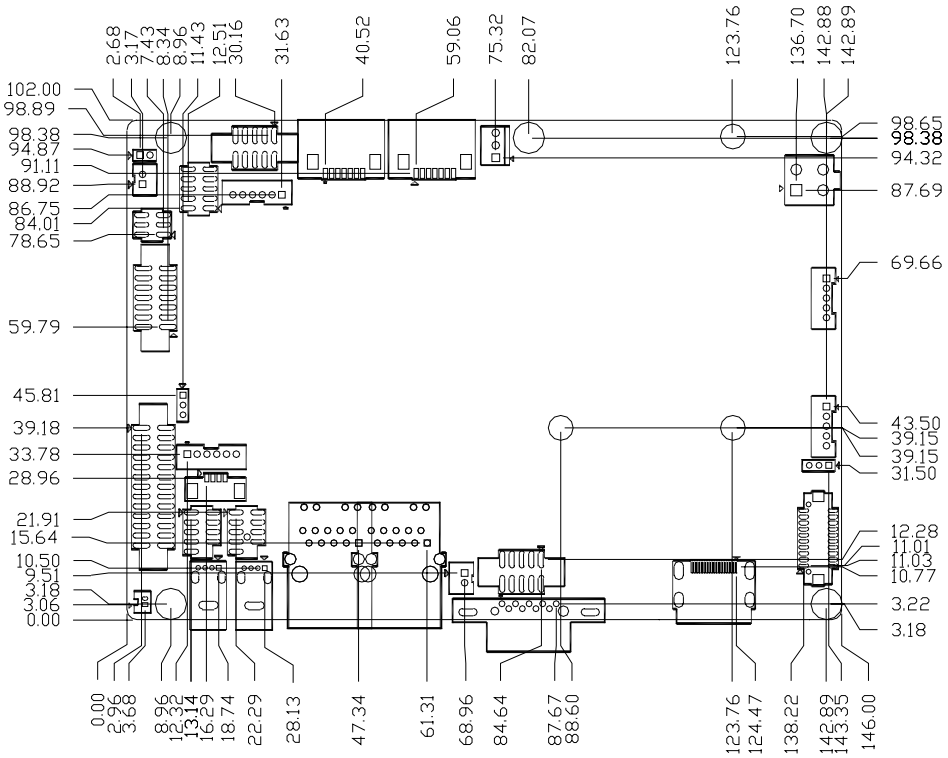


Figure 2.6 PCM-9363 HDMI mechanical drawing (top View)

Chapter 3

BIOS settings

3.1 Introduction

AMIBIOS has been integrated into a slew of motherboards for over two decades. With the AMIBIOS Setup program, you can modify BIOS settings and control the various system features. This chapter describes the basic navigation of the PCM-9363 BIOS setup screens.

AMI's BIOS ROM has a built-in setup program that allows users to modify the basic system configuration. This information is stored in battery-backed CMOS so it retains the setup information when the power is turned off.

3.2 Entering Setup

Turn on the computer and check for the “patch" code. If there is a number assigned to the patch code, it means that the BIOS supports your CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that your CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press <DEL> and you will immediately be allowed to enter setup.

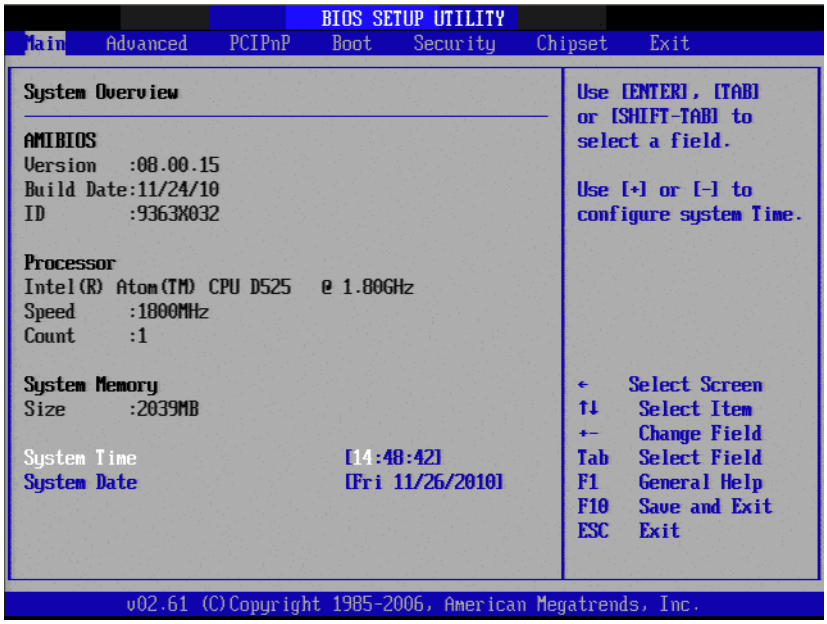


Figure 3.1 Setup program initial screen

3.2.1 Main Setup

When you first enter the BIOS Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.

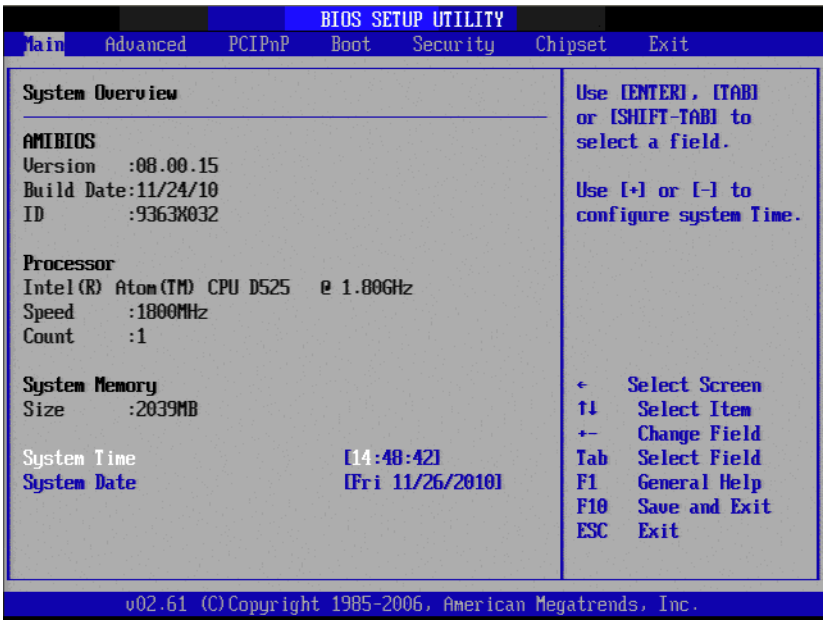


Figure 3.2 Main setup screen

The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

3.2.1.1 System Time / System Date

Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

3.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the PCM-9363 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub menus are described on the following pages.

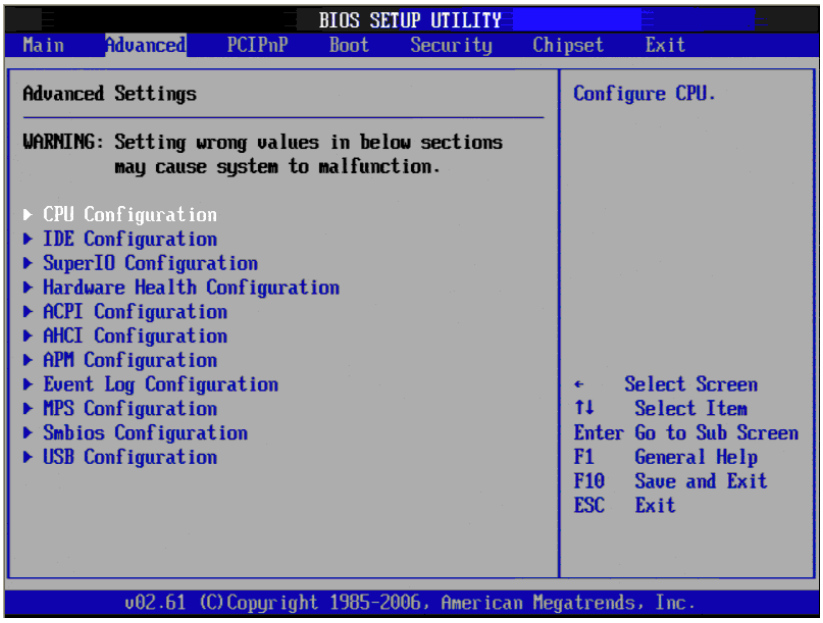


Figure 3.3 Advanced BIOS features setup screen

3.2.2.1 CPU Configuration

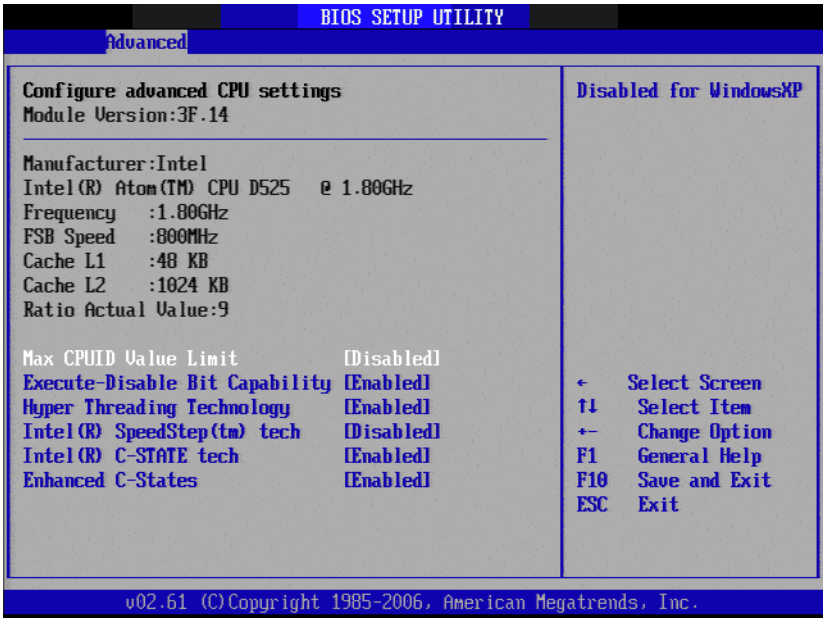


Figure 3.4 CPU Configuration Setting

- **Max CPUID Value Limit**
  This item allows you to limit CPUID maximum value.
- **Execute-Disable Bit Capability**
  This item allows you to enable or disable the No-Execution page protection technology.
- **Hyper Threading Technology**
  This item allows you to enable or disable Intel® Hyper Threading technology.
- **Intel® SpeedStep® tech**
  When set to disabled, the CPU runs at its default speed, when set to enabled, the CPU speed is controlled by the operating system.
- **Intel® C-STATE tech**
  This item allows the CPU to save more power under idle mode.
- **Enhanced C-States**
  CPU idle set to enhanced C-States, disabled by Intel® C-STATE tech item.

3.2.2.2 IDE Configuration

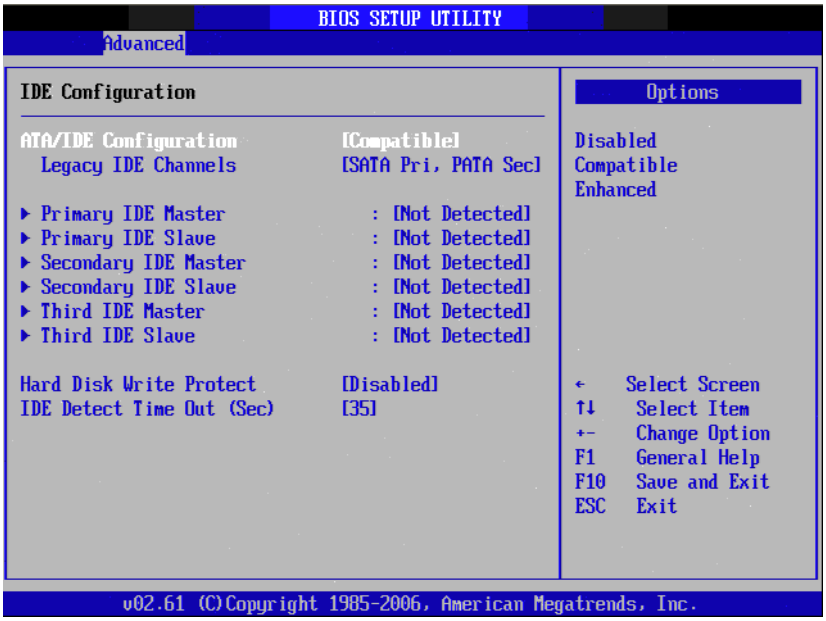


Figure 3.5 IDE Configuration

- **ATA/IDE Configuration**

  This item allows you to select Disabled / Compatible / Enhanced.

- **Legacy IDE Channels**

  When set to Enhanced mode you can select IDE or AHCI mode. When select Compatible mode you can select SATA only; SATA pri, PATA sec; or PATA only.

- **Primary/Secondary/Third IDE Master/Slave**

  BIOS auto detects the presence of IDE device, and displays the status of auto detection of IDE device.

  - **Type:** Select the type of SATA driver.[Not Installed][Auto][CD/DVD][ARMD]
  - **LBA/Large Mode:** Enables or Disables the LBA mode.
  - **Block (Multi-Sector Transfer):** Enables or disables data multi-sectors transfers.
  - **PIO Mode:** Select the PIO mode.
  - **DMA Mode:** Select the DMA mode.
  - **S.M.A.R.T.:** Select the smart monitoring, analysis, and reporting technology.
  - **32Bit Data Transfer:** Enables or disables 32-bit data transfer.

- **Hard Disk Write Protect**

  Disable/Enable device write protection. This will be effective only if the device is accessed through BIOS.

- **IDE Detect Time Out (Sec)**

  This item allows you to select the time out value for detecting ATA/ATAPI device(s).

3.2.2.3 Super I/O Configuration

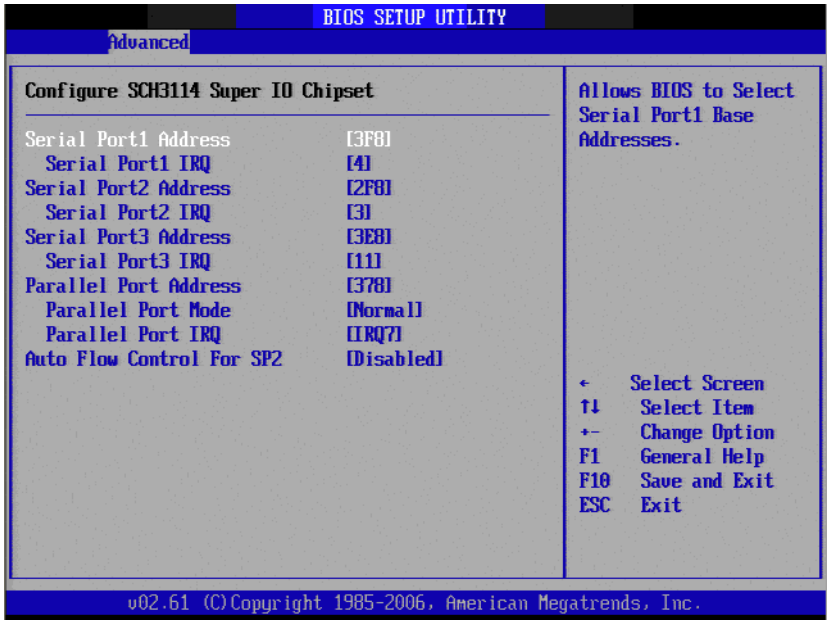


Figure 3.6 Super I/O Configuration

- **Serial Port1 / Port2 / Port3 / Port 4 address**
  This item allows you to select serial port1 ~ port4 base addresses.
- **Serial Port1 / Port2 / Port3 / Port 4 IRQ**
  This item allows you to select serial port1 ~ port4 IRQs.
- **Parallel Port Address**
  This item allows you to select parallel port base address.
- **Parallel Port Mode**
  This item allows you to select parallel port mode.
- **Parallel Port IRQ**
  This item allows you to select parallel port IRQ.
- **Auto Flow Control For SP2**
  This item allows you to enable or disable auto flow control.

3.2.2.4 Hardware Health Configuration

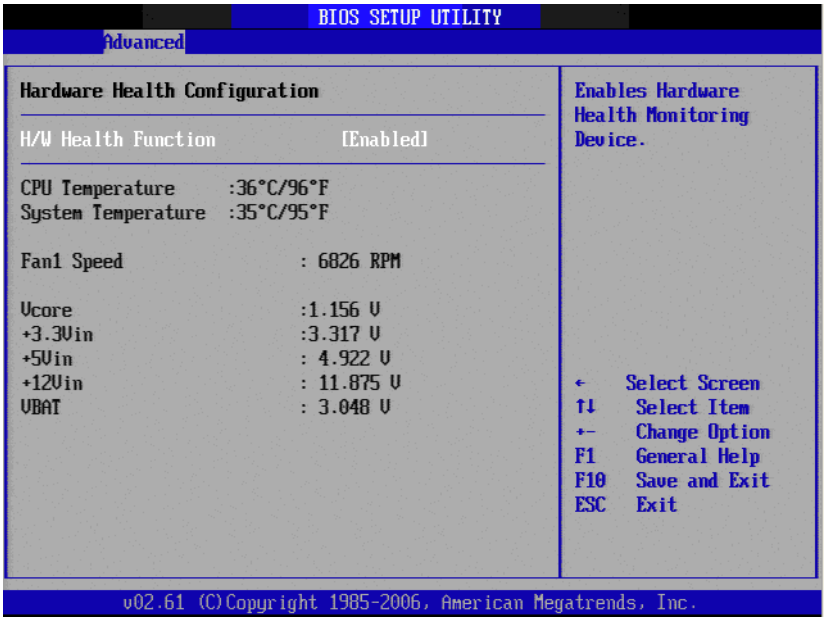


Figure 3.7 Hardware health configuration

- **H/W Health Function**
  This item allows you to control H/W monitoring.
- **Temperature & Voltage show**
  CPU/System Temperature
  Vcore / +3.3 Vin / +5 Vin / +12 Vin / VBAT
- **Fan1 Speed show**
  Display Fan1 Speed RPM.

3.2.2.5 ACPI Settings

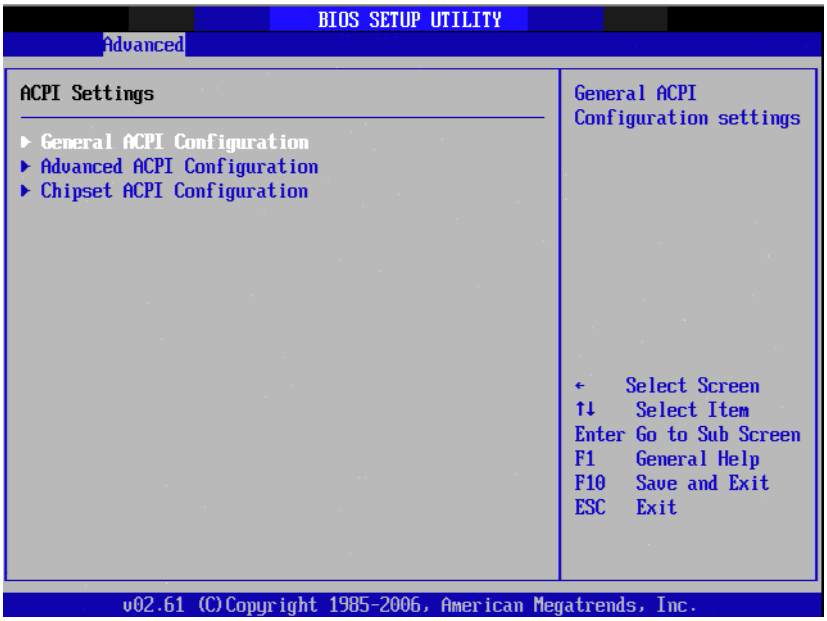


Figure 3.8 ACPI Settings

- **General ACPI Configuration**

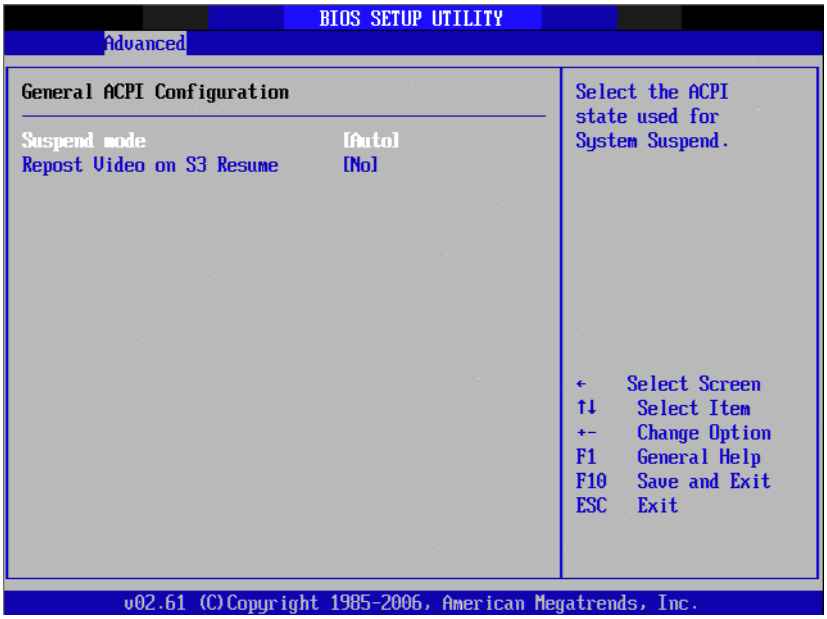


Figure 3.9 General ACPI Configuration

– **Suspend mode**
Select the ACPI state used for system suspend.

– **Report Video on S3 Resume**
This item allows you to invoke VA BIOS POST on S3/STR resume.

Advanced ACPI Configuration

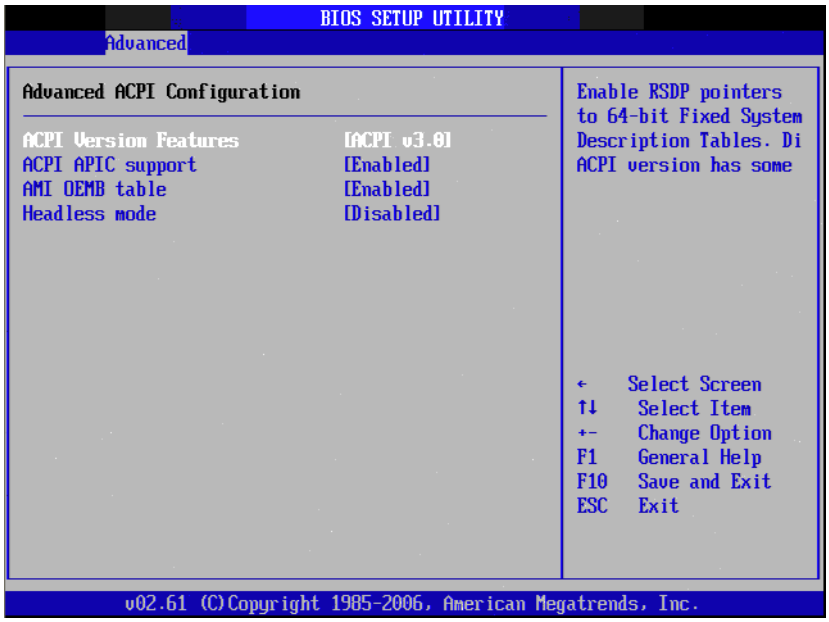


Figure 3.10 Advanced ACPI Configuration

- **ACPI Version Features**
  This item allows you to enable RSDP pointers to 64-bit fixed system description tables.
- **ACPI APIC support**
  Include APIC table pointer to RSDT pointer list.
- **AMI OEMB table**
  Include OEMB table pointer to R(x)SDT pointer lists.
- **Headless mode**
  Enable / Disable Headless operation mode through ACPI.

Chipset ACPI Configuration

Figure 3.11 Chipset ACPI Configuration

– **Energy Lake Feature**
  Allows you to configure Intel's Energy Lake power management technology.
– **APIC ACPI SCI IRQ**
  Enable/Disable APIC ACPI SCI IRQ.
– **USB Device Wakeup From S3**
  Enable/Disable USB Device Wakeup from S3.
– **High Performance Event Timer**
  Enable/Disable High performance Event timer.

3.2.2.6 AHCI Configuration

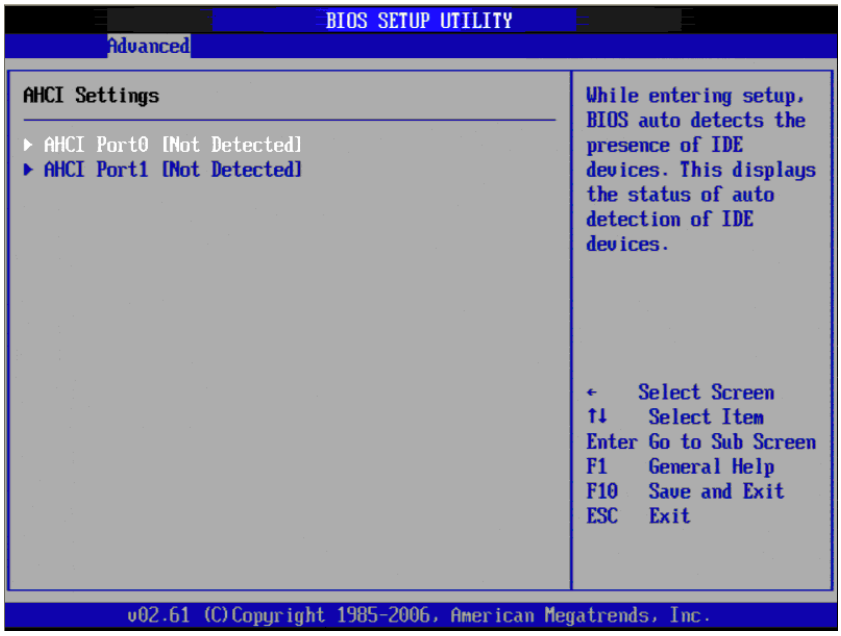


Figure 3.12 AHCI Configuration

■ **AHCI Port0 / Port1**
  While entering setup, BIOS auto detects the presence of IDE devices. This displays the status of auto detection of IDE device.

3.2.2.7 APM Configuration

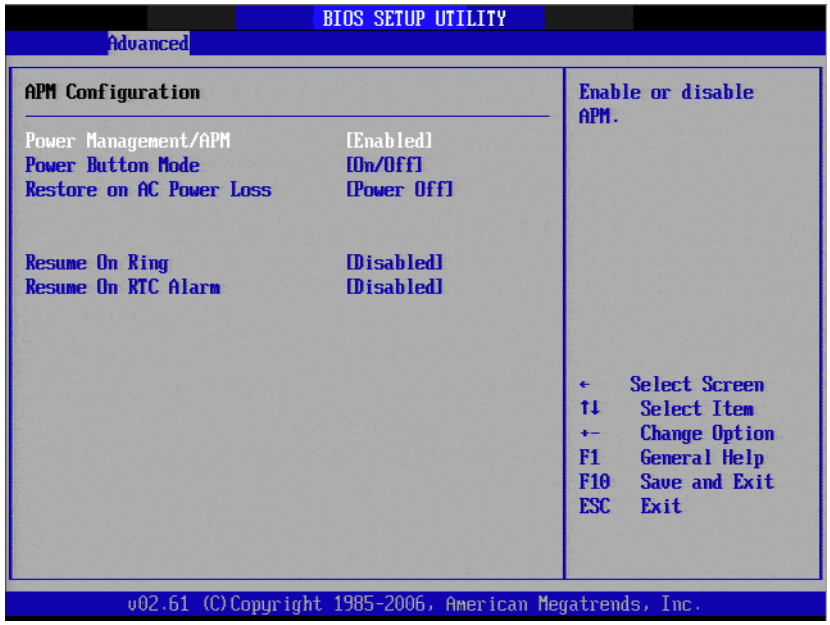


Figure 3.13 APM Configuration

- **Power Management/APM**
  Enable or disable APM.
- **Power Button Mode**
  Power on, off, or enter suspend mode when the power button is pressed. The following options are also available.
- **Restore on AC power Loss**
  Use this to set up the system response after a power failure. The "Off" setting keeps the system powered off after power failure, the “On” setting boots up the system after failure, and the "Last State" returns the system to the status just before power failure.
- **Video Power Down Mode**
  Power down video in suspend or standby mode.
- **Hard Disk Power Down Mode**
  Power down Hard Disk in suspend or standby mode.
- **Resume On Ring**
  Enable / Disable RI to generate a wake event.
- **Resume On RTC Alarm**
  Enable / Disable RTC to generate a wake event.

3.2.2.8 Event Log Configuration

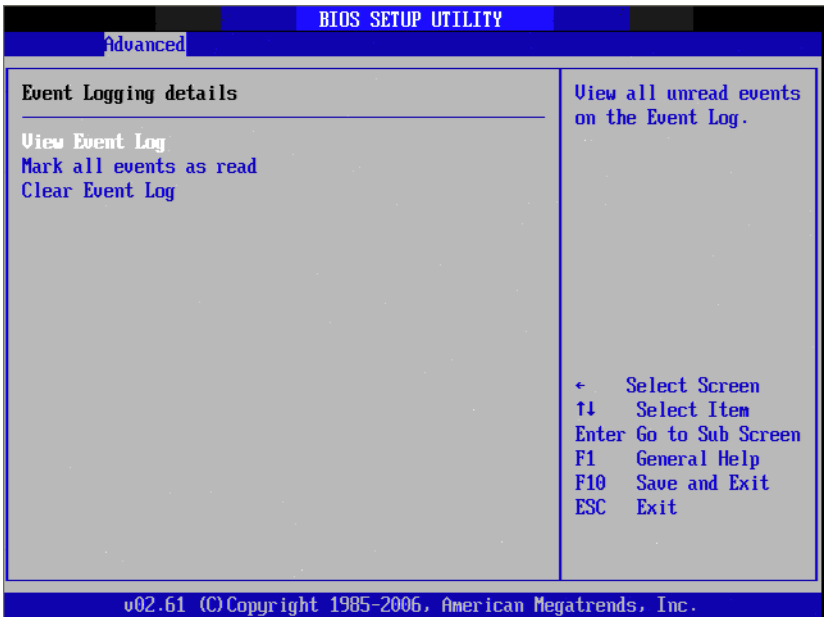


Figure 3.14 Event Log Configuration

- **View Event Log**
  View all unread events on the event Log.
- **Mark all events as read**
  Mark all unread events as read.
- **Clear Event Log**
  Discard all events in the event Log.

3.2.2.9 MPS Configuration

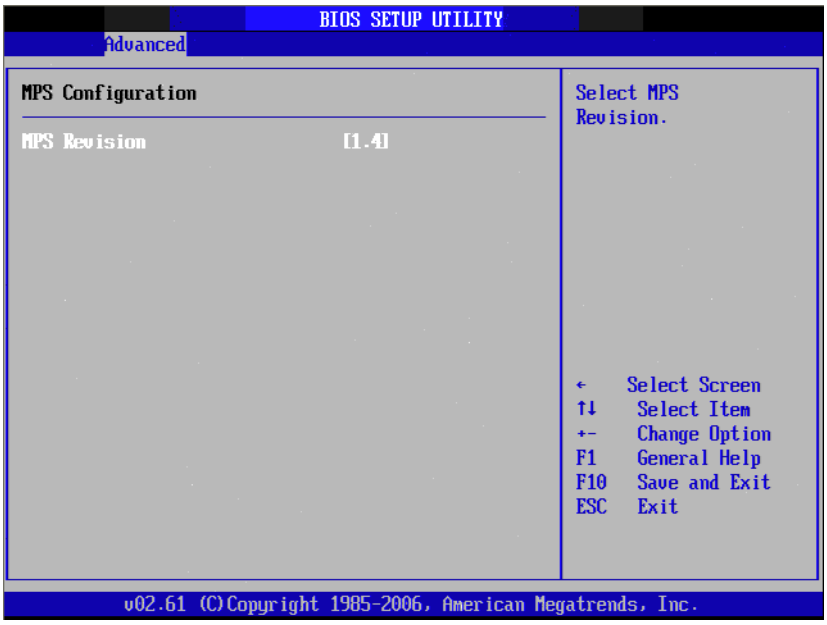


Figure 3.15 MPS Configuration

- **MPS Revision**
  This item allows you to select MPS (Multi-Processor Specification) version.

3.2.2.10 Smbios Configuration

Figure 3.16 Smbios Configuration

- **SMBIOS SMI Support**
  SMBIOS SMI wrapper support for PnP function 50h-54h.

3.2.2.11 USB Configuration

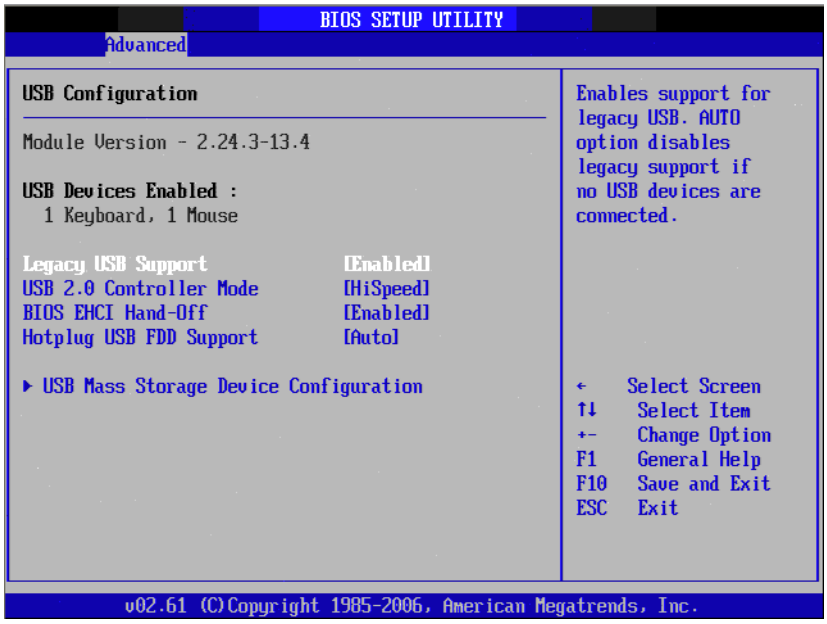


Figure 3.17 USB Configuration

- **Legacy USB Support**
  Enables support for legacy USB. Auto option disables legacy support if no USB devices are connected.
- **USB 2.0 Controller Mode**
  This item allows you to select HiSpeed(480Mbps) or FullSpeed (12Mpbs).

- **BIOS EHCI Hand-Off**

  This is a workaround for an OS without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

- **Hotplug USB FDD Support**

  A dummy FDD device is created that will later be associated with a hotplugged FDD. Auto option creates this dummy device only if there is no USB FDD present.

- **USB Mass Storage Device Configuration**

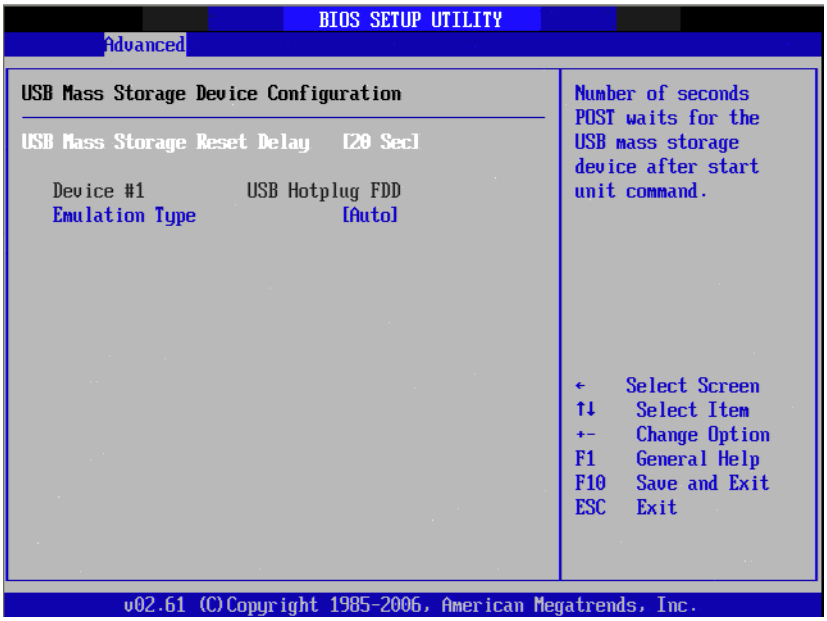


Figure 3.18 USB Mass storage Device Configuration

  - **USB Mass Storage Reset Delay**

    Number of sends POST wait for the USB mass storage device after start unit command.

  - **Emulation Type**

    If Auto, any USB device less than 530MB will be emulated as a floppy drive and the remaining as hard drives. Force FDD option can be used to force a FDD formatted drive to boot as FDD (Ex. ZIP drive).

3.2.3 Advanced PCI/PnP Settings

Select the PCI/PnP tab from the PCM-9363 setup screen to enter the Plug and Play BIOS Setup screen. You can display a Plug and Play BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.

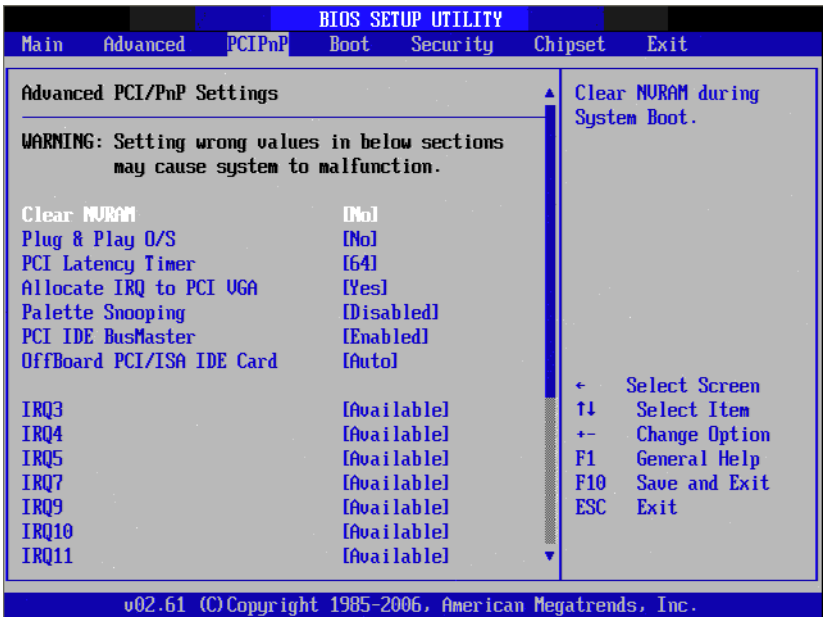


Figure 3.19 PCI/PNP Setup (top)

3.2.3.1 Clear NVRAM

Set this value to force the BIOS to clear the Non-Volatile Random Access Memory (NVRAM).The Optimal and Fail-Safe default setting is No.

3.2.3.2 Plug & Play O/S

When set to No, BIOS configures all the devices in the system. When set to Yes and if you install a Plug and Play operating system, the operating system configures Plug and Play devices not required for bootup.

3.2.3.3 PCI Latency Timer

Value in units of PCI clocks for PCI device latency timer register.

3.2.3.4 Allocate IRQ to PCI VGA

When set to Yes, assigns IRQ to PCI VGA card if card requests IRQ. When set to No, will not assign IRQ to PCI VGA card even if card requests an IRQ.

3.2.3.5 Palette Snooping

This item is designed to solve problems caused by some non-standard VGA cards.

3.2.3.6 PCI IDE BusMaster

When set to enabled BIOS uses PCI busmastering for reading/writing to IDE drives.

3.2.3.7 OffBoard PCI/ISA IDE Card

Some PCI IDE cards may require this to be set to the PCI slot number that is holding the card. When set to Auto will works for most PCI IDE cards.

3.2.3.8 IRQ3 / 4 / 5 / 7 / 9 / 10 /11

This item allows you respectively assign an interruptive type for IRQ-3, 4, 5, 7, 9, 10, 11.

3.2.3.9 DMA Channel 0 / 1 / 3 / 5 / 6 / 7

When set to Available will specify which DMA is available to be used by PCI/PnP devices. When set to Reserved will specify which DMA will be reserved for use by legacy ISA devices.

3.2.3.10 Reserved Memory Size

This item allows you to reserve the size of memory block for legacy ISA device.

3.2.4 Boot Settings

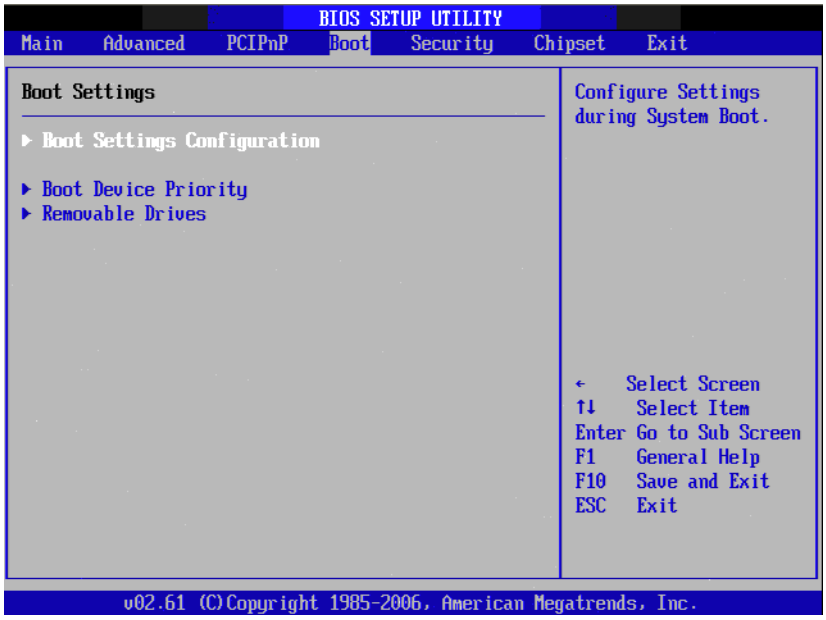


Figure 3.20 Boot Setup Utility

3.2.4.1 Boot Settings Configuration

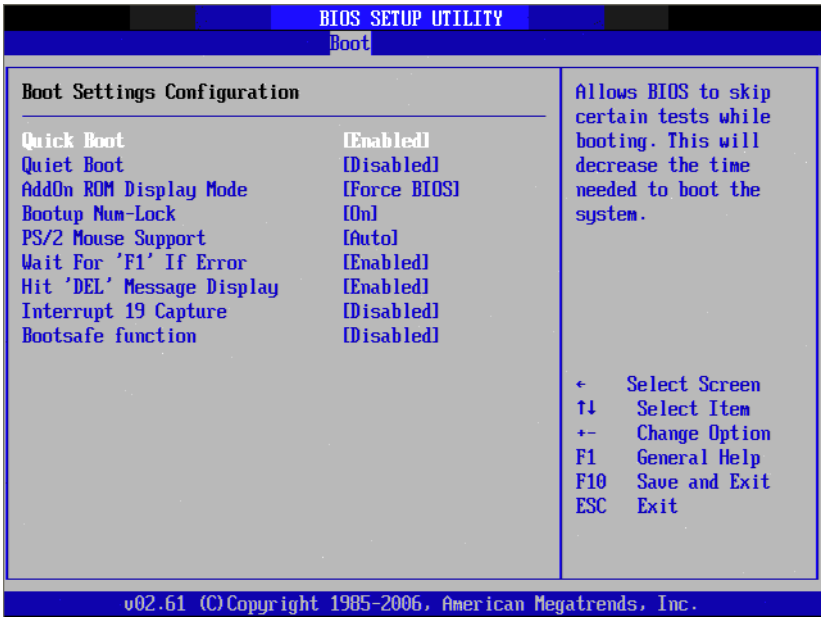


Figure 3.21 Boot Setting Configuration

- **Quick Boot**
  This item allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.
- **Quiet Boot**
  If this option is set to Disabled, the BIOS displays normal POST messages. If Enabled, an OEM Logo is shown instead of POST messages.
- **AddOn ROM Display Mode**
  Set display mode for option ROM.
- **Bootup Num-Lock**
  Select the Power-on state for Numlock.
- **PS/2 Mouse Support**
  Select support for PS/2 Mouse.
- **Wait For 'F1' If Error**
  Wait for the F1 key to be pressed if an error occurs.
- **Hit 'DEL' Message Display**
  Displays -Press DEL to run Setup in POST.
- **Interrupt 19 Capture**
  This item allows options for ROMs to trap interrupt 19.
- **Bootsafe function**
  This item allows you to enable or disable the bootsafe function.

3.2.5 Security Setup

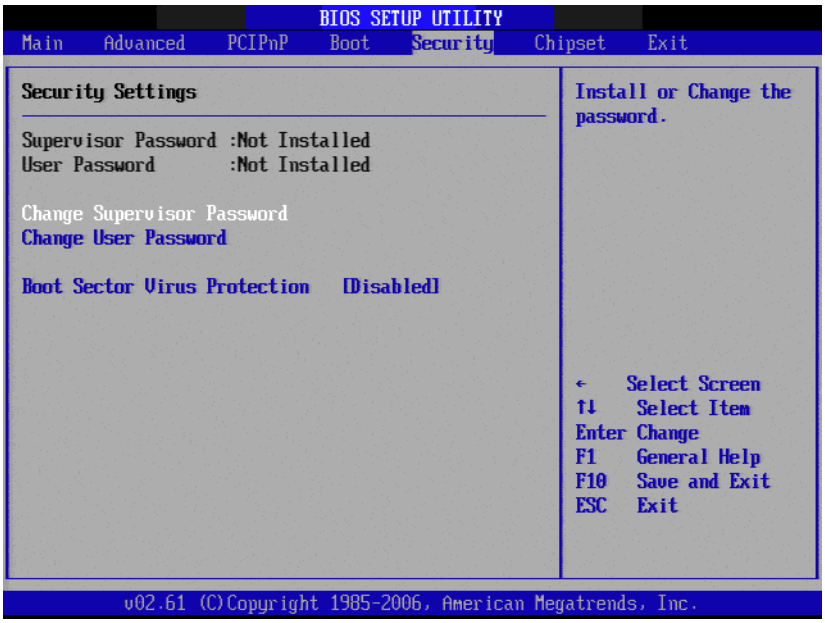


Figure 3.22 Password Configuration

Select Security Setup from the PCM-9363 Setup main BIOS setup menu. All Security Setup options, such as password protection and virus protection are described in this section. To access the sub menu for the following items, select the item and press <Enter>:

3.2.5.1 Change Supervisor / User Password

- **Boot Sector Virus protection**

  The boot sector virus protection will warn if any program tries to write to the boot sector.

3.2.6 Advanced Chipset Settings

Figure 3.23 Advanced Chipset Settings

3.2.6.1 North Bridge Chipset Configuration

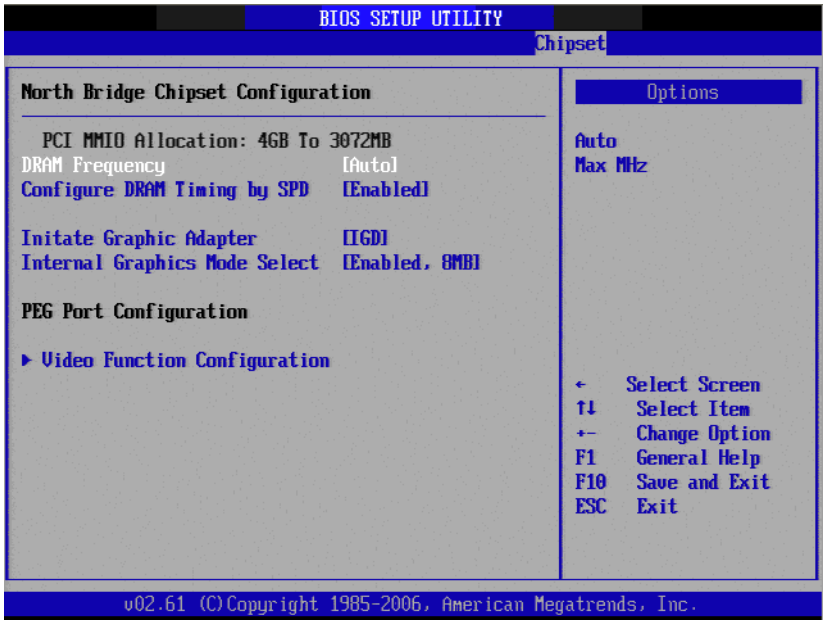


Figure 3.24 North Bridge Configuration

- **DRAM Frequency**

  This item allows you to manually change DRAM frequency.

- **Configure DRAM Timing by SPD**

  This item allows you to enables or disable detection by DRAM SPD.

- **Initiate Graphic Adapter**
  This item allows you to select which graphics controller to use as the primary boot device.
- **Internal Graphics Mode Select**
  Select the amount of system memory used by the Internal graphics device.
- **Video Function Configuration**

Figure 3.25 Video function configuration

  - **DVMT Mode Select**
    Displays the active system memory mode.
  - **DVMT/FIXED Memory**
    Specify the amount of DVMT / FIXED system memory to allocate for video memory.
  - **Boot Display Device**
    Select boot display device at post stage.
  - **Flat Panel Type**
    This item allows you to select which panel resolution you want.
  - **Spread Spectrum Clock**
    This item allows you to enable or disable the spread spectrum clock.
  - **Backlight Control1/2 Type**
    This item allows you to select backlight control type.
  - **Backlight 1/2 Level**
    This item allows you to select backlight level.

3.2.6.2 South Bridge Chipset Configuration

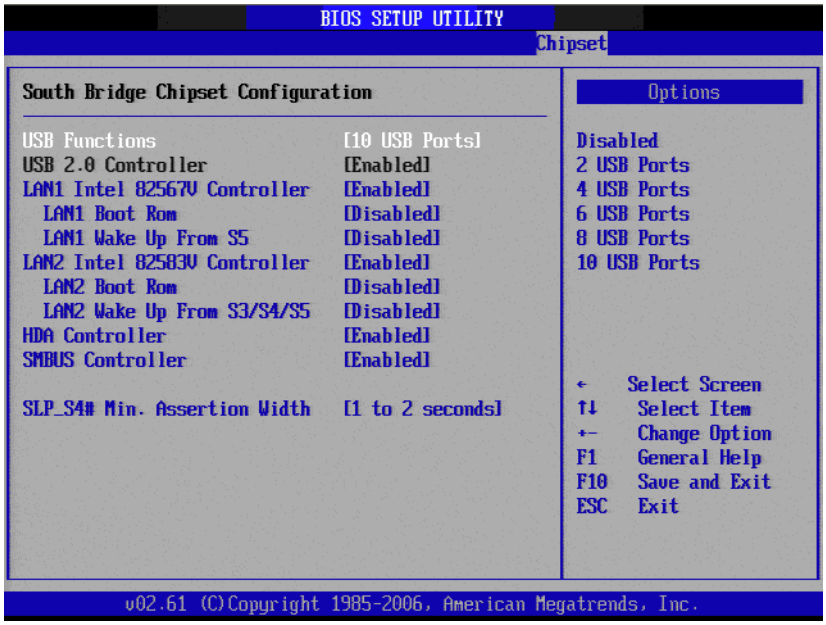


Figure 3.26 South Bridge Configuration

- **USB Functions**
  Disabled, 2 USB Ports, 4 USB Ports, 6 USB Ports or 8 USB Ports or 10 USB Ports.
- **USB 2.0 Controller**
  Enables or disables the USB 2.0 controller.
- **LAN1 Intel 82576V controller**
  Enables or disables the Intel LAN1 controller.
- **LAN1 Boot ROM**
  Enables or disables internal LAN1 boot.
- **LAN1 Wake Up From S5**
  Enables or disables LAN1 wake up from S5 function.
- **LAN2 Intel 82583V controller**
  Enables or disables the LAN2 controller.
- **LAN2 Boot ROM**
  Enables or disables LAN2 boot.
- **LAN2 Wake Up From S3/S4/S5**
  Enables or disables LAN2 wake up from S3/S4S5 function.
- **HDA Controller**
  Enables or disables the HDA controller.
- **SMBUS Controller**
  Enables or disables the SMBUS controller.
- **SLP_S4# Min. Assertion Width**
  SLP_S4# is a signal for power plane control. This signal shuts off power to all non-critical systems when in the S4 (Suspend to disk) or S5 (Soft off) state. This setting indicates minimum assertion width of the SLP_S4# signal to ensure that the DRAMs have been safely power-cycled.

3.2.7 Exit Option

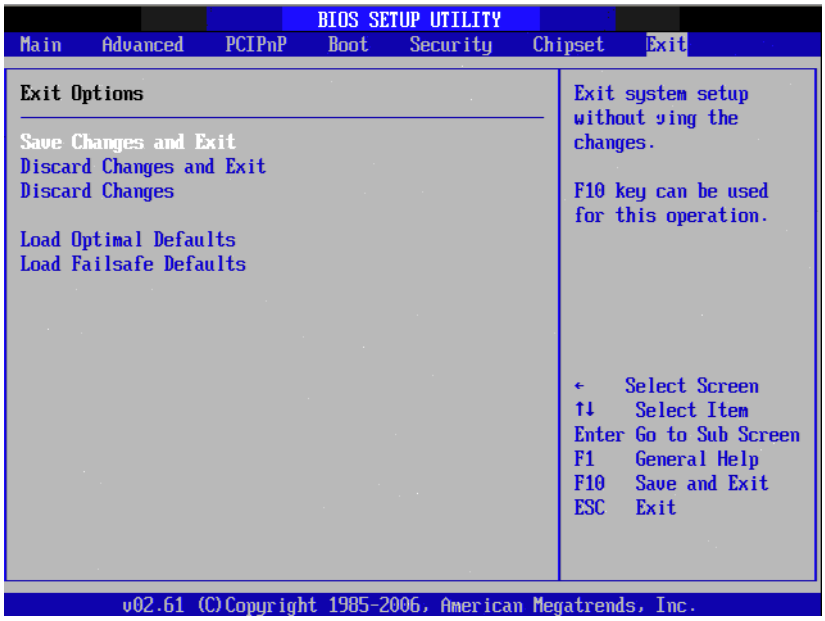


Figure 3.27 Exit Option

3.2.7.1 Save Changes and Exit

When you have completed system configuration, select this option to save your changes, exit BIOS setup and reboot the computer so the new system configuration parameters can take effect.

1. Select Exit Saving Changes from the Exit menu and press <Enter>.
   The following message appears:
   Save Configuration Changes and Exit Now?
   [Ok] [Cancel]
2. Select Ok or cancel.

3.2.7.2 Discard Changes and Exit

Select this option to quit Setup without making any permanent changes to the system configuration.

1. Select Exit Discarding Changes from the Exit menu and press <Enter>.
   The following message appears:
   Discard Changes and Exit Setup Now?
   [Ok] [Cancel]
2. Select Ok to discard changes and exit. Discard Changes
3. Select Discard Changes from the Exit menu and press <Enter>.

3.2.7.3 Load Optimal Defaults

The PCM-9363 automatically configures all setup items to optimal settings when you select this option. Optimal defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the Optimal Defaults if your computer is experiencing system configuration problems. Select Load Optimal Defaults from the Exit menu and press <Enter>.

3.2.7.4 Load Fail-Safe Defaults

The PCM-9363 automatically configures all setup options to fail-safe settings when you select this option. Fail-Safe Defaults are designed for maximum system stability, but not maximum performance. Select Fail-Safe Defaults if your computer is experiencing system configuration problems.

1. Select Load Fail-Safe Defaults from the Exit menu and press <Enter>.
   The following message appears:
   Load Fail-Safe Defaults?
   [OK] [Cancel]
2. Select OK to load Fail-Safe defaults.

Chapter 4

S/W Introduction & Installation

4.1 S/W Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft Windows embedded technology." We enable Windows embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (Hardware suppliers, System integrators, Embedded OS distributor) for projects. Our goal is to make Windows embedded software solutions easily and widely available to the embedded computing community.

4.2 Driver Installation

To install the drivers please just insert the CD into CD-ROM, select the drivers that you want to install, then run .exe (set up) file under each chipset folder and follow Driver Setup instructions to complete the installation.

4.2.1 Windows XP Professional

To install the drivers for Windows XP Professional, insert the CD into the CD-ROM, it will auto-detect the hardware platform and then pop up with the "Embedded Computing Install Wizard box"; just select the drivers that you want to install then click Install All Selected drivers. Follow the Driver Setup Wizard instructions; click "Next" to complete the installation.

4.2.2 Other OS

To install the drivers for another Windows OS or Linux, please browse the CD to run the setup file under each chipset folder on the CD-ROM.

4.3 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. Provides not only the underlying drivers required but also a rich set of user-friendly, intelligent and integrated interfaces, which speeds development, enhances security and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

4.3.1 SUSI Introduction

To make hardware easier and convenient to access for programmers, Advantech has released a suite of API (Application Programming Interface) in the form of a program library. The program Library is called Secured and Unified Smart Interface or SUSI for short.

In modern operating systems, user space applications cannot access hardware directly. Drivers are required to access hardware. User space applications access hardware through drivers. Different operating systems usually define different interface for drivers. This means that user space applications call different functions for hardware access in different operating systems. To provide a uniform interface for accessing hardware, an abstraction layer is built on top of the drivers and SUSI is such an abstraction layer. SUSI provides a uniform API for application programmers to access the hardware functions in different Operating Systems and on different Advantech hardware platforms.

Application programmers can invoke the functions exported by SUSI instead of calling the drivers directly. The benefit of using SUSI is portability. The same set of API is defined for different Advantech hardware platforms. Also, the same set of API is implemented in different Operating Systems including Windows XP and Windows CE. This user's manual describes some sample programs and the API in SUSI. The hardware functions currently supported by SUSI can be grouped into a few categories including Watchdog, I^2C, SMBus, GPIO, and VGA control. Each category of API in SUSI is briefly described below.

4.3.2 Software APIs

4.3.2.1 The GPIO API

General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off a device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

4.3.2.2 The I^2C API

I^2C is a bi-directional two-wire bus that was developed by Phillips for use in their televisions in the 1980s and nowadays is used in various types of embedded systems. The strict timing requirements defined in the I^2C protocol has been taken care of by SUSI. Instead of asking application programmers to figure out the strict timing requirements in the I^2C protocol, the I^2C API in SUSI can be used to control I^2C devices by invoking other function calls. SUSI provides a consistent programming interface for different Advantech boards. That means user programs using SUSI are portable among different Advantech boards as long as the boards and SUSI provide the required functionalities. Overall product development times can be greatly reduced using SUSI.

4.3.2.3 The SMBus API

The System Management Bus (SMBus) is a two-wire interface defined by Intel® Corporation in 1995. It is based on the same principles of operation of I^2C and is used in personal computers and servers for low-speed system management communications. Nowadays, it can be seen in many types of embedded systems. As with other API in SUSI, the SMBus API is available on many platforms including Windows XP and Windows CE.

4.3.2.4 The Display Control API

There are two kinds of VGA control APIs, backlight on/off control and brightness control. Backlight on/off control allows a developer to turn on or off the backlight, and to control brightness smoothly.

1. Brightness Control
   - The Brightness Control API allows a developer to interface with an embedded device to easily control brightness.
2. Backlight Control
   - The Backlight API allows a developer to control the backlight (screen) on/off in an embedded device.

4.3.2.5 The Watchdog API

A watchdog timer (abbreviated as WDT) is a hardware device which triggers an action, e.g. rebooting the system, if the system does not reset the timer within a specific period of time. The WDT API in SUSI provides developers with functions such as starting the timer, resetting the timer, and setting the timeout value if the hardware requires customized timeout values.

4.3.2.6 The Hardware Monitor API

The hardware monitor (abbreviated as HWM) is a system health supervision capability achieved by placing certain I/O chips along with sensors for inspecting the target of interests for certain condition indexes, such as fan speed, temperature and voltage etc.

However, due to the inaccuracy among many commercially available hardware monitoring chips, Advantech has developed a unique scheme for hardware monitoring - achieved by using a dedicated micro-processor with algorithms specifically designed for providing accurate, real-time and reliable data content; helping protect your system in a more reliable manner.

4.3.2.7 The Power Saving API

1. CPU Speed
   - Make use of Intel SpeedStep technology to reduce power consumption. The system will automatically adjust the CPU Speed depending on system loading.
2. System Throttling
   - Refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. APIs allow the user to lower the clock from 87.5% to 12.5%.

4.3.3 SUSI Utilities

4.3.3.1 BIOS Flash

The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up current BIOS by copying it from the flash chip to a file on customers'disk. The BIOS Flash utility also provides a command line version and API for fast implementation into customized applications.

4.3.3.2 Embedded Security ID

The embedded application is the most important property of a system integrator. It contains valuable intellectual property, design knowledge and innovation, but it is easily copied! The Embedded Security ID utility provides reliable security functions for customers to secure their application data within embedded BIOS.

4.3.3.3 Monitoring utility

The Monitoring utility allows the customer to monitor system health, including voltage, CPU and system temperature and fan speed. These items are important to a device; if critical errors happen and are not solved immediately, permanent damage may be caused.

4.3.3.4 eSOS

The eSOS is a small OS stored in BIOS ROM. It will boot up in case of a main OS crash. It will diagnose the hardware status, and then send an e-mail to a designated administrator. The eSOS also provides remote connection: Telnet server and FTP server, allowing the administrator to rescue the system.

4.3.3.5 Flash Lock

Flash Lock is a mechanism that binds the board and CF card (SQFlash) together. The user can “Lock” SQFlash via the Flash Lock function and “Unlock” it via BIOS while booting. A locked SQFlash cannot be read by any card reader or boot from other platforms without a BIOS with the “Unlock” feature.

4.3.4 SUSI Installation

SUSI supports many different operating systems. Each subsection below describes how to install SUSI and related software on a specific operating system. Please refer to the subsection matching your operating system.

4.3.4.1 Windows XP

In windows XP, you can install the library, drivers and demo programs onto the platform easily using the installation tool--The SUSI Library Installer. After the installer has executed, the SUSI Library and related files for Windows XP can be found in the target installation directory. The files are listed in the following table.

Directory	Contents
\Library	■ Susi.lib Library for developing the applications on Windows XP. ■ Susi.dll Dynamic library for SUSI on Windows XP.
\Demo	■ SusiDemo.EXE Demo program on Windows XP. ■ Susi.dll Dynamic library for SUSI on Windows XP.
\Demo\SRC	Source code of the demo program on Windows XP.

The following section illustrates the installation process.

Note! *The SUSI Library Installer screen shots shown below are examples only. Your screens may vary depending on your particular version.*

1. Extract Susi.zip.
2. Double-click the "Setup.exe" file.

The installer searches for a previous installation of the SUSI Library. If it locates one, a dialog box opens asking whether you want to modify, repair or remove the software. If a previous version is located, please see the [Maintenance Setup] section. If it is not located, an alternative window appears. Click Next.

4.3.4.2 Windows CE

In windows CE, there are three ways to install the SUSI Library, you can install it manually or use Advantech CE-Builder to install the library or just copy the programs and the library onto a compact flash card.

Express Installation:

You can use Advantech CE-Builder to load the library into the image.

- First, you click the My Component tab.
- In this tab, you click Add New Category button to add a new category, e.g. the SUSI Library.
- Then you can add a new file in this category, and upload the SUSI.dll for this category.
- After these steps, you can select the SUSI Library category you created for every project.

Manual Installation:

You can add the SUSI Library into the image by editing any bib file.

First you open project.bib in the platform builder.

- Add this line to the MODULES section of project.bib
  Susi.dll $(_FLATRELEASEDIR)\Susi.dll NK SH
- If you want to run the window-based demo, add following line:
  SusiTest.exe $(_FLATRELEASEDIR)\SusiTest.exe
- If you want to run the console-based demo, add following lines:
  Watchdog.exe $(_FLATRELEASEDIR)\Watchdog.exe NK S
  GPIO.exe $(_FLATRELEASEDIR)\GPIO.exe NK S
  SMBUS.exe $(_FLATRELEASEDIR)\SMBUS.exe NK S
- Place the three files into any files directory.
- Build your new Windows CE operating system.

4.3.5 SUSI Sample Programs

Sample Programs

The sample programs demonstrate how to incorporate SUSI into your program. There are sample programs for two categories of operating system, i.e. Windows XP and Windows CE. The sample programs run in graphics mode in Windows XP and Windows CE. The sample programs are described in the subsections below.

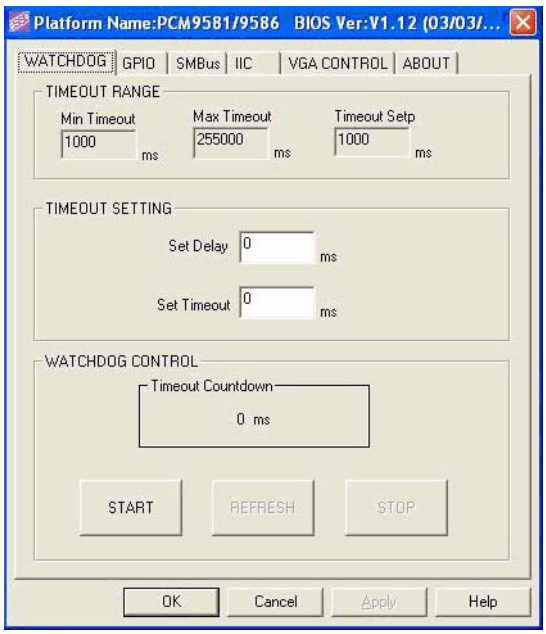
Windows Graphics Mode

There are sample programs of Windows in graphics mode for two categories of operating system, i.e. Windows CE and Windows XP. Each demo application contains an executable file SusiDemo.exe, a shared library Susi.dll and source code within the release package. The files of Windows CE and Windows XP are not compatible with each other.

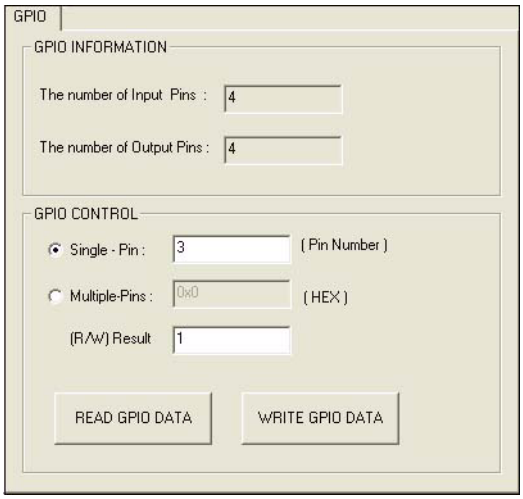
SusiDemo.exe is an executable file and it requires the shared library, Susi.dll, to demonstrate the SUSI functions. The source code of SusiDemo.exe also has two versions, i.e. Windows CE and Windows XP, and must be compiled under Microsoft Visual C++ 6.0 on Windows XP or under Microsoft Embedded Visual C++ 4.0 on Windows CE. Developers must add the header file Susi.h and library Susi.lib to their own projects when they want to develop something with SUSI.

SusiDemo.exe

The SusiDemo.exe test application is an application which uses all functions of the SUSI Library. It has five major function blocks: Watchdog, GPIO, SMBus, I^2C and VGA control. The following screen shot appears when you execute SusiDemo.exe. You can click function tabs to select test functions respectively. Some function tabs will not show on the test application if your platform does not support such functions. For a complete support list, please refer to Appendix A. We describe the steps to test all functions of this application.



GPIO



When the application is executed, it will display GPIO information in the GPIO INFORMATION group box. It displays the number of input pins and output pins. You can click the radio button to choose to test either the single pin function or multiple pin functions. The GPIO pin assignments of the supported platforms are located in Appendix B.

- Test Read Single Input Pin
  - Click the radio button- Single-Pin.
  - Key in the pin number to read the value of the input pin. The Pin number starts from '0'.

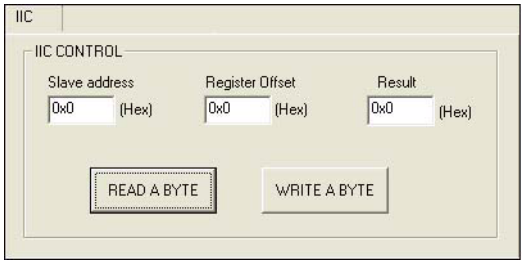
– Click the READ GPIO DATA button and the status of the GPIO pin will be displayed in (R/W) Result field.

- Test Read Multiple Input Pin
  – Click the radio button- Multiple-Pins.
  – Key in the pin number from ‘0x01’ to ‘0x0F’ to read the value of the input pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to read pin 0, 1, and 3, the pin numbers should be ‘0x0B’.
  – Click READ GPIO DATA button and the statuses of the GPIO pins will be displayed in (R/W) Result field.

- Test Write Single Output Pin
  – Click the radio button- Single-Pin.
  – Key in the pin numbers you want to write. Pin numbers start from '0'.
  – Key in the value either '0' or '1' in (R/W) Result field to write the output pin you chose above step.
  – Click the WRITE GPIO DATA button to write the GPIO output pin.

- Test Write Multiple Output Pins
  – Click the radio button- Multiple-Pins.
  – Key in the pin number from ‘0x01’ to ‘0x0F’ to choose the multiple pin numbers to write the value of the output pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to write pin 0, 1, and 3, the pin numbers should be ‘0x0B’.
  – Key in the value in (R/W) Result field from ‘0x01’ to ‘0x0F’ to write the value of the output pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to set pin 0 and 1 high, 3 to low, the pin number should be ‘0x0B/, and then you should key in the value ‘0x0A’ to write.
  – Click the WRITE GPIO DATA button to write the GPIO output pins.

I²C

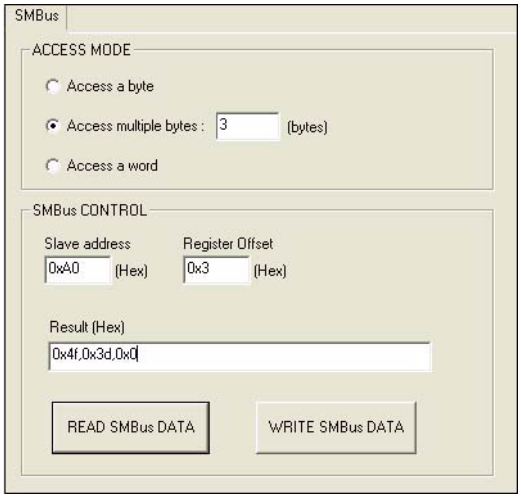


When the application is executed, you can read or write a byte of data through I²C devices. All data must be read or written in hexadecimal system.

- Read a byte
  – Key in the slave device address in Slave address field.
  – Key in the register offset in Register Offset field.
  – Click the READ A BYTE button and then a byte of data from the device will be shown on the Result field.

- Write a byte
  - Key in the slave device address in Slave address field.
  - Key in the register offset in Register Offset field.
  - Key in the desirous of data in Result field to write to the device.
  - Click the WRITE A BYTE button and then the data will be written to the device through I^2C.

SMBus



When the application has executed, you can click the radio button to choose to test each access mode, i.e. Access a byte, Access multiple bytes and Access a word. All data must be read or written in hexadecimal except the numbers for radio button: Access multiple bytes mode must be written in decimal. You can test the functionalities of the watchdog as follows:

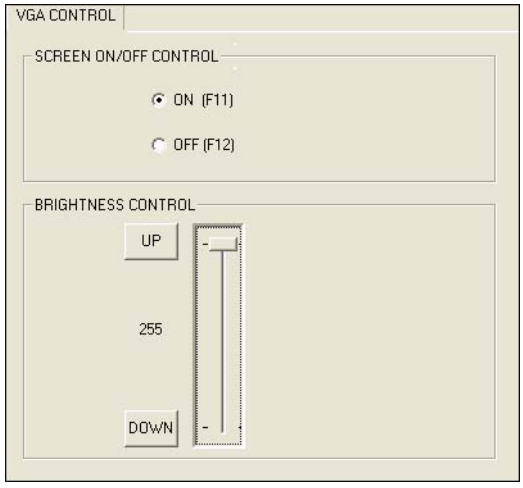
- Read a byte
  - Click the radio button- Access a byte.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Click the READ SMBus DATA button and a byte of data from the device will be shown on the Result field.

- Write a byte
  - Click the radio button- Access a byte.
  - Key in the slave device address in Slave address field.
  - Key in the register offset in Register Offset field.
  - Key the desired data in the Result field to write to the device.
  - Click the WRITE SMBus DATA button and then the data will be written to the device through SMBus.

- Read a word
  - Click the radio button- Access a word.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Click the READ SMBus DATA button and then a word of data from the device will be shown on the Result field.

- Write a word
  - Click the radio button- Access a word.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Key in the desired data, such as 0x1234, in the Result field to write to the device.
  - Click the WRITE SMBus DATA button and the data will be written to the device through the SMBus.
- Read Multiple bytes
  - Click the radio button- Access multiple bytes.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Key in the desired number of bytes, such as 3, in the right side field of radio button- Access multiple bytes. The number must be written in decimal.
  - Click the READ SMBus DATA button and then all data from the device will be divided from each other by commas and be shown in the Result field.
- Write Multiple bytes
  - Click the radio button- Access multiple bytes.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Key in the desired number of bytes, such as 3, in the right side field of the radio button- Access multiple bytes. The number must be written in decimal.
  - Key in all the desired data in the Result field in hexadecimal format, divided by commas, for example, 0x50,0x60,0x7A.
  - Click the WRITE SMBus DATA button and all of the data will be written to the device through the SMBus.

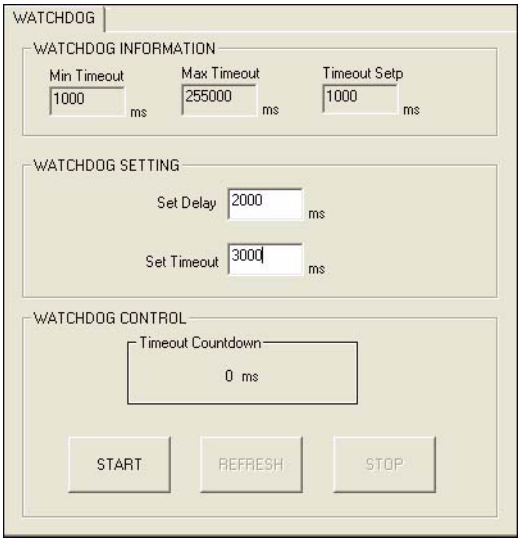
Display Control



When the application is executed, it will display two blocks of VGA control functions. The application can turn on or turn off the screen shot freely, and it also can tune the brightness of the panels if your platform is being supported. You can test the functionalities of VGA control as follows:

- Screen on/off control
  - Click the radio button ON or push the key F11 to turn on the panel screen.
  - Click the radio button OFF or push the key F12 to turn off the panel screen.
  - The display chip of your platform must be in the support list in Appendix A, or this function cannot work.
- Brightness control
  - Move the slider in increments, using either the mouse or the direction keys, or click the UP button to increase the brightness.
  - Move the slider in decrements, using either the mouse or the direction keys, or click the DOWN button to decrease the brightness.

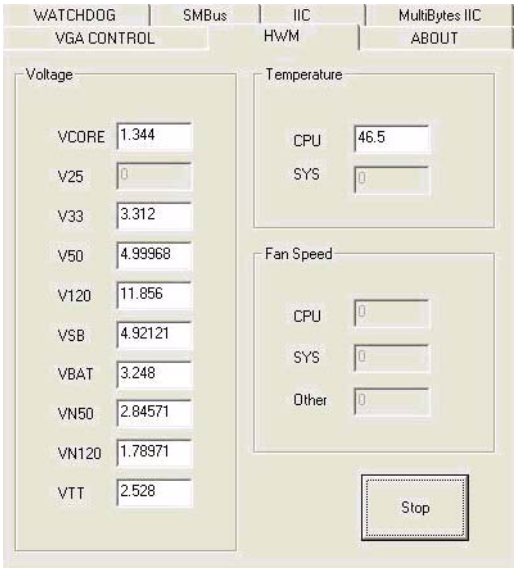
Watchdog



When the application is executed, it will display watchdog information in the WATCHDOG INFORMATION group box. It displays max timeout, min timeout, and timeout steps in milliseconds. For example, a 1~255 seconds watchdog will have 255000 max timeout, 1000 min timeout, and 1000 timeout steps. You can test the functionality of the watchdog as follows:

- Set the timeout value 3000 (3 sec.) in the SET TIMEOUT field and set the delay value 2000 (2 sec.) in the SET DELAY field, then click the START button. The Timeout Countdown field will countdown the watchdog timer and display 5000 (5 sec.).
- Before the timer counts down to zero, you can reset the timer by clicking the REFRESH button. After you click this button, the Timeout Countdown field will display the value of the SET TIMEOUT field.
- If you want to stop the watchdog timer, just click the STOP button.

Hardware Monitor



When the Monitor application is executed by clicking the button, hardware monitoring data values will be displayed. If certain data values are not supported by the platform, the correspondent data field will be grayed-out with a value of 0.

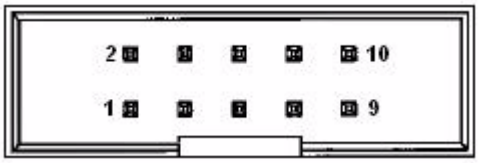
For more details on PCM-9363 software API, please contact your dealer or Advantech AE. API user manuals are also included on this CD.

Appendix A

PIN Assignments

A.1 PIN Assignments

Table A.1: CN1: Audio	
Part Number	1653205260
Footprint	HD_5x2P_79_BOX
Description	BOX HEADER SMD 5*2 180D (M) 2.0mm
Pin	**Pin Name**
1	LOUTR
2	LINR
3	GND
4	GND
5	LOUTL
6	LINL
7	GND
8	GND
9	MIC1R
10	MIC1L



Matching Cable: 1703100152

Table A.2: CN2: SATA	
Part Number	1654002320
Footprint	FOX_LD1107V-S33T5
Description	Serial ATA 7P 1.27 90D(M) SMD LD1107V-S33T5
Pin	**Pin Name**
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

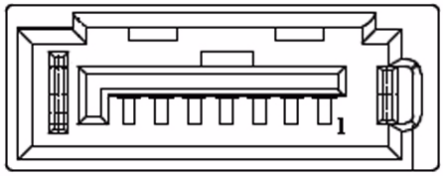


Table A.3: CN3: SATA	
Part Number	1654002320
Footprint	FOX_LD1107V-S33T5
Description	Serial ATA 7P 1.27 90D(M) SMD LD1107V-S33T5
Pin	**Pin Name**
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

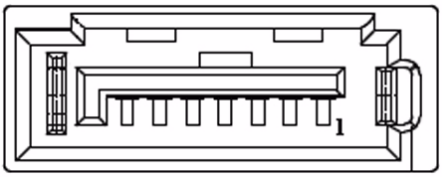


Table A.4: CN4: GPIO	
Part Number	1653005261
Footprint	HD_5x2P_79
Description	PIN HEADER SMD 5*2P 180D(M) 2.0mm
Pin	**Pin Name**
1	+5V
2	GPIO4
3	GPIO0
4	GPIO5
5	GPIO1
6	GPIO6
7	GPIO2
8	GPIO7
9	GPIO3
10	GND

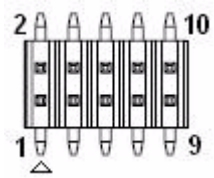


Table A.5: CN5: HDD & PWR LED	
Part Number	1655306020
Footprint	WHL6V-2M
Description	WAFER BOX 2.0mm 6P 180D(M) W/LOCK
Pin	**Pin Name**
1	+5V
2	GND
3	Power LED+
4	Power LED-
5	HDD LED+
6	HDD LED-

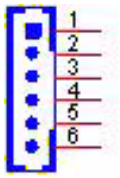


Table A.6: CN6: 12 V Power Input	
Part Number	1655404090
Footprint	ATXCON-2X2-42
Description	ATX PWR CONN. 2*2P 180D 4.2mm 24W4310-04S10-01T
Pin	**Pin Name**
1	GND
2	GND
3	+12V
4	+12V

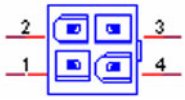
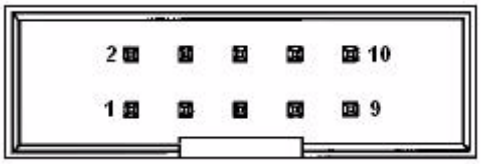
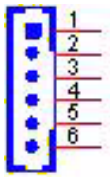


Table A.7: CN8: COM3	
Part Number	1653205260
Footprint	BH_5x2V_S2.00mm
Description	BOX HEADER SMD 5*2P 180D(M) 2.0mm
Pin	**Pin Name**
1	DCD#
2	DSR#
3	RXD
4	RTS#
5	TXD
6	CTS#
7	DTR#
8	RI#
9	GND
10	GND



Matching Cable: TBD

Table A.8: CN10: PS2	
Part Number	1655306020
Footprint	WHL6V-2M
Description	WAFER BOX 2.0mm 6P 180D(M) W/LOCK
Pin	**Pin Name**
1	KBCLK
2	KBDAT
3	MSCLK
4	GND
5	+5V
6	MSDAT



Matching Cable: 1703060053 1700060202

Table A.9: CN11: SMBus	
Part Number	1655904020
Footprint	FPC4V-125M
Description	Wafer SMT 1.25mmS/T type 4P 180D(M) 85205-04001
Pin	**Pin Name**
1	GND
2	SMB_DAT
3	SMB_CLK
4	+5V

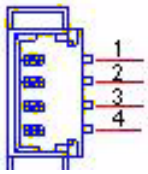
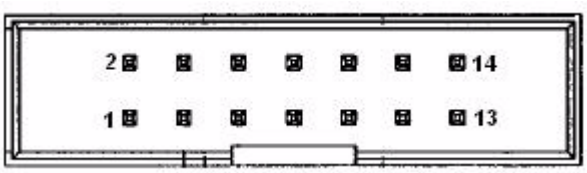


Table A.10: CN12: COM2	
Part Number	1653207260
Footprint	HD_7x2P_79_BOX
Description	BOX HEADER SMD 7*2P 180D(M) 2.0mm
Pin	**Pin Name**
1	DCD#
2	DSR#
3	RXD
4	RTS#
5	TXD
6	CTS#
7	DTR#
8	RI#
9	GND
10	GND
11	422TX+/485+
12	422TX-/485-
13	422RX+
14	422RX-

Note: *Pins 1 ~ 10: RS-232; Pins 11 ~ 12: RS-485; Pins 11 ~ 14: RS-422*



Matching Cable: 1701140201

Table A.11: CN13: Inverter Power Output	
Part Number	1655000453
Footprint	WHL5V-2M-24W1140
Description	WAFER BOX 2.0mm 5P 180D(M) DIP WO/pb JIH VEI
Pin	**Pin Name**
1	+12V
2	GND
3	ENABKL
4	VBR
5	+5V

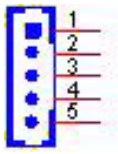
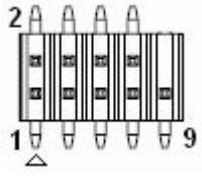
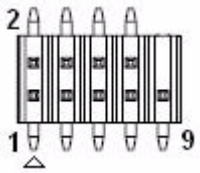


Table A.12: CN14: Internal USB	
Part Number	1653005260
Footprint	HD_5x2P_79_N10
Description	PIN HEADER 2*5P 180D(M) 2.0mm SMD IDIOT-PROOF
Pin	**Pin Name**
1	+5V
2	+5V
3	A_D-
4	B_D-
5	A_D+
6	B_D+
7	GND
8	GND
9	GND



Matching Cable: 1703100121

Table A.13: CN15: Internal USB	
Part Number	1653005260
Footprint	HD_5x2P_79_N10
Description	PIN HEADER 2*5P 180D(M) 2.0mm SMD IDIOT-PROOF
Pin	**Pin Name**
1	+5V
2	+5V
3	A_D-
4	B_D-
5	A_D+
6	B_D+
7	GND
8	GND
9	GND



Matching Cable: 1703100121

Table A.14: CN16: 18 or 24 bits LVDS Panel	
Part Number	1653910261
Footprint	SPH10X2
Description	*CONN. SMD 10*2P 180D(M)DF13-20DP-1.25V(91) HRS
Pin	**Pin Name**
1	GND
2	GND
3	LVDS0_D0+
4	NC
5	LVDS0_D0-
6	NC
7	LVDS0_D1+
8	NC
9	LVDS0_D1-
10	NC
11	LVDS0_D2+
12	NC
13	LVDS0_D2-
14	NC
15	LVDS0_CLK+
16	LVDS0_z_D3+
17	LVDS0_CLK-

Table A.14: CN16: 18 or 24 bits LVDS Panel	
18	LVDS0_z_D3-
19	+5V or +3.3V
20	+5V or +3.3V

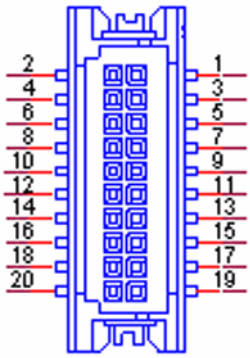


Table A.15: CN17: Single LAN (Optional)	
Part Number	1652002996
Footprint	RJ45_14P_RTA-195AAK1A
Description	PHONE JACK RJ45 14P 90D(M) DIP RTA-195AAK1A
Pin	**Pin Name**
1	TX+(10/100),BI_DA+(GHz)
2	TX-(10/100),BI_DA-(GHz)
3	RX+(10/100),BI_DB+(GHz)
4	BI_DC+(GHz)
5	BI_DC-(GHz)
6	RX-(10/100),BI_DB-(GHz)
7	BI_DD+(GHz)
8	BI_DD-(GHz)

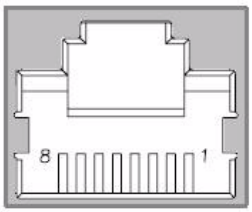


Table A.16: CN18: LAN1	
Part Number	1652002996
Footprint	RJ45_14P_RTA-195AAK1A
Description	Phone Jack RJ45 14P 90D(M) DIP RTA-195AAK1A
Pin	**Pin Name**

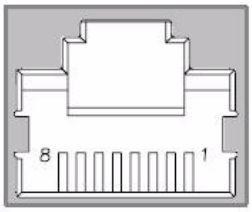


Table A.17: CN19: LAN2	
Part Number	1652002996
Footprint	RJ45_14P_RTA-195AAK1A
Description	Phone Jack RJ45 14P 90D(M) DIP RTA-195AAK1A
Pin	**Pin Name**

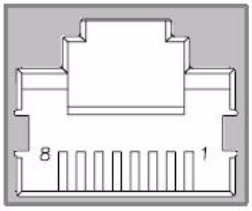


Table A.18: CN20: Power Switch (Low Active)	
Part Number	1655302020
Footprint	WF_2P_79_BOX_R1_D
Description	WAFER BOX 2P 180D(M) 2.0mm W/Lock
Pin	**Pin Name**
1	PSIN
2	GND

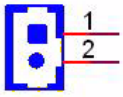
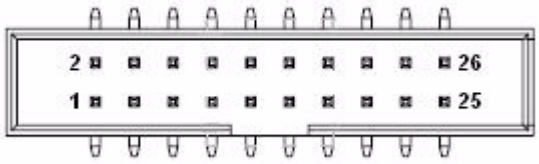


Table A.19: CN21: LPT	
Part Number	1653213260
Footprint	HD_13x2P_79_BOX
Description	BOX HEADER 13*2P 180D(M) 2.0mm SMD
Pin	**Pin Name**
1	STROBE#
2	AUTOFEED#
3	D0
4	ERROR#
5	D1
6	INIT#
7	D2
8	SLCT IN#
9	D3
10	GND
11	D4
12	GND
13	D5
14	GND
15	D6
16	GND
17	D7
18	GND
19	ACK#
20	GND
21	BUSY
22	GND
23	PE
24	GND
25	SLCT
26	NC



Matching Cable: 1700260250 1700001531

Table A.20: CN22: HDMI (Optional)	
CN22	**HDMI**
Part Number	1654009225
Footprint	HDMI_19P_QJ51193-FFD4-4F
Description	HDMI Conn 19P 0.5mm 90D(M) SMD QJ51193-FFB4-7F
Pin	Pin Name
1	HDMI_D2+
2	GND
3	HDMI_D2-
4	HDMI_D1+
5	GND
6	HDMI_D1-
7	HDMI_D0+
8	GND
9	HDMI_D0-
10	HDMI_CLK+
11	GND
12	HDMI_CLK-
13	HDMI_z_CEC
14	NC
15	HDMI_SCL
16	HDMI_SDA
17	GND
18	+V5_HDMI
19	HDMI_z_DET

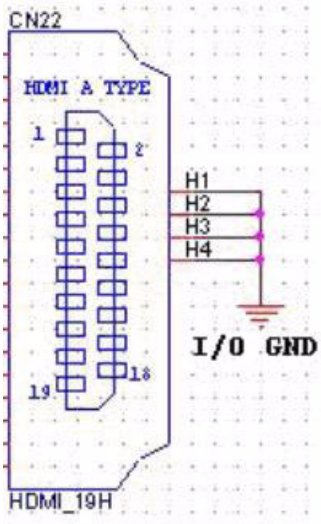


Table A.21: CN23: Reset	
Part Number	1655302020
Footprint	WF_2P_79_BOX_R1_D
Description	WAFER BOX 2P 180D(M) 2.0mm W/Lock
Pin	**Pin Name**
1	RESET#
2	GND

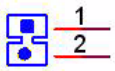


Table A.22: CN24: External USB	
Part Number	1654904105
Footprint	USB-V-4A
Description	USB CON. 4P 90D(F) DIP A TYPE RoHS
Pin	**Pin Name**
1	+5V
2	D-
3	D+
4	GND

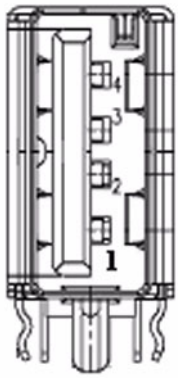


Table A.23: CN25: External USB	
Part Number	1654904105
Footprint	USB-V-4A
Description	USB CON. 4P 90D(F) DIP A TYPE RoHS
Pin	**Pin Name**
1	+5V
2	D-
3	D+
4	GND

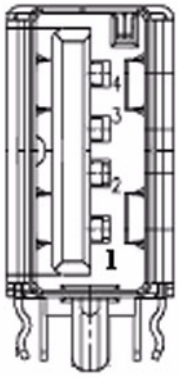


Table A.24: CN26: COM1	
Part Number	1654000056
Footprint	DBCOM-VM5MS
Description	D-SUB CON. 9P 90D(M)DIP 070241MR009S200ZU SUYIN
Pin	**Pin Name**
1	DCD#
2	RXD
3	TXD
4	DTR#
5	GND
6	DSR#
7	RTS#
8	CTS#
9	RI#

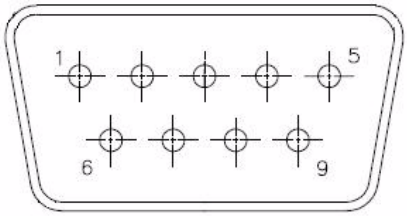


Table A.25: CN27: VGA	
Part Number	1654000055
Footprint	DBVGA-VF5MS
Description	D-SUB Conn. 15P 90D(F) DIP 070242FR015S200ZU
Pin	**Pin Name**
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND
9	NC
10	GND
11	NC
12	DDAT
13	HSYNC
14	VSYNC
15	DCLK

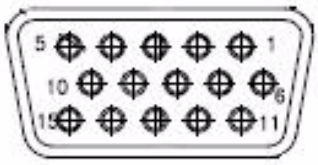


Table A.26: CN28: Mini PCIE lock	
Part Number	1654002539
Footprint	FOX_AS0B226-S68K7F_HOLDER
Description	MINI PCI Express LATCH 52P 90D SMD 6.8mm
Pin	**Pin Name**

Table A.27: CN29: Mini PCIE slot	
Part Number	1654002538
Footprint	FOX_AS0B226-S68K7F
Description	MINI PCI express 52P 90D SMD H=6.8mm
Pin	**Pin Name**
1	WAKE#
2	+3.3V or +3.3VSB
3	NC
4	GND
5	NC
6	+1.5V
7	CLKREQ#
8	NC
9	GND
10	NC
11	REFCLK-
12	NC
13	REFCLK+
14	NC

Table A.27: CN29: Mini PCIE slot	
15	GND
16	NC
17	NC
18	GND
19	NC
20	NC
21	GND
22	PERST#
23	PERn0
24	+3.3VSB
25	PERp0
26	GND
27	GND
28	+1.5V
29	GND
30	SMB CLK
31	PETn0
32	SMB DAT
33	PETp0
34	GND
35	GND
36	USB D-
37	GND
38	USB D+
39	+3.3V or +3.3VSB
40	GND
41	+3.3V or +3.3VSB
42	NC
43	GND
44	NC
45	NC
46	NC
47	NC
48	+1.5V
49	NC
50	GND
51	NC
52	+3.3V or +3.3VSB
53	NC
54	NC
55	GND
56	GND

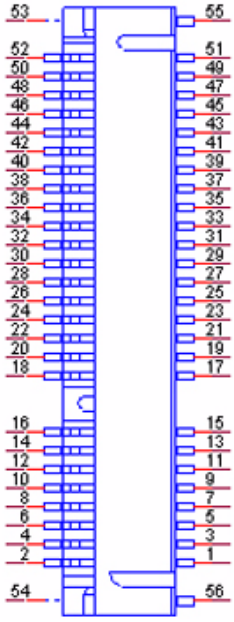


Table A.28: CN30: DDR3 SODIMM	
Part Number	1651001904
Footprint	DDR-SODIMM-STD65
Description	SKT DIMM 200P DDR2 H=6.5mm STD SMD WO/Pb
Pin	**Pin Name**
1	VREF
2	GND
3	GND
4	DQ59
5	DQ63
6	DQ58
7	DQ62
8	GND
9	GND
10	DM7
11	DQS#7
12	GND
13	DQS7
14	DQ57
15	GND
16	DQ56
17	DQ61
18	GND
19	DQ60
20	DQ51
21	GND
22	DQ50
23	DQ55

Table A.28: CN30: DDR3 SODIMM	
24	GND
25	DQ54
26	DM6

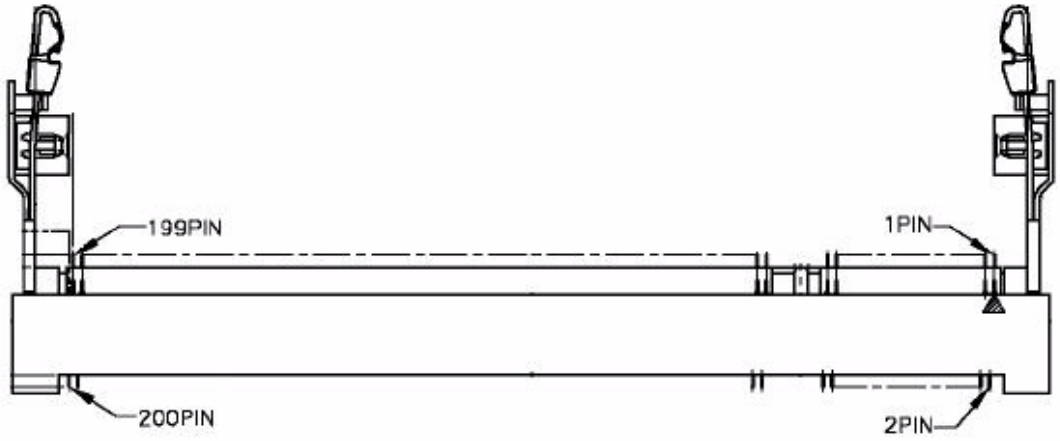


Table A.29: CN31: BIOS Socket	
Part Number	1651000682
Footprint	SOCKET_8P_ACA-SPI-004-K01
Description	IC SKT 8P SMD WO/Pb C ACA-SPI-004-K01
Pin	**Pin Name**
1	CE#
2	SO
3	WP#
4	GND
5	SI
6	SCK
7	HOLD#
8	+3.3V

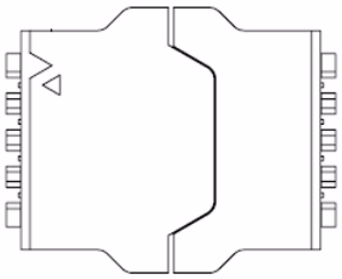


Table A.30: CN32: CF	
Part Number	1653002919
Footprint	CF_50P_CFCMD-35T15W100
Description	CF Type2 Conn.50P 90D(M) SMD WO/Pb CFCMD-35T15W1
Pin	**Pin Name**
1	GND
2	D03
3	D04
4	D05
5	D06
6	D07
7	CS0#
8	GND
9	GND
10	GND
11	GND
12	GND
13	+5V
14	GND
15	GND
16	GND
17	GND
18	A02
19	A01
20	A00
21	D00
22	D01
23	D02
24	NC
25	CD2#
26	CD1#

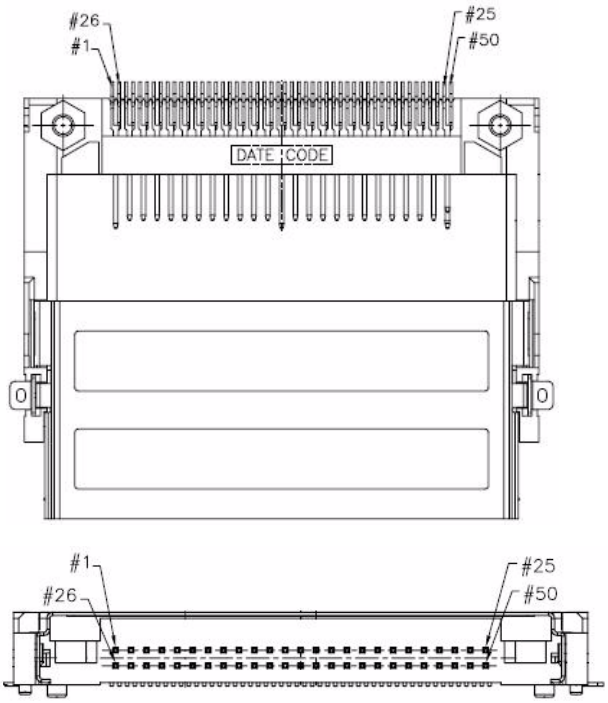
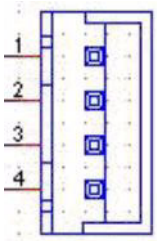


Table A.31: CN36: SATA Power	
CN36	**SATA Power**
Part Number	1655000453
Footprint	WF_4P_98_BOX_R1_D
Description	WAFER BOX 2.0mm 5P 180D(M) DIP WO/Pb JIH VEI
Pin	Pin Name
1	+V5
2	GND
3	GND
4	+12V



Appendix B

WDT & GPIO

B.1 Watchdog Timer Sample Code

Watchdog function:

```
;The SCH3114 Runtime base I/O address is A00h
;Setting WatchDog time value location at offset 66h
;If set value "0", it is mean disable WatchDog function.
Superio_GPIO_Port = A00h
mov dx,Superio_GPIO_Port + 66h
mov al,00h
out dx,al
.model small
.486p
.stack 256
.data
SCH3114_IO EQU A00h
.code
org 100h
.STARTup
;=====================================================
;47H
;enable WDT function bit [0]=0Ch
;=====================================================
mov dx,SCH3114_IO + 47h
mov al,0Ch
out dx,al
;=====================================================
;65H
;bit [1:0]=Reserved
;bit [6:2]Reserve=00000
;bit [7] WDT time-out Value Units Select
;Minutes=0 (default) Seconds=1
;=====================================================
mov dx,SCH3114_IO + 65h ;
mov al,080h
out dx,al
;=====================================================
;66H
;WDT timer time-out value
;bit[7:0]=0~255
;=====================================================
mov dx,SCH3114_IO + 66h
mov al,01h
out dx,al
;=====================================================
;bit[0] status bit R/W
;WD timeout occurred =1
```

```
;WD timer counting = 0
;=====================================================
mov dx,SCH3114_IO + 68h
mov al,01h
out dx,al
.exit
END
```

B.2 GPIO Sample Code

```
;=====================================================
;       Get Number of GPIO group
;       one group mean 8 gpio pins(one GPIO Chip)
; Input:
;       ax=5E87h
;       bh=00h
; output:
;       ax=5E78         ;function success, other value means function fail
;       cl= n group of gpio
;=====================================================

;=====================================================
;       Get GPIO Config
; Input:
;       ax=5E87h
;       bh=01h
;       cl= n ; n means which group of GPIO you want to get
; output:
;       ax=5E78         ;function success, other value means function fail
;       bl= the n group of gpio config
;           bit 0 = gpio 0 , 0 => output pin; 1 => input pin
;           bit 1 = gpio 1 , 0 => output pin; 1 => input pin
;               .....
;           bit 7 = gpio 7 , 0 => output pin; 1 => input pin
;=====================================================

;=====================================================;
Set GPIO Config
; Input:
;       ax=5E87h
;       bh=02h
;       cl= n ; n means which group of GPIO you want to set
;       bl= the n group of gpio config
;           bit 0 = gpio 0 , 0 => output pin; 1 => input pin
;           bit 1 = gpio 1 , 0 => output pin; 1 => input pin
;               .....
```

```
;          bit 7 = gpio 7 , 0 => output pin; 1 => input pin
; output:
;      ax=5E78        ;function success, other value means function fail
;=======================================================

;=======================================================;
Get GPIO status
; Input:
;      ax=5E87h
;      bh=03h
;      cl= n ; n means which group of GPIO you want to get
; output:
;      ax=5E78        ;function success, other value means function fail
;      bl= the n group of gpio status
;          bit 0 = gpio 0 , 0 => Low; 1 => High
;          bit 1 = gpio 1 , 0 => Low; 1 => High
;              .....
;          bit 7 = gpio 7 , 0 => Low; 1 => High
;=======================================================

;=======================================================
;      Set GPIO status
; Input:
;      ax=5E87h
;      bh=04h
;      cl= n ; n means which group of GPIO you want to set
;      bl= the n group of gpio status
;          bit 0 = gpio 0 , 0 => Low; 1 => High
;          bit 1 = gpio 1 , 0 => Low; 1 => High
;              .....
;          bit 7 = gpio 7 , 0 => Low; 1 => High
; output:
;      ax=5E78        ;function success, other value means function fail
;=============================================================
              mov     ax,5e87h
              mov     bh,00h
              int     15h
              cmp     ax,5e78h
              je      next_test

              lea     dx, Error_Str1
              mov     ah,09h
              int     21h
              jmp     Finish_Test
next_test:
```

```
    xor     ch,ch
    push    cx              ;save NO. of GPIO chip
;1.Set GPIO 0,2,4,6 as output, GPI 1,3,5,7 as input
    mov     ax,5e87h
    mov     bx,02aah
    int     15h
;2. Set GPIO 0,2,4,6 Output Low
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,0400h
    int     15h
;3. Check GPI 1,3,5,7 value
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,03FFh
    int     15h

    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    dec     cx

    mov     al,Fail_lenght
    mul     cl
    lea     dx, Fail_Str
    add     dx,ax
    cmp     bl,00
    jne     test_result


;4. Set GPIO 0,2,4,6 Output differential
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,0411h
    int     15h
;5. Check GPI 1,3,5,7 value
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,03FFh
    int     15h

    pop     cx              ;restore  NO. of GPIO chip
```

```
    push    cx              ;save NO. of GPIO chip
    dec     cx

    mov     al,Fail_lenght
    mul     cl
    lea     dx, Fail_Str
    add     dx,ax
    cmp     bl,33h
    jne    test_result

    cmp    al,00h
    jne    test_fail
 ;4.Set GPIO 1,3,5,7 as output,GPIO 0,2,4,6 as input
    pop     cx
    push    cx
    mov     ax,5e87h
    mov     bx,0255h
    int     15h
;5. Set GPIO 1,3,5,7 Output High
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,04ffh
    int     15h
;6. Check GPIO 0,2,4,6 value
    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    mov     ax,5e87h
    mov     bx,0300h
    int     15h

    pop     cx              ;restore  NO. of GPIO chip
    push    cx              ;save NO. of GPIO chip
    dec     cx

    mov     al,Fail_lenght
    mul     cl
    lea     dx, Fail_Str
    add     dx,ax
    cmp     bl,0ffh
    jne     test_result


 ;4. Set GPIO 1,3,5,7 Output differential
    pop     cx              ;restore  NO. of GPIO chip
```

```
            push    cx              ;save NO. of GPIO chip
            mov     ax,5e87h
            mov     bx,0422h
            int     15h
        ;5. Check GPI 0,2,4,6 value
            pop     cx              ;restore  NO. of GPIO chip
            push    cx              ;save NO. of GPIO chip
            mov     ax,5e87h
            mov     bx,03FFh
            int     15h

            pop     cx              ;restore  NO. of GPIO chip
            push    cx              ;save NO. of GPIO chip
            dec     cx

            mov     al,Fail_lenght
            mul     cl
            lea     dx, Fail_Str
            add     dx,ax
            cmp     bl,33h
            jne     test_result

            pop     cx              ;restore  NO. of GPIO chip
            push    cx              ;save NO. of GPIO chip
            dec     cx
            mov     al,Success_lenght
            mul     cl
            lea     dx, Success1_Str
            add     dx,ax

        ;Do Second PCA9554 test
        ;1.Set GPIO 0,2,4,6 as output, GPI 1,3,5,7 as input

test_result:
            mov     ah,09h
            int     21h
            pop     cx
            dec     cx
            jnz     next_test
    Finish_Test:
            popa
            .exit
```

Appendix C

System Assignments

C.1 System I/O Ports

Table C.1: System I/O Ports	
Addr. Range (Hex)	**Device**
000-01F	DMA Controller
20h–2Dh	Interrupt Controller
50h–52h	Timer/Counter
060-06F	8042 (keyboard controller)
070-07F	Real-time clock, non-maskable interrupt (NMI) mask
080-09F	DMA page register
0A0-0BF	0A0-0BF
0C0-0DF	DMA controller
170h–177h	IDE Controller
1F0h–1F7h	IDE Controller
2F8-2FF	Serial port 2
378-37F	Parallel printer port
3E8-3EF	Serial port 3
3F8-3FF	Serial port 1

C.2 1st MB Memory Map

Table C.2: 1st MB memory map	
Addr. Range (Hex)	**Device**
F0000h - FFFFFh	System ROM
D0000h - EFFFFh	Unused (reserved for Ethernet ROM)
C0000h - CE7FFh	Expansion ROM (for VGA BIOS)
B8000h - BFFFFh	CGA/EGA/VGA text
B0000h - B7FFFh	Unused
A0000h - AFFFFh	EGA/VGA graphics
00000h - 9FFFFh	Base memory

C.3 DMA Channel Assignments

Table C.3: DMA channel assignments

Channel	Function
0	Available
1	Reserved (audio)
2	Floppy disk (8-bit transfer)
3	Available (parallel port)
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

* Audio DMA select 1, 3, or 5
** Parallel port DMA select 1 (LPT2) or 3 (LPT1)

C.4 Interrupt Assignments

Table C.4: Interrupt assignments

Interrupt#	Interrupt source
IRQ0	Interval timer
IRQ1	Keyboard
IRQ2	Interrupt from controller 2 (cascade)
IRQ3	COM2
IRQ4	COM1
IRQ5	Reserved
IRQ6	Reserved
IRQ7	LPT
IRQ8	RTC
IRQ9	Reserved
IRQ10	Reserved
IRQ11	COM3
IRQ12	PS/2 mouse
IRQ13	Math Coprocessor
IRQ14	Primary IDE
IRQ15	Secondary IDE

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