MIC28500

75V/4A Hyper Speed Control™ Synchronous DC-DC Buck Regulator

SuperSwitcher II™

General Description

The Micrel MIC28500 is an adjustable frequency, synchronous buck regulator featuring a unique adaptive on-time control architecture. The MIC28500 operates over an input supply range of 30V to 75V and provides a regulated output of up to 4A of output current. The output voltage is adjustable down to 0.8V with a guaranteed accuracy of ±1%.

Micrel's Hyper Speed Control™ architecture allows for ultra-fast transient response while reducing the output capacitance and also makes (High V_{IN})/(Low V_{OUT}) operation possible. This adaptive t_{ON} ripple control architecture combines the advantages of fixed-frequency operation and fast transient response in a single device.

The MIC28500 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, foldback current limit, "hiccup" mode short-circuit protection and thermal shutdown.

All support documentation can be found on Micrel's web site at: www.micrel.com.

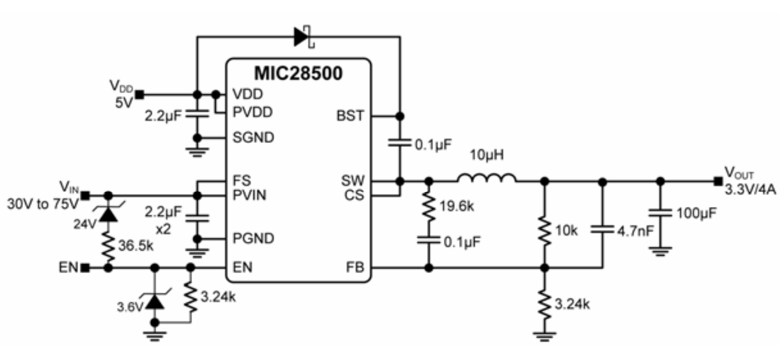
Features

- Hyper Speed Control™ architecture enables
  - High Delta V operation (V_{IN} = 75V and V_{OUT} = 0.8V)
  - Small output capacitance
- 30V to 75V voltage input
- Adjustable output down to 0.8V
- ±1% FB accuracy
- Any Capacitor™ Stable
  - Zero-ESR to high-ESR output capacitors
- 4A output current capability, up to 90% efficiency
- 100kHz to 500kHz switching frequency
- Internal compensation
- Foldback current-limit and "hiccup" mode short-circuit protection
- Thermal shutdown
- Supports safe startup into a pre-biased load
- –40°C to +125°C junction temperature range
- 28-pin 5mm × 6mm MLF® package

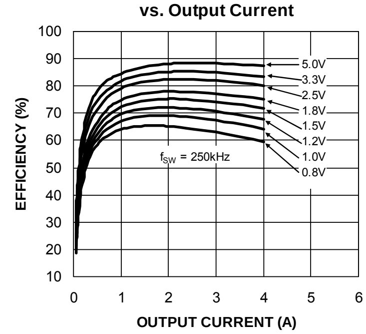
Applications

- Distributed power systems
- Communications/networking infrastructure
- Set-top box, gateways and routers
- Printers, scanners, graphic cards and video cards

Typical Application



Efficiency (V_{IN} = 48V) vs. Output Current



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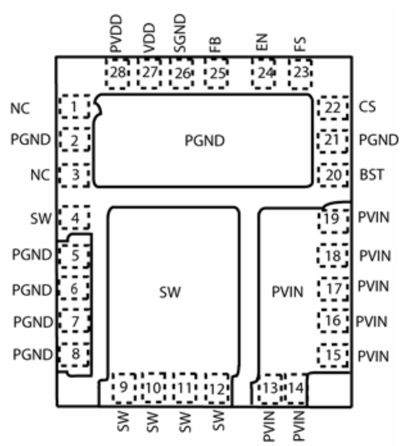
Ordering Information

Part Number	Voltage	Switching Frequency	Junction Temperature Range	Package	Lead Finish
MIC28500YJL	Adjustable	Adjustable	–40°C to +125°C	28-pin 5mm × 6mm MLF®	Pb-Free

Pin Configuration



28-Pin 5mm × 6mm MLF® (YJL)

Pin Description

Pin Number	Pin Name	Pin Function
13, 14, 15, 16, 17, 18, 19	PVIN	High-Side internal N-channel MOSFET Drain Connection (Input): The PVIN operating voltage range is from 30V to 75V. Input capacitors between the PVIN pins and the power ground (PGND) are required and keep the connection short. Enabling the device below 30V VIN and under maximum loading could heat up the device beyond safe operating conditions.
24	EN	Enable (Input): A logic level control of the output. The EN pin is CMOS-compatible. Logic high or floating = enable, logic low = shutdown. In the off state, the V_{DD} supply current of the device is reduced (typically 0.7mA). Do not pull the EN pin above the V_{DD} supply. Enabling the device below 30V VIN and under maximum loading could heat up the device beyond safe operating conditions.
25	FB	Feedback (Input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
26	SGND	Signal ground. SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer, see PCB layout guidelines for details.
27	VDD	VDD Bias (Input): Power to the internal reference and control sections of the MIC28500. The VDD operating voltage range is from 4.5V to 5.5V. A 2.2µF ceramic capacitor from the VDD pin to the PGND pin must be placed next to the IC. VDD must be powered up at the same time or after PVIN to make the soft-start function correctly.
2, 5, 6, 7, 8, 21	PGND	Power Ground. PGND is the ground path for the MIC28500 buck converter power stage. The PGND pin connects to the sources of low-side N-Channel internal MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the signal ground (SGND) loop.
22	CS	Current Sense (Input): High current output driver return. The CS pin connects directly to the switch node. Due to the high-speed switching on this pin, the CS pin should be routed away from sensitive nodes. CS pin also senses the current by monitoring the voltage across the low-side internal MOSFET during OFF-time.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
20	BST	Boost (Output): Bootstrapped voltage to the high-side N-channel internal MOSFET driver. A Schottky diode is connected between the VDD pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the SW pin.
4, 9, 10, 11, 12	SW	Switch Node (Output): Internal connection for the high-side MOSFET source and low-side MOSFET drain.
23	FS	Frequency Setting Pin.
28	PVDD	Power Supply for gate driver of bottom MOSFET.
1, 3	NC	No Connect.

Absolute Maximum Ratings[1, 2]

PV_{IN} to PGND .... –0.3V to +76V
FS to PGND ....–0.3V to PV_{IN}
PV_{DD}, V_{DD} to PGND .... –0.3V to +6V
V_{SW}, V_{CS} to PGND ....–0.3V to (PV_{IN} +0.3V)
V_{BST} to V_{SW} .... –0.3V to 6V
V_{BST} to PGND .... –0.3V to 82V
V_{EN} to PGND ....–0.3V to (V_{DD} + 0.3V)
V_{FB} to PGND......................................–0.3V to (V_{DD} + 0.3V)
PGND to SGND .... –0.3V to +0.3V
Junction Temperature ....+150°C
Storage Temperature (T_S).........................–65°C to +150°C
Lead Temperature (soldering, 10sec)........................260°C

Operating Ratings[3]

Supply Voltage (PV_{IN}) .... 30V to 75V
Bias Voltage (PV_{DD}, V_{DD})................................. 4.5V to 5.5V
Enable Input (V_{EN})..0V to V_{DD}
Junction Temperature (T_J) ....–40°C to +125°C
Maximum Power Dissipation.....................................Note 4
Package Thermal Resistance[4]
5mm x 6mm MLF® (θ_{JA}) ....36°C/W

Electrical Characteristics[5]

$PV_{IN} = V_{FS} = 48V$, $V_{DD} = 5V$; $V_{BST} – V_{SW} = 5V$; $T_A = 25°C$, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min.	Typ.	Max.	Units
Power Supply Input					
Input Voltage Range (PV_{IN})		**30**		**75**	V
FS Voltage Range		**2**		**75**	V
V_{DD} Bias Voltage					
Operating Bias Voltage (V_{DD})		**4.5**	5	**5.5**	V
Under-Voltage Lockout Trip Level	V_{DD} Rising	**3.2**	3.85	**4.45**	V
UVLO Hysteresis			380		mV
Quiescent Supply Current (I_{VDD})	$V_{FB} = 1.5V$		1.4	**3**	mA
Shutdown Supply Current (I_{VDD})	$V_{DD} = V_{BST} = 5.5V$, $V_{IN} = 48V$ SW = unconnected, $V_{EN} = 0V$		0.7	**2**	mA
Reference					
Feedback Reference Voltage	0°C ≤ T_J ≤ 85°C (±1.0%)	**0.792**	0.8	**0.808**	V
	–40°C ≤ T_J ≤ 125°C (±1.5%)	**0.788**	0.8	**0.812**	
Load Regulation	I_{OUT} = 0A to 4A		0.04		%
Line Regulation	PV_{IN} = 30 to 75V		0.1		%
FB Bias Current	$V_{FB} = 0.8V$	**-0.5**	0.005	**0.5**	µA
Enable Control					
EN Logic Level High	4.5V < V_{DD} < 5.5V	**1.2**	0.85		V
EN Logic Level Low	4.5V < V_{DD} < 5.5V		0.78	**0.4**	V
EN Bias Current	$V_{EN} = 0V$		50	**100**	µA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
3. The device is not guaranteed to function outside operating range.
4. $PD_{(MAX)} = (T_{J(MAX)} – T_A)/ \theta_{JA}$, where θ_{JA} depends upon the printed circuit layout. See “Applications Information.”
5. Specification for packaged product only.

Electrical Characteristics[5] (Continued)

$PV_{IN} = V_{FS} = 48V$, $V_{DD} = 5V$; $V_{BST} - V_{SW} = 5V$; $T_A = 25°C$, unless noted. **Bold** values indicate $-40°C \le T_J \le +125°C$.

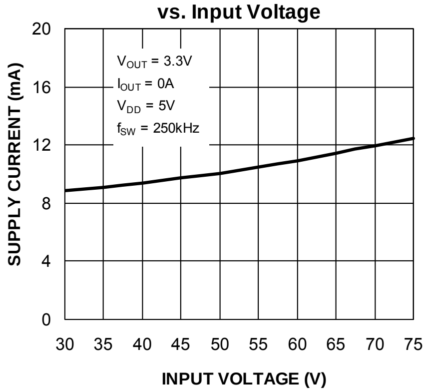
Parameter	Condition	Min.	Typ.	Max.	Units
Oscillator					
Switching Frequency [6]	$V_{FS}=PV_{IN}$	**375**	500	**625**	kHz
Maximum Duty Cycle [7]	$V_{FB} = 0V$, $V_{FS}=PV_{IN}$		82		%
Minimum Duty Cycle	$V_{FB} > 0.8V$		0		%
Minimum Off-time			360		ns
Soft-Start					
Soft-Start time			6		ms
Short Circuit Protection					
Current-Limit Threshold	$V_{FB} = 0.8V$, $T_J = 25°C$	5.5	7	9	A
	$V_{FB} = 0.8V$, $T_J = 125°C$	4.2	5.5	8.5	A
Short-Circuit Current	$V_{FB} = 0V$	2	3.6	5.2	A
Internal FETs					
Top-MOSFET $R_{DS (ON)}$	$I_{SW} = 1A$		175		mΩ
Bottom-MOSFET $R_{DS (ON)}$	$I_{SW} = 1A$		31		mΩ
SW Leakage Current	$PV_{IN} = 36V$, $V_{SW} = 36V$, $V_{EN} = 0V$, $V_{BST} = 41V$			**55**	µA
PV_{IN} Leakage Current	$PV_{IN} = 36V$, $V_{SW} = 0V$, $V_{EN} = 0V$, $V_{BST} = 41V$			**55**	µA
Thermal Protection					
Over-Temperature Shutdown	T_J Rising		**160**		°C
Over-Temperature Shutdown Hysteresis			**25**		°C

Notes:

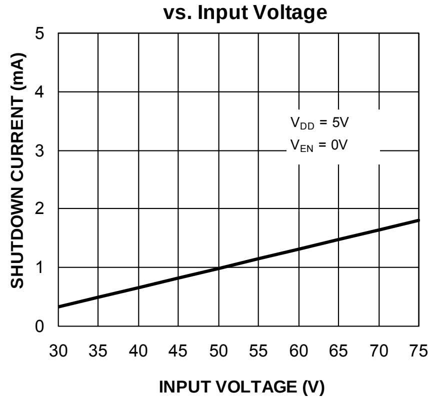
6. Measured in test mode.
7. The maximum duty-cycle is limited by the fixed mandatory off-time t_{OFF} of typically 360ns.

Typical Characteristics

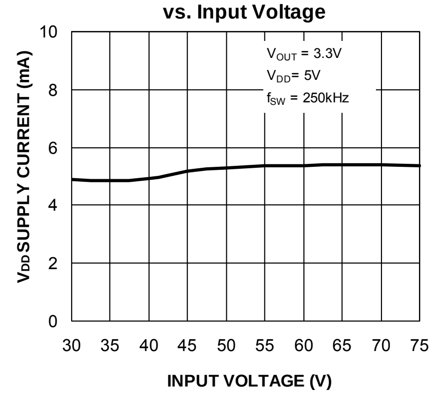
V_{IN} Operating Supply Current vs. Input Voltage



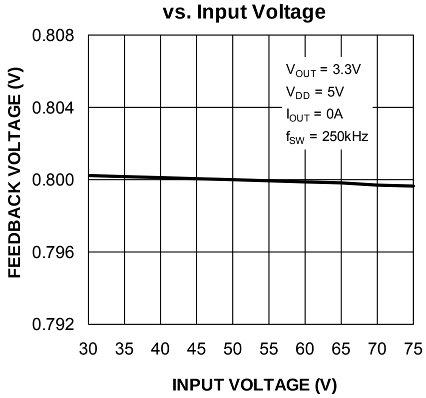
V_{IN} Shutdown Current vs. Input Voltage



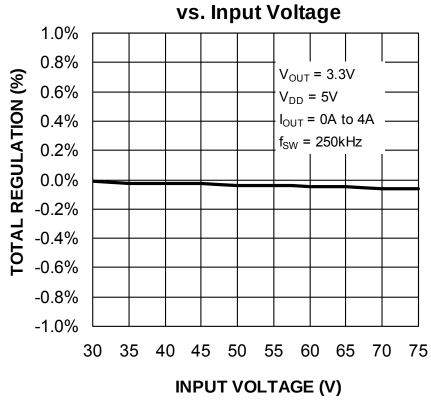
V_{DD} Operating Supply Current vs. Input Voltage



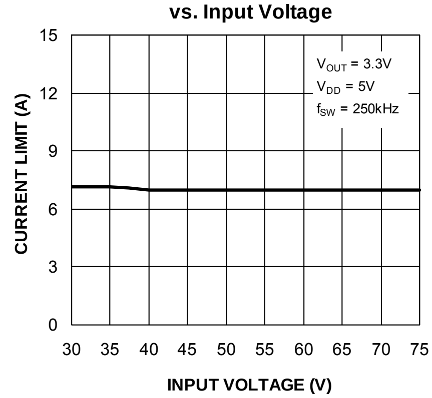
Feedback Voltage vs. Input Voltage



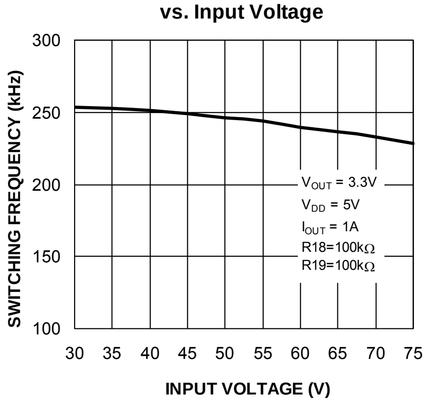
Total Regulation vs. Input Voltage



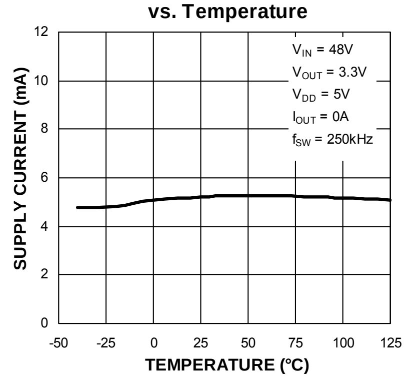
Current Limit vs. Input Voltage



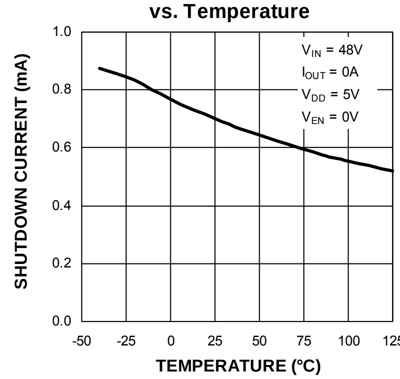
Switching Frequency vs. Input Voltage



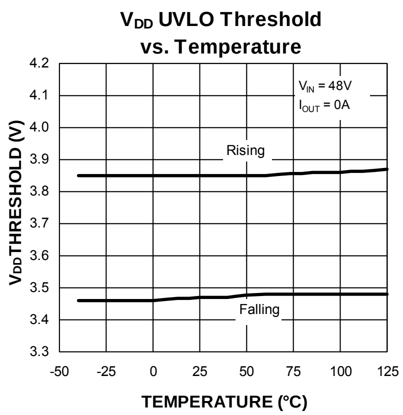
V_{DD} Operating Supply Current vs. Temperature

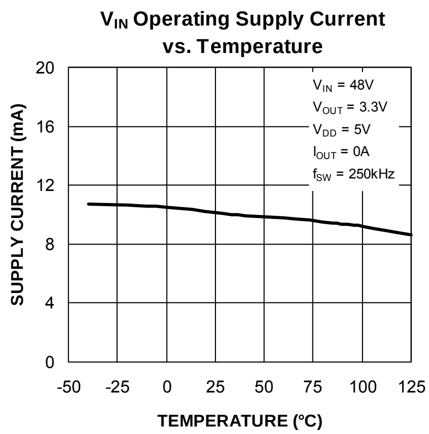


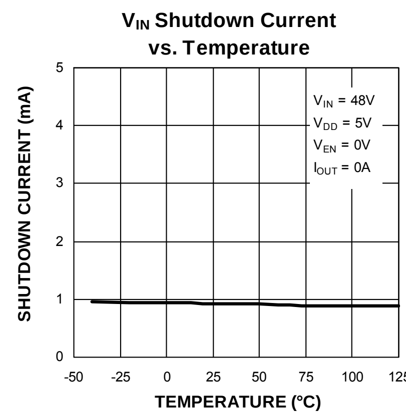
V_{DD} Shutdown Current vs. Temperature

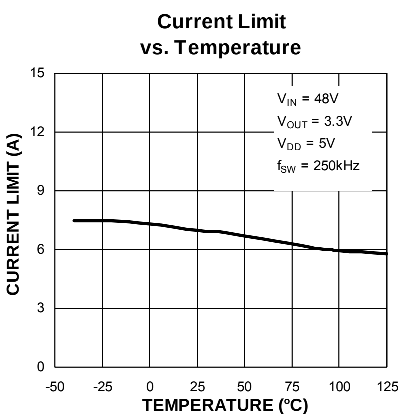


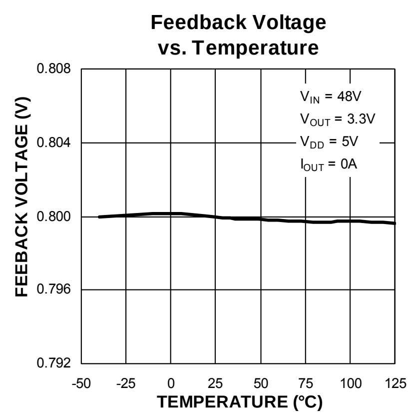
Typical Characteristics (Continued)

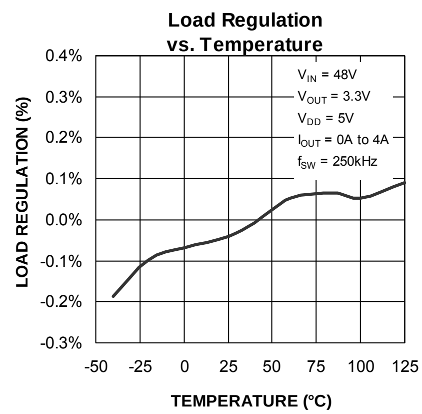


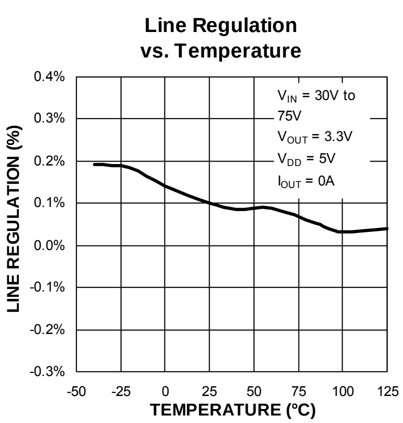


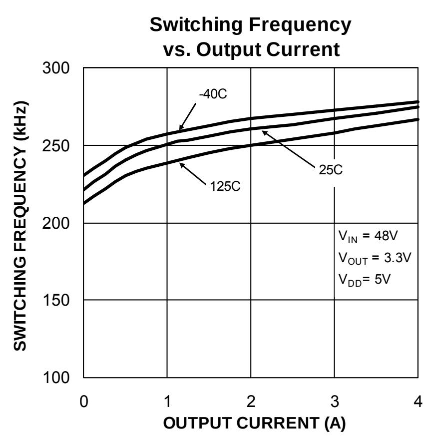


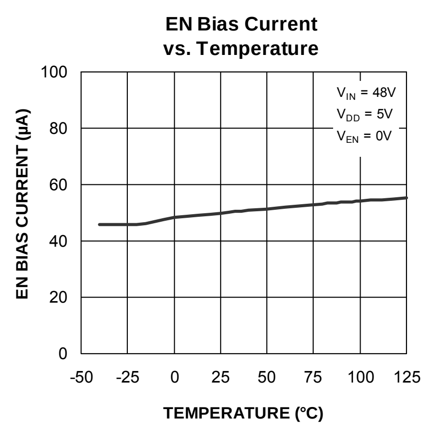




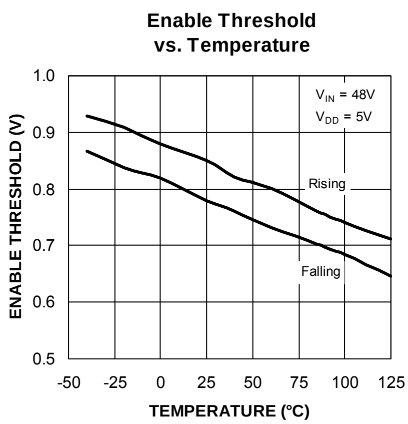


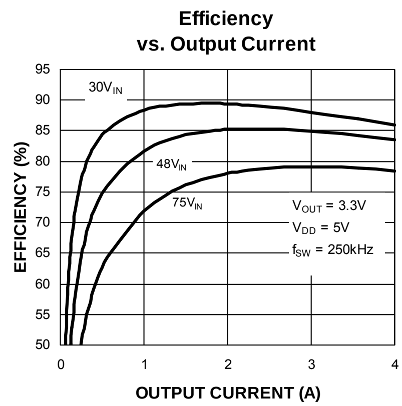


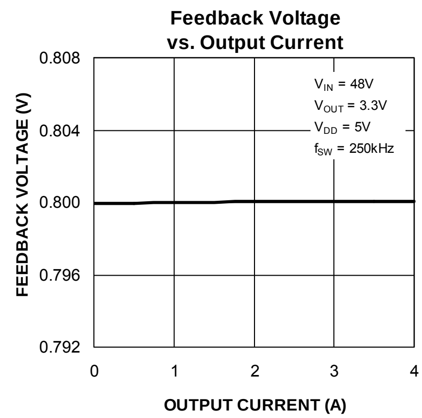


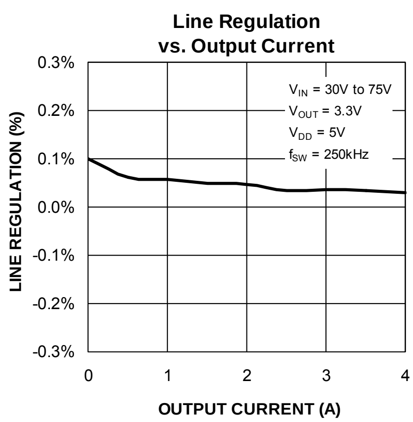


Typical Characteristics (Continued)



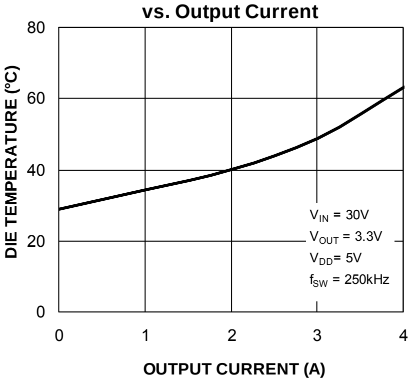




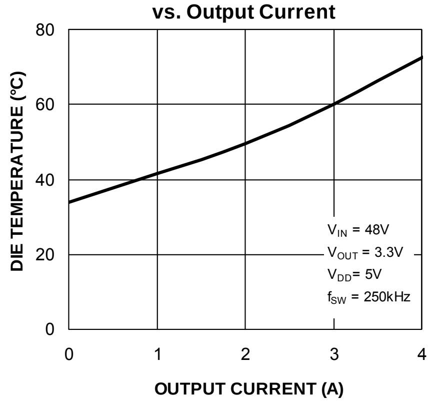


Typical Characteristics (Continued)

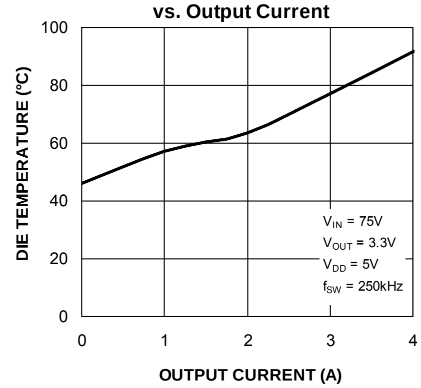
Die Temperature* (V_{IN} = 30V) vs. Output Current



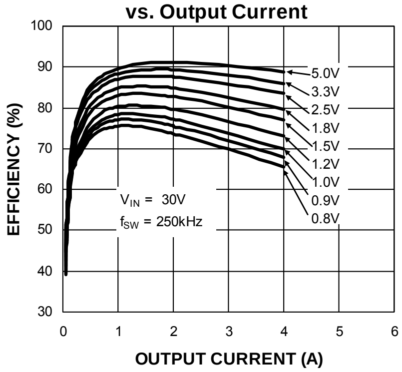
Die Temperature* (V_{IN} = 48V) vs. Output Current



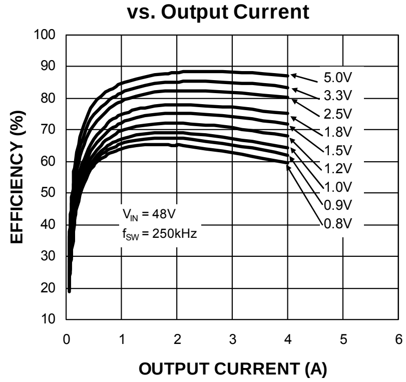
Die Temperature* (V_{IN} = 75V) vs. Output Current



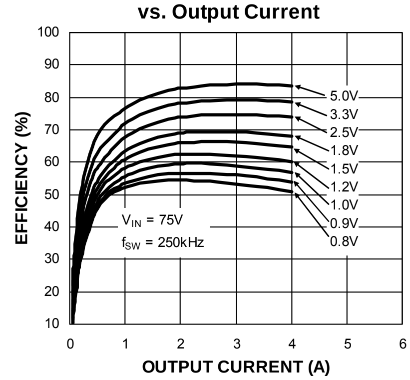
Efficiency (V_{IN} = 30V) vs. Output Current



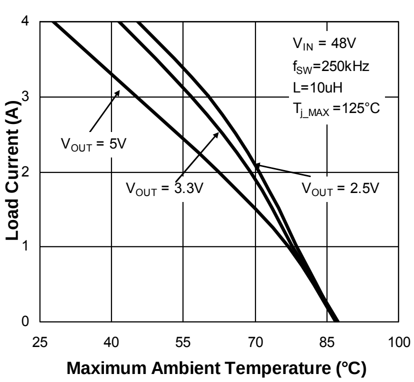
Efficiency (V_{IN} = 48V) vs. Output Current



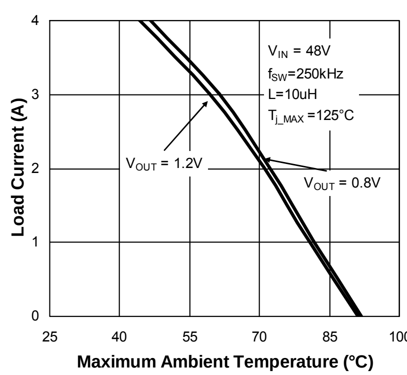
Efficiency (V_{IN} = 75V) vs. Output Current



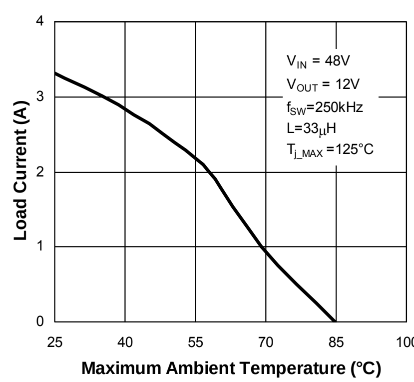
Thermal Derating



Thermal Derating

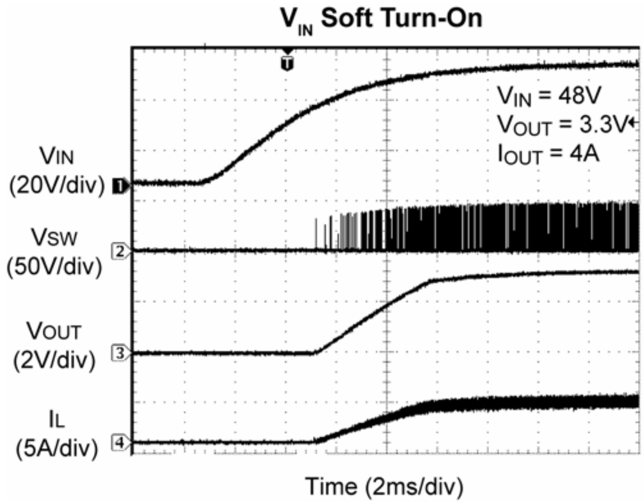


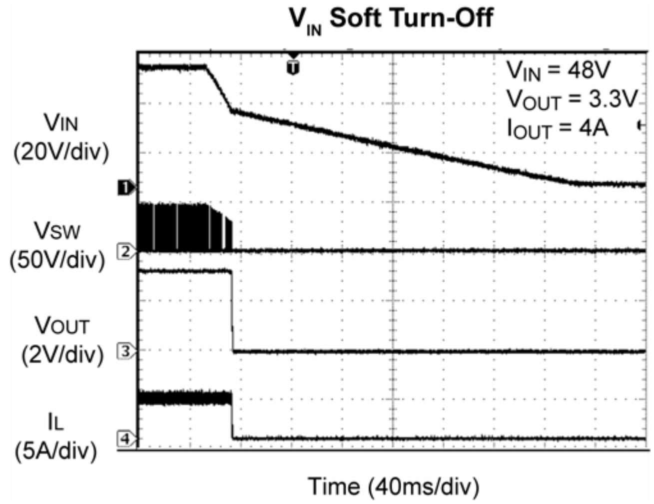
Thermal Derating

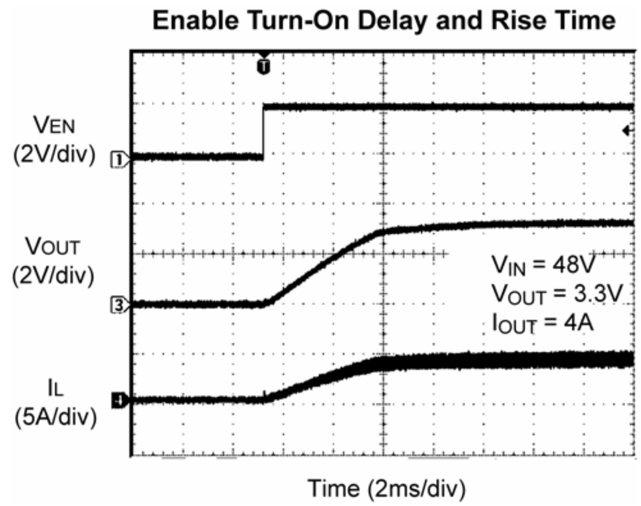


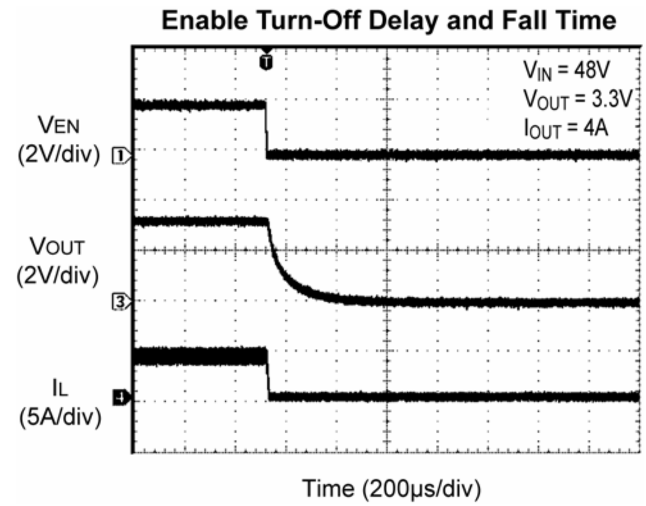
Die Temperature* : The temperature measurement was taken at the hottest point on the MIC28500 case mounted on a 5 square inch 4 layer, 0.62", FR-4 PCB with 2oz. finish copper weight per layer, see Thermal Measurement section. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

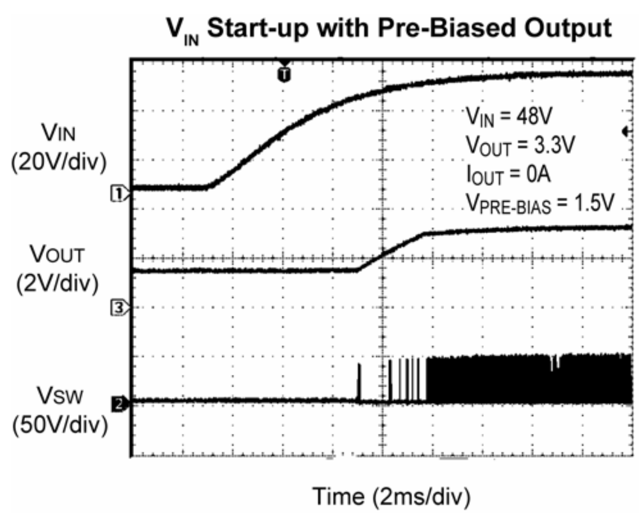
Functional Characteristics

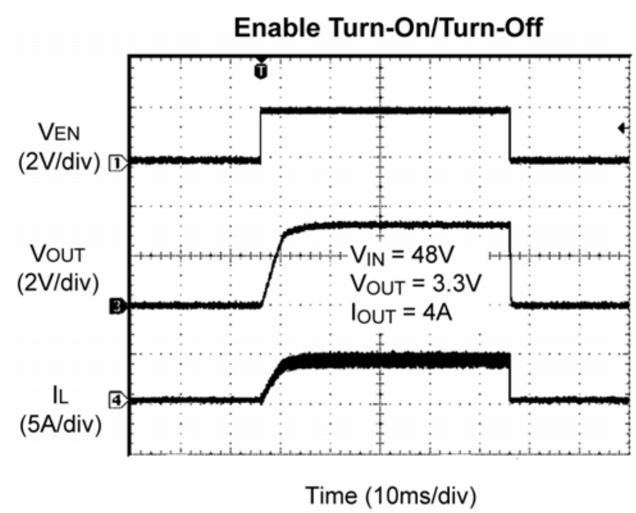




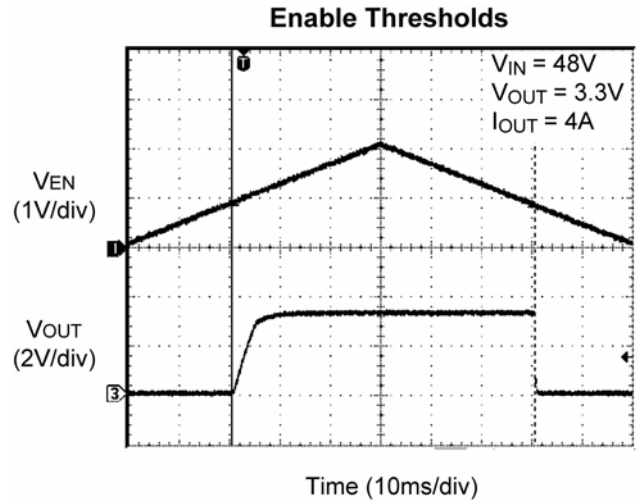


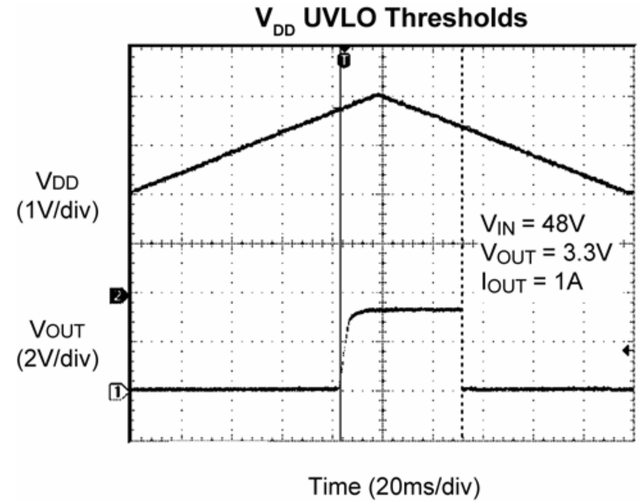


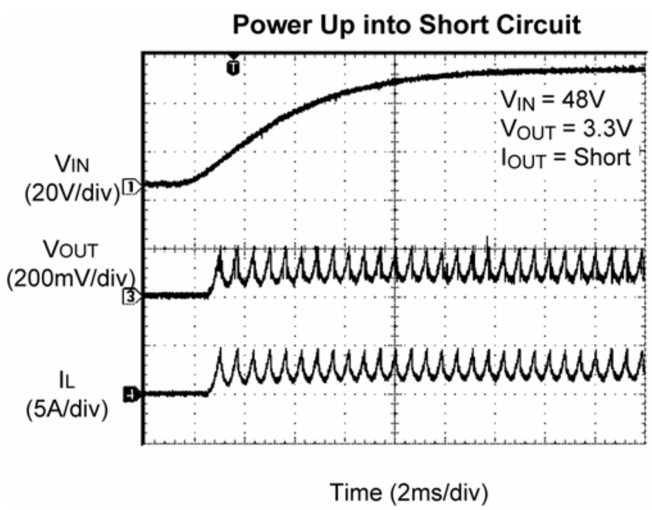


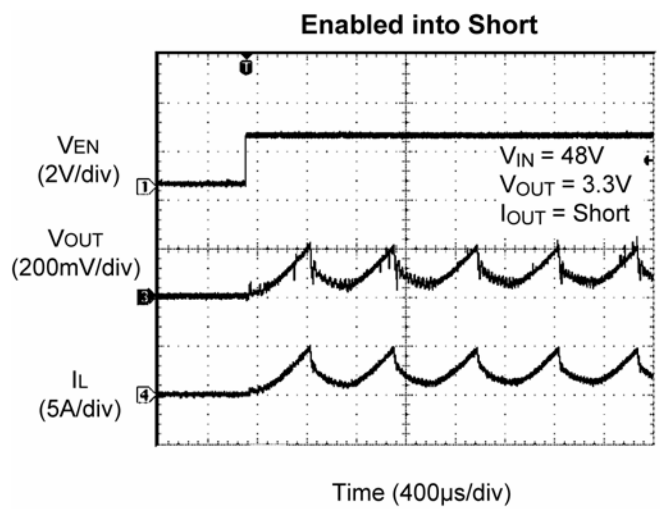


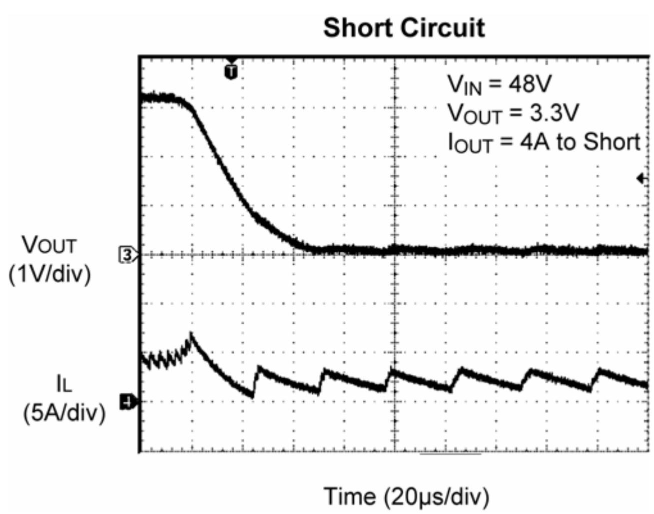
Functional Characteristics (Continued)

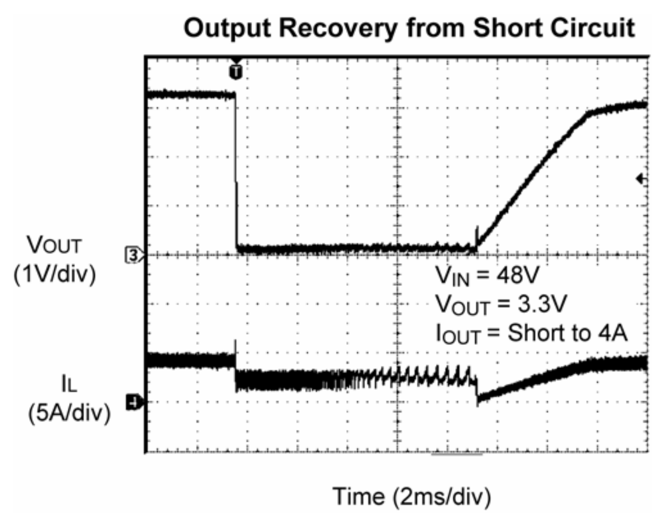




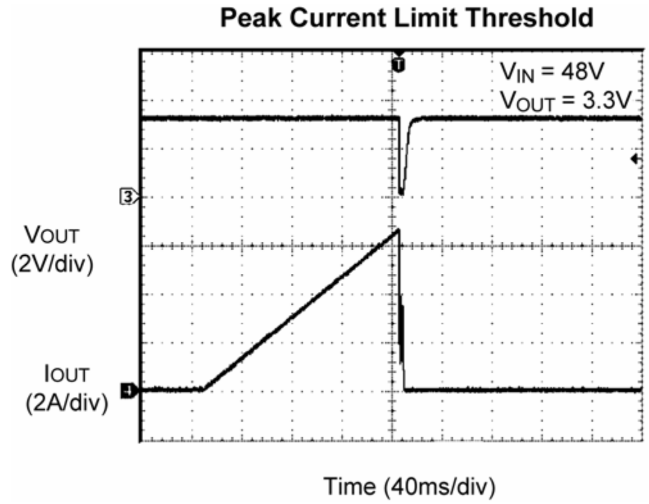


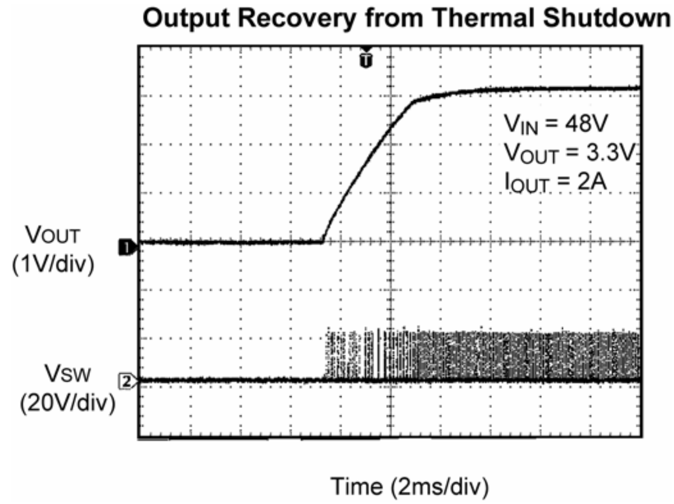


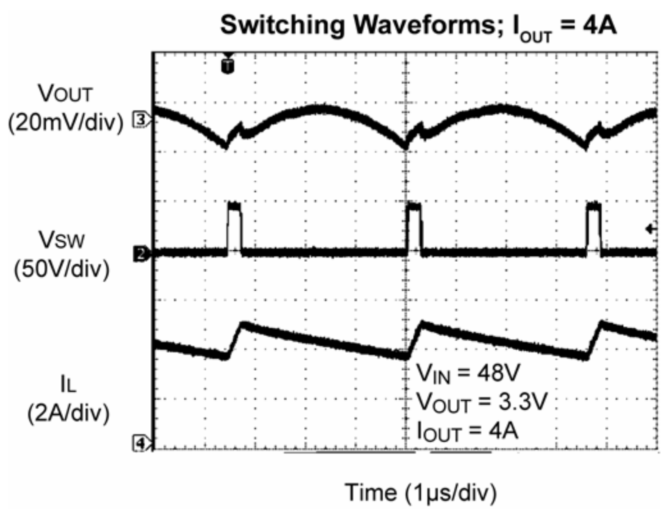


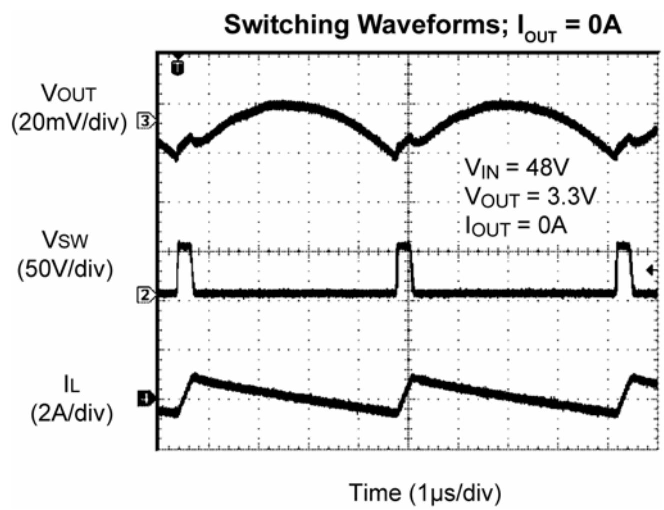


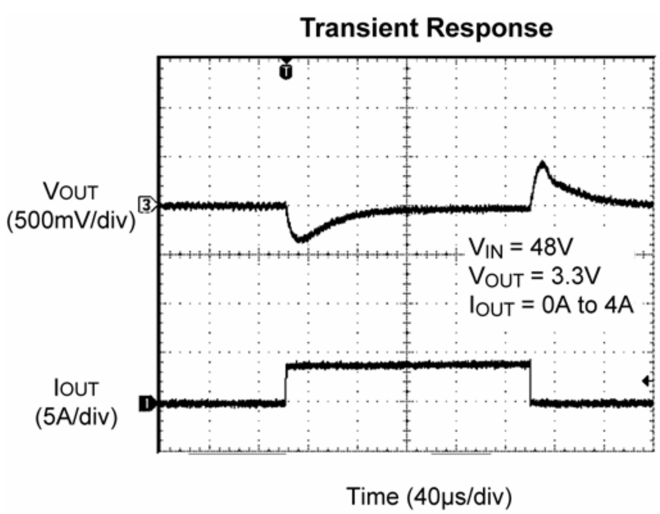
Functional Characteristics (Continued)











Functional Diagram

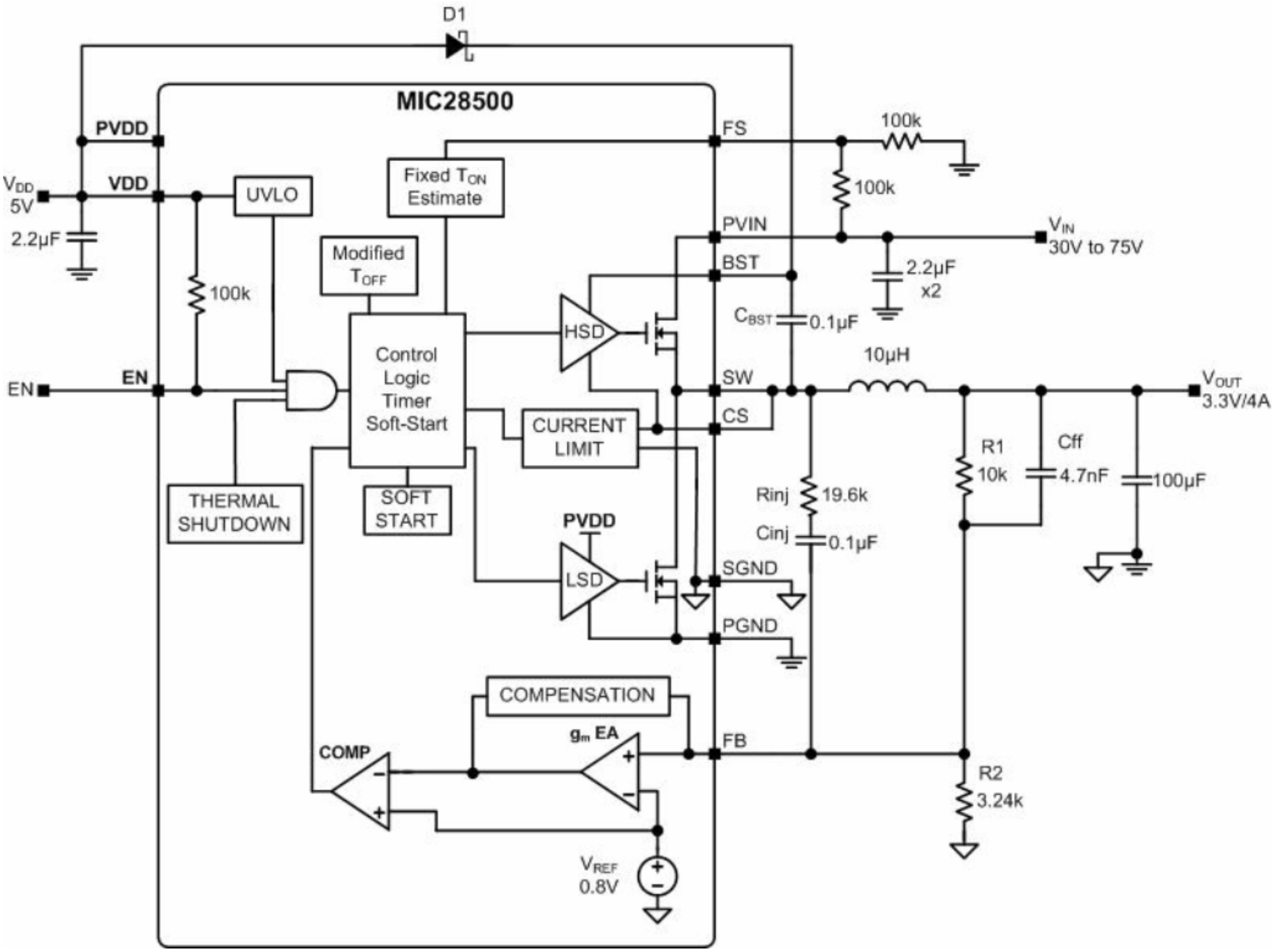


Figure 1. MIC28500 Block Diagram

Functional Description

The MIC28500 is an adaptive ON-time synchronous step-down DC-DC regulator. It is designed to operate over a wide input voltage range from, 30V to 75V, and provides a regulated output voltage at up to 4A of output current. A digitally modified adaptive ON-time control scheme is employed in to obtain a constant switching frequency and to simplify the control compensation. Over current protection is implemented without the use of an external sense resistor. The device includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

Theory of Operation

Figure 1 illustrates the block diagram for the control loop of the MIC28500. The output voltage is sensed by the MIC28500 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage V_{REF} at the error comparator through a low gain transconductance (g_m) amplifier. If the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "FIXED t_{ON} ESTIMATION" circuitry:

$$t_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad \text{Eq. 1}$$

where V_{OUT} is the output voltage and V_{IN} is the power stage input voltage and f_{SW} is the switching frequency.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(min)}$, which is about 360ns, then the MIC28500 control logic will apply the $t_{OFF(min)}$ instead. The minimum $t_{OFF(min)}$ period is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET. The maximum duty cycle is obtained from the 360ns $t_{OFF(min)}$:

$$D_{max} = \frac{t_S - t_{OFF(min)}}{t_S} = 1 - \frac{360ns}{t_S} \quad \text{Eq. 2}$$

where $t_S = 1/f_{SW}$. It is not recommended to use MIC28500 with a OFF-time close to $t_{OFF(min)}$ during steady-state operation..

The actual ON-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the V_{DD} voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 75V to 1.0V. The minimum t_{ON} measured on the MIC28500 evaluation board is about 184ns. During load transients, the switching frequency is changed due to the varying OFF-time.

Figure 2 shows the MIC28500 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

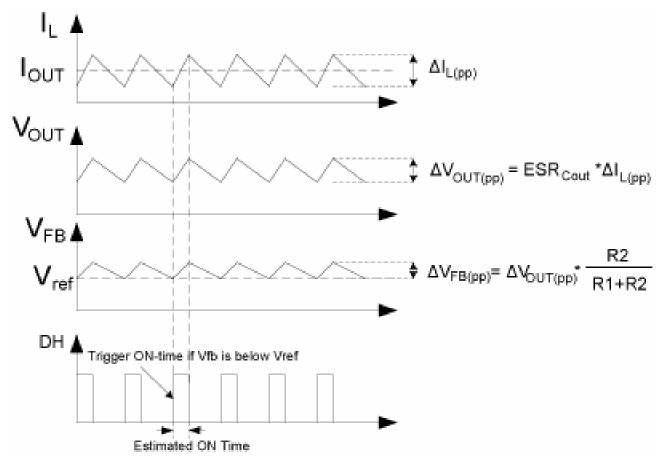


Figure 2. MIC28500 Control Loop Timing

Figure 3 shows the operation of the MIC28500 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(min)}$ is generated to charge C_{BST} since the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC28500 converter.

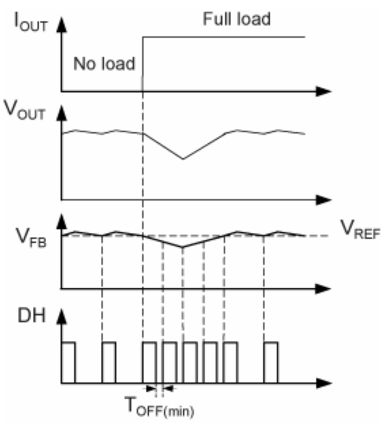


Figure 3. MIC28500 Load Transient Response

Unlike true current-mode control, the MIC28500 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC28500 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to "Ripple Injection" subsection in *Application Information* for more details about the ripple injection technique.

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC28500 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 6ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. V_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

Current Limit

The MIC28500 uses the $R_{DS(ON)}$ of the internal low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC28500 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. If the peak inductor current is greater than 7A, then the MIC28500 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called "hiccup mode" and its purpose is to protect the downstream load in case of a hard short. The current-limit threshold has a foldback characteristic related to the feedback voltage, as shown in Figure 4.

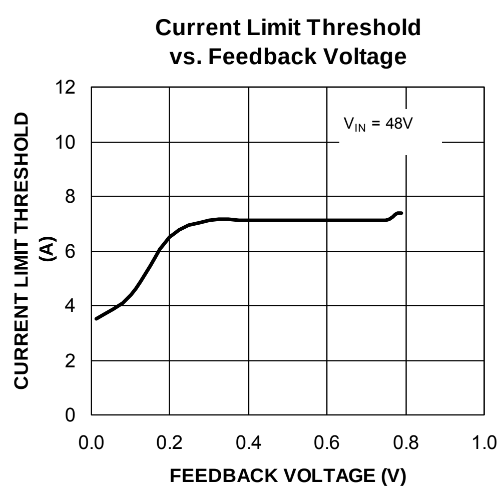


Figure 4. MIC28500 Current Limit Foldback Characteristic

Internal MOSFET Gate Drive

Figure 1 (Block Diagram) shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e. $\Delta BST = 10mA \times 3.33\mu s/0.1\mu F = 333mV$. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G, which is in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the PV_{DD} supply voltage. The nominal low-side gate drive voltage is PV_{DD} and the nominal high-side gate drive voltage is approximately $PV_{DD} – V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

Setting the Switching Frequency

The MIC28500 is an adjustable-frequency, synchronous buck regulator featuring a unique digitally modified adaptive on-time control architecture. The switching frequency can be adjusted between 100kHz and 500kHz by changing the resistor divider connected network consisting of R18 and R19.

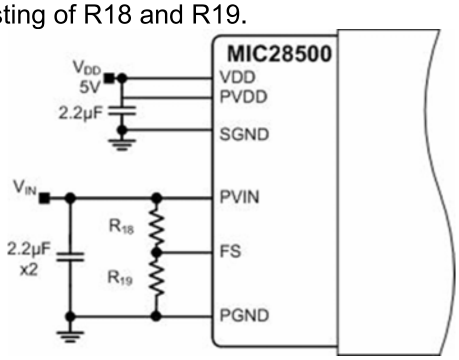


Figure 5. Switching Frequency Adjustment

The following formula gives the estimated switching frequency:

$$f_{SW\_ADJ} = f_O \times \frac{R_{19}}{R_{18} + R_{19}} \qquad \text{Eq. 2}$$

Where f_O = Switching Frequency when R18 is 100k and R19 being open, f_O should be typically 500kHz. For more precise setting, it is recommended to use the following graph.

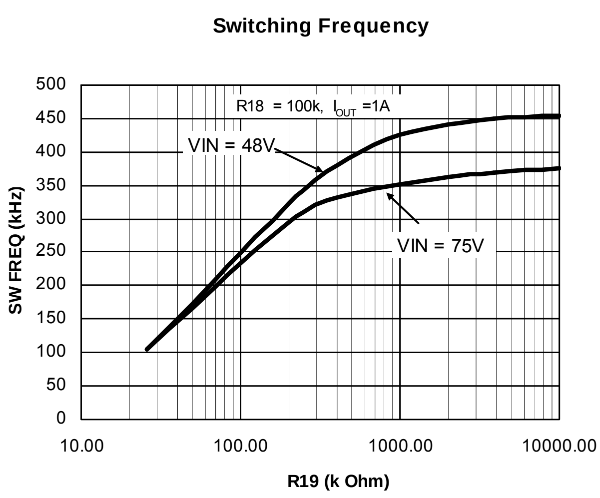


Figure 6. Switching Frequency vs. R19

The evaluation board design is optimized for a switching frequency of 250kHz. If the switching frequency is programmed to either lower end or higher end, the design needs optimization.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by Equation 3:

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times 20\% \times I_{OUT(max)}} \qquad \text{Eq. 3}$$

where:

f_{SW} = switching frequency, 300kHz

20% = ratio of AC ripple current to DC output current

$V_{IN(max)}$ = maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times L} \qquad \text{Eq. 4}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)} \qquad \text{Eq. 5}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^{\ 2} + \frac{\Delta I_{L(PP)}^{\ 2}}{12}} \qquad \text{Eq. 6}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC28500 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 7:

$$P_{INDUCTOR(Cu)} = I_{L(RMS)}^2 \times R_{WINDING} \qquad \text{Eq. 7}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature:

$$P_{WINDING(Ht)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \qquad \text{Eq. 8}$$

where:

T_H = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated:

$$ESR_{C_{OUT}} \le \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \qquad \text{Eq. 9}$$

where:

$\Delta V_{OUT(pp)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 10:

$$\Delta V_{OUT(pp)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2} \qquad \text{Eq. 10}$$

where:

C_{OUT} = output capacitance value

f_{SW} = switching frequency

As described in the "Theory of Operation" subsection in *Functional Description*, the MIC28500 requires at least 20mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Please refer to the "Ripple Injection" subsection for more details.

The voltage rating of the capacitor should be 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 11:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \qquad \text{Eq. 11}$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}^2 \times ESR_{C_{OUT}} \qquad \text{Eq. 12}$$

Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(pk)} \times C_{ESR} \qquad \text{Eq. 13}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{CIN(RMS)} \approx I_{OUT(max)} \times \sqrt{D \times (1-D)} \qquad \text{Eq. 14}$$

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = I_{CIN(RMS)}{}^2 \times C_{ESR} \qquad \text{Eq. 15}$$

Ripple Injection

The V_{FB} ripple required for proper operation of the MIC28500 g_m amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10mV to 20mV, and the feedback voltage ripple is less than 20mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator can't sense it, then the MIC28500 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1) Enough ripple at the feedback voltage due to the large ESR of the output capacitors.

As shown in Figure 7a, the converter is stable without any ripple injection. The feedback voltage ripple is:

$$\Delta V_{FB(pp)} = \frac{R2}{R1+R2} \times ESR_{C_{OUT}} \times \Delta I_{L(pp)} \qquad \text{Eq. 16}$$

where $\Delta I_{L(pp)}$ is the peak-to-peak value of the inductor current ripple.

2) Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

The output voltage ripple is fed into the FB pin through a feedforward capacitor C_{ff} in this situation, as shown in Figure 7b. The typical C_{ff} value is between 1nF and 22nF.

With the feedforward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

$$\Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)} \qquad \text{Eq. 17}$$

3) Virtually no ripple at the FB pin voltage due to the very low ESR of the output capacitors.

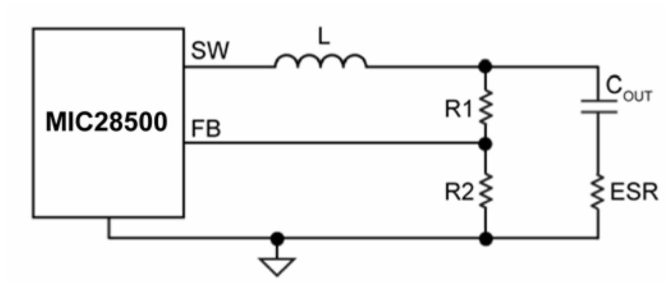


Figure 7a. Enough Ripple at FB

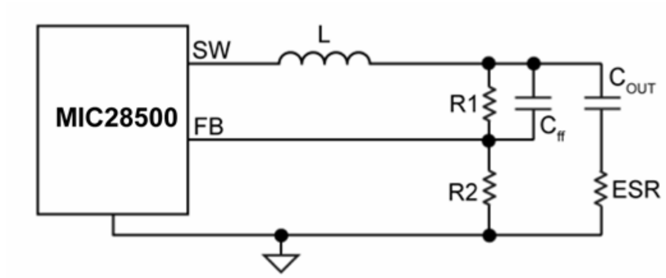


Figure 7b. Inadequate Ripple at FB

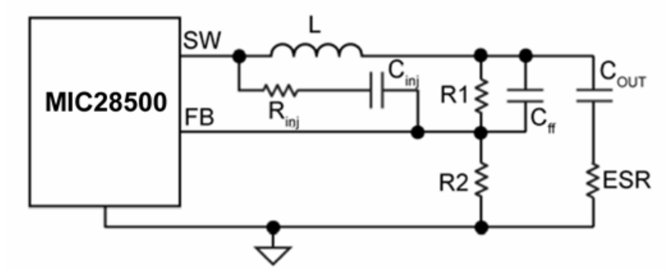


Figure 7c. Invisible Ripple at FB

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{inj} and a capacitor C_{inj}, as shown in Figure 7c.

The injected ripple is:

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \qquad \text{Eq. 18}$$

$$K_{div} = \frac{R1//R2}{R_{inj} + R1//R2} \qquad \text{Eq. 19}$$

where

V_{IN} = Power stage input voltage

D = duty cycle

f_{SW} = switching frequency

$\tau = (R1//R2//R_{inj}) \times C_{ff}$

In Equations 18 and 19, it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1 \qquad \text{Eq. 20}$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a C_{ff} of 1nF to 22nF can easily satisfy the large time constant requirements. Also, a 100nF injection capacitor C_{inj} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select C_{ff} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{ff} is 1nF to 22nF if R1 and R2 are in kΩ range.

Step 2. Select R_{inj} according to the expected feedback voltage ripple using Equation 21:

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1-D)} \qquad \text{Eq. 21}$$

Then the value of R_{inj} is obtained as:

$$R_{inj} = (R1//R2) \times \left(\frac{1}{K_{div}} - 1\right) \qquad \text{Eq. 22}$$

Step 3. Select C_{inj} as 100nF, which could be considered as short for a wide range of the frequencies.

Setting Output Voltage

The MIC28500 requires two resistors to set the output voltage as shown in Figure 8.

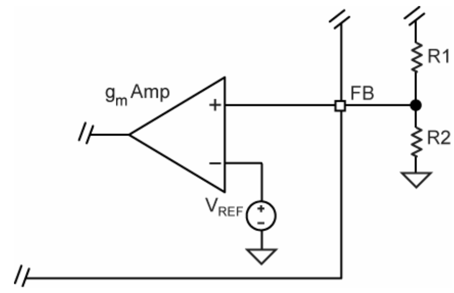


Figure 8. Voltage-Divider Configuration

The output voltage is determined by Equation 23:

$$V_O = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \qquad \text{Eq. 23}$$

where, V_{FB} = 0.8V. A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}} \qquad \text{Eq. 24}$$

The inverting input voltage V_{INJ} is clamped to 1.2V. As the injected ripple increases, the swing of V_{INJ} will be clamped. The clamped V_{INJ} reduces the line regulation because it is reflected back as a DC error on the FB terminal.

Thermal Measurements

Measuring the IC's case temperature is recommended to ensure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher then (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.

External V_{IN} Limiter Circuit

The external V_{IN} limiter circuit can be implemented either on EN pin or VDD pin. Only one of these V_{IN} limiter circuits is required. The external V_{IN} limiter circuit limits the minimum input to 30V. If the minimum input in certain applications is more than 30V then neither of these limiter circuits is needed. Enabling the device below 30V VIN and under maximum loading could heat up the device beyond safe operating conditions. The following figures show the external V_{IN} limiter circuit on EN and VDD pins Figure 9A and Figure 9B respectively. The V_{IN} limiter on EN consists of D5, R22, D6, R23 and V_{IN} limiter on the VDD pin along with VDD supply regulator consists of D4, R14, D2, and Q1.

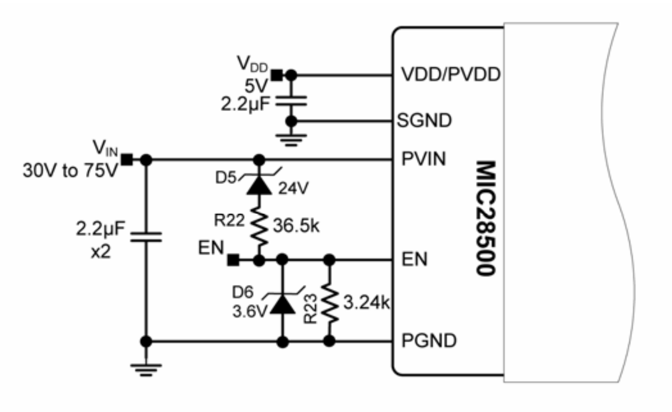


Figure 9A: V_{IN} Limiter On EN pin

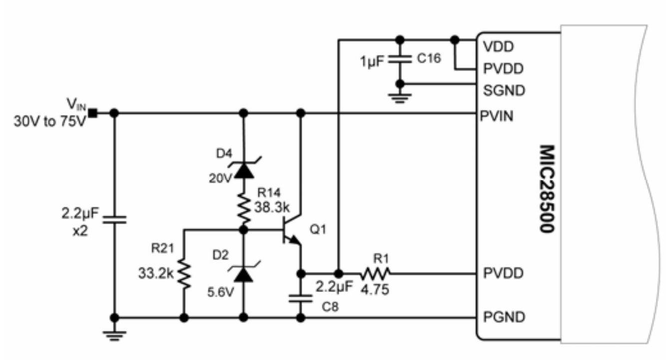


Figure 9B: V_{IN} Limiter On VDD pin

PCB Layout Guidelines

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths. Thickness of the copper planes is also important in terms of dissipating heat. The 2oz copper thickness is adequate from thermal point of view and also thick copper plain helps in terms of noise immunity. Keep in mind thinner planes can be easily penetrated by noise

The following guidelines should be followed to insure proper operation of the MIC28500 converter.

IC

- The 2.2µF ceramic capacitor, which is connected to the VDD pin, must be located right at the IC. The VDD pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the VDD and PGND pins.
- The signal ground pin (SGND) must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- Place the input capacitor next to the power pins.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The CS pin should be connected directly to the SW pin to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

Evaluation Board Schematic

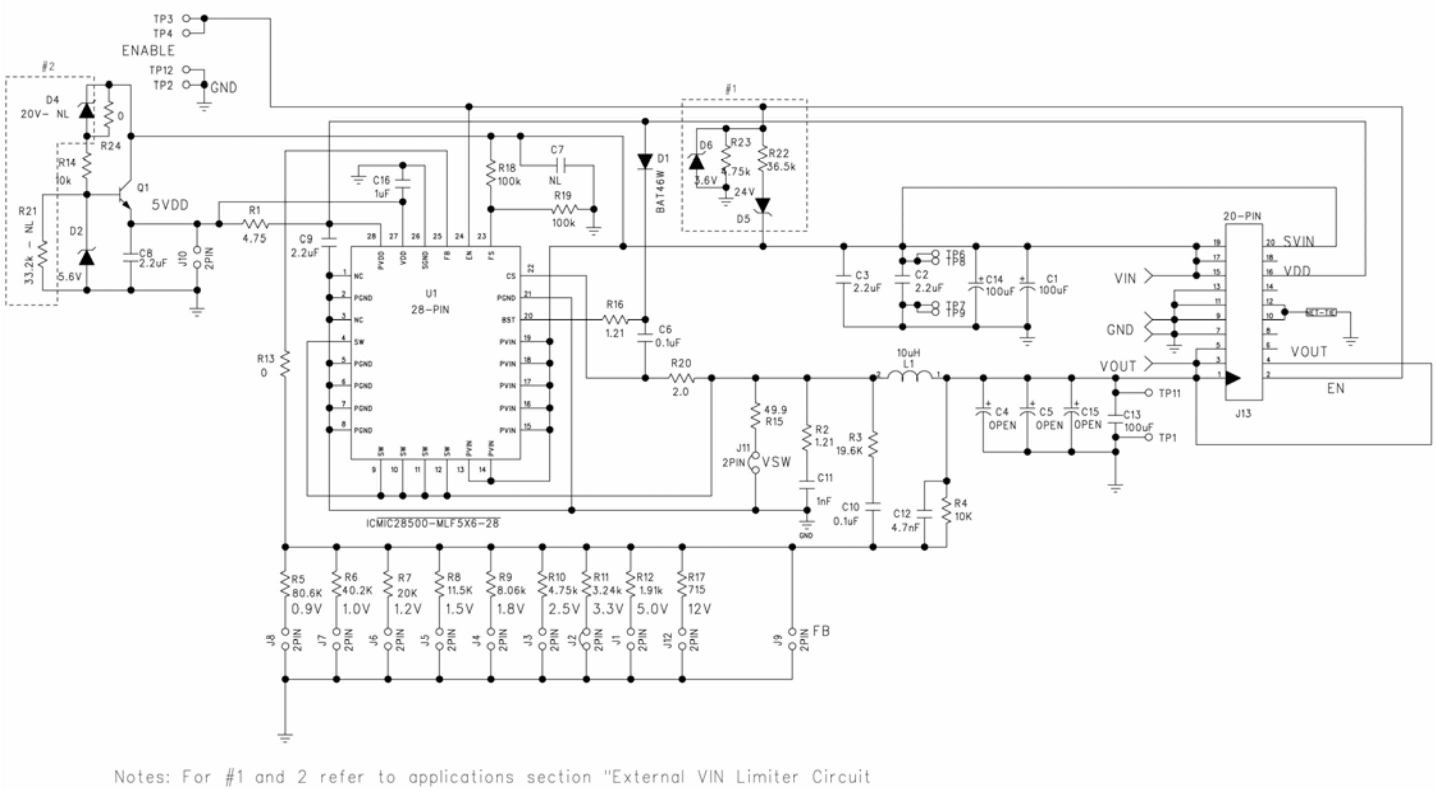


Figure 10. Schematic of MIC28500 Evaluation Board

(J9, J10, J11, R13, R15 are for testing purposes)

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1	EEU-FC2A101B	Panasonic (1)	100µF Aluminum Capacitor, SMD, 100V	1
C2, C3	GRM32ER72A225KA35L	Murata (2)	2.2µF Ceramic Capacitor, X7R, Size 1210, 100V	2
	C3225X7R2A225KT5	TDK(3)		
C13	GRM32ER60J107ME20L	Murata	100µF Ceramic Capacitor, X5R, Size 1210, 6.3V	1
	12106D107MAT2A	AVX(4)		
C6	06035C104KAT2A	AVX	0.1µF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H104KA93D	Murata		
	C1608X7R1H104K	TDK		
C10	GRM188R72A104KA35D	Murata	0.1µF Ceramic Capacitor, X7R, Size 0603, 100V	1
	C1608X7S2A104K	TDK		
C8, C9	0805ZC225MAT2A	AVX	2.2µF Ceramic Capacitor, X7R, Size 0805, 10V	2
	GRM21BR71A225KA01L	Murata		
	C2012X7R1A225K	TDK		
C11	GRM188R72A102KA01D	Murata	1nF Ceramic Capacitor, X7R, Size 0603, 100V	1
	C1608X7R2A102K	TDK		
	06031C102KAT2A	AVX		
C12	GRM188R71H472KA01D	Murata	4.7nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	C1608X7R2A472K	TDK		
	06035C472KAT2A	AVX		
C16	GRM21BR71A105KA01L	Murata	1µF Ceramic Capacitor, X7R, Size 0805, 10V	1
	C2012X7R1A105K	TDK		
C4, C5	Open			
C7	Open			
C14, C15	Open			
D1	BAT46W-TP	MCC(5)	Small Signal Schottky Diode	1
	BAT46W-7-F	Diodes Inc. (6)		
D2	MMXZ5232B-TP	MCC	5.6V Zener Diode	1
	CMDZ5L6	Central Semi(7)		1
D5	CMDZ24L-MIC	Central Semi	24V Zener	1
D6	CMDZ3L6-MIC	Central Semi	3.6V Zener	1
D4	Open			
L1	DR125-100-R	Cooper Bussmann(8)	10µH Inductor, 5.35A RMS, 7A Saturation Current	1
Q1	FCX493	Diodes Inc/ZETEX	100V NPN Transistor	1
R1	CRCW06034R75FKEA	Vishay Dale	4.75Ω Resistor, Size 0603, 1%	1
R2, R16	CRCW08051R21FKEA	Vishay Dale	1.21Ω Resistor, Size 0805, 1%	2
R3	CRCW060319K6FKEA	Vishay Dale	19.6kΩ Resistor, Size 0603, 1%	1
R4	CRCW060310K0FKEA	Vishay Dale	10kΩ Resistor, Size 0603, 1%	1
R5	CRCW060380K6FKEA	Vishay Dale	80.6kΩ Resistor, Size 0603, 1%	1
R6	CRCW060340K2FKEA	Vishay Dale	40.2kΩ Resistor, Size 0603, 1%	1

Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty.
R7	CRCW060320K0FKEA	Vishay Dale	20kΩ Resistor, Size 0603, 1%	1
R8	CRCW060311K5FKEA	Vishay Dale	11.5kΩ Resistor, Size 0603, 1%	1
R9	CRCW06038K06FKEA	Vishay Dale	8.06kΩ Resistor, Size 0603, 1%	1
R10, R23	CRCW06034K75FKEA	Vishay Dale	4.75kΩ Resistor, Size 0603, 1%	1
R11	CRCW06033K24FKEA	Vishay Dale	3.24kΩ Resistor, Size 0603, 1%	1
R12	CRCW06031K91FKEA	Vishay Dale	1.91kΩ Resistor, Size 0603, 1%	1
R13, R24	CRCW06030000Z0EAHP	Vishay Dale	0Ω Resistor, Size 0603	2
R14	CRCW080510K0JNEA	Vishay Dale	10kΩ Resistor, Size 0805, 1%	1
R15	CRCW060349R9FKEA	Vishay Dale	49.9Ω Resistor, Size 0603, 1%	1
R17 (OPEN)	CRCW0603715RFKEA	Vishay Dale	715Ω Resistor, Size 0603, 1%	
R18, R19	CRCW0603100KFKEAHP	Vishay Dale	100kΩ Resistor, Size 0603, 1%	2
R20	CRCW06032R00FKEA	Vishay Dale	2Ω Resistor, Size 0603, 1%	1
R21 (OPEN)	CRCW060333K2FKEA	Vishay Dale	33.2kΩ Resistor, Size 0603, 1%	1
R22	CRCW060336K5FKEA	Vishay Dale	36.5kΩ Resistor, Size 0603, 1%	1
U1	**MIC28500YJL**	**Micrel. Inc.[9]**	**75V/4A Synchronous Buck DC-DC Regulator**	**1**

Notes:

1. Panasonic: www.panasonic.com.
2. Murata: www.murata.com.
3. TDK: www.tdk.com.
4. AVX: www.avx.com.
5. MCC: www.mccsemi.com.
6. Diode Inc.: www.diodes.com.
7. Central Semi: www.centralsemi.com.
8. Cooper: www.cooperbussman.com.
9. **Micrel, Inc.: www.micrel.com.**

PCB Layout

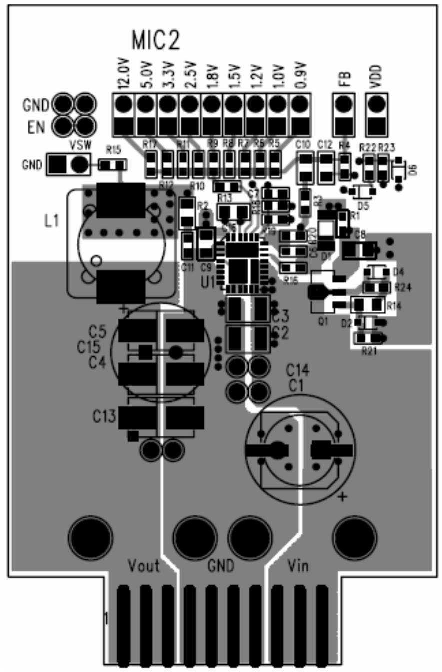


Figure 11. MIC28500 Evaluation Board Top Layer

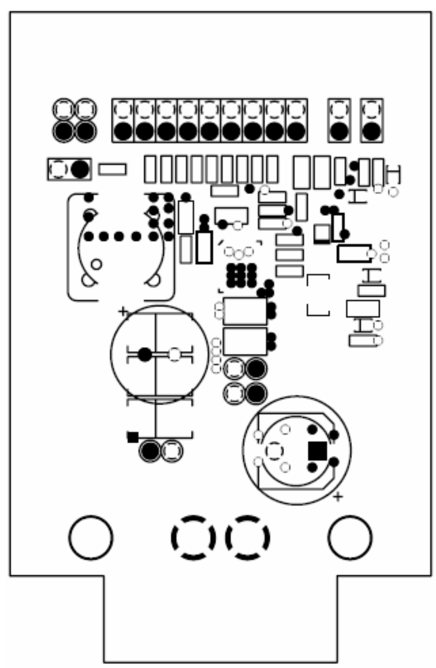


Figure 12. MIC28500 Evaluation Board Mid-Layer 1 (Ground Plane)

PCB Layout (Continued)

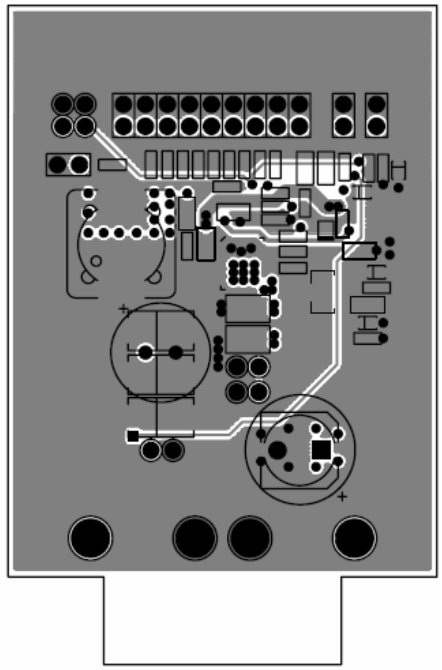


Figure 13. MIC28500 Evaluation Board Mid-Layer 2

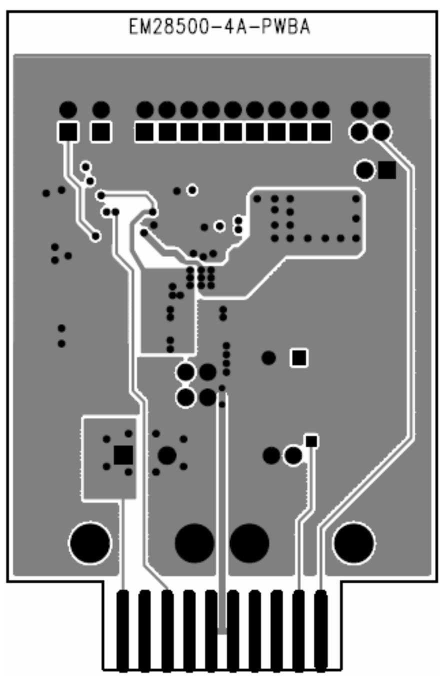
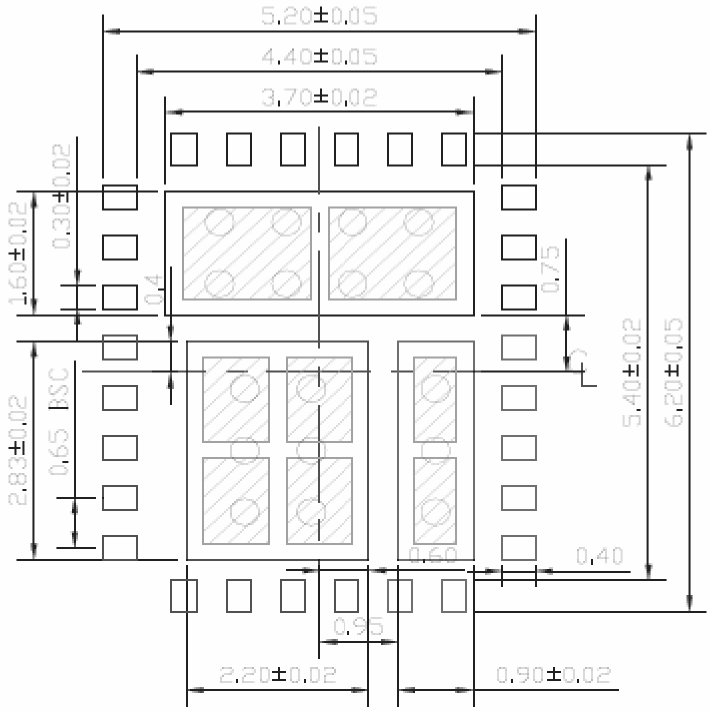


Figure 14. MIC28500 Evaluation Board Bottom Layer

Recommended Land Pattern

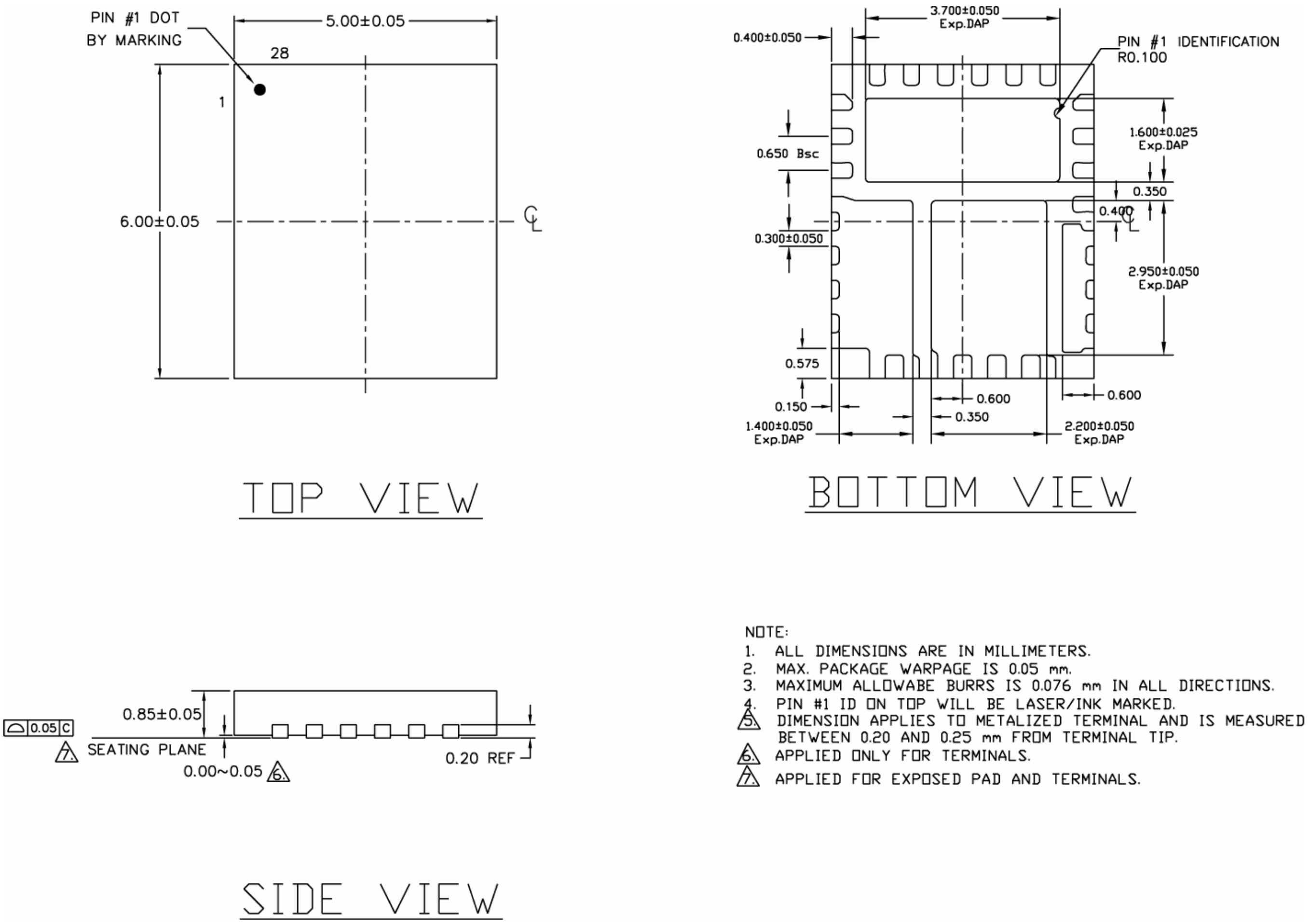
LP # MLF56Q-28LD-LP-1
All units are in mm
Tolerance ± 0.05 if not noted



Red circle indicates Thermal Via. Size should be .300-.350 mm in diameter, 0.80 mm pitch, and it should be connected to GND plane for maximum thermal performance.
Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Sizes should be a) 1.55x1.20 mm, 1.75 mm pitch, b) 0.80x1.11 mm, 1.31 mm pitch, c) 0.50x1.11 mm, 1.31 mm pitch.

Blue colored pads & Magenta colored pads indicates different potential. **DO NOT connect to GND plane.**

Package Information



28-Lead 5mm x 6mm MLF® (YJL)

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