



MX555ABB500M000

Ultra-Low Jitter 500MHz LVDS XO

ClockWorks® FUSION

General Description

The MX555ABB500M000 is an ultra-low phase jitter XO with LVDS output optimized for high line rate applications.

Features

- 500MHz LVDS
- Typical phase noise:
 - 101fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

Absolute Maximum Ratings

Supply Voltage (VIN).....	+4.6V
Lead Temperature (soldering, 10s).....	260°C
Storage Temperature (T _s).....	125°C
ESD Rating (HBM).....	2kV

Operating Ratings

Supply Voltage (VIN).....	+2.375V to +3.63V
Ambient Temperature (TA).....	-40°C to +85°C

Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 100 Ohms between Q and /Q.¹

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				90	mA
F0	Center Frequency			500		MHz
	Frequency Stability	Note 2			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		140 101		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		100		400	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage VOH max = VCM max + 1/2 VOD max	LVDS output levels	1.248	1.375	1.602	V
VOL	Output Low Voltage VOL min = VCM min - 1/2 VOD max	LVDS output levels	0.898	1.025	1.252	V
VOD	Output Differential Voltage		247	350	454	mV
VCM	Common Mode Output Voltage		1.125	1.2	1.375	V

Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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May 30, 2017
MX555AB1-4555

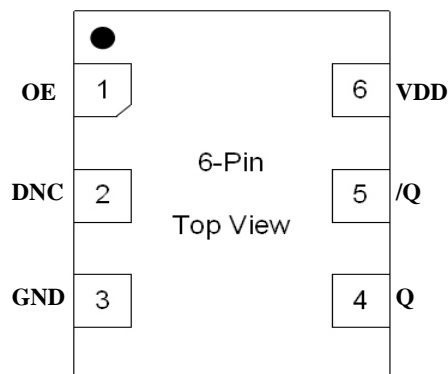
Revision 1.0
tcghelp@microchip.com

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX555ABB500M000	MX555A	BB5000	Tube	6-Pin 5mm x 3.2mm LGA
MX555ABB500M000-TR	MX555A	BB5000	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVDS	Clock Output Frequency = 500MHz
6	VDD	PWR		Power Supply

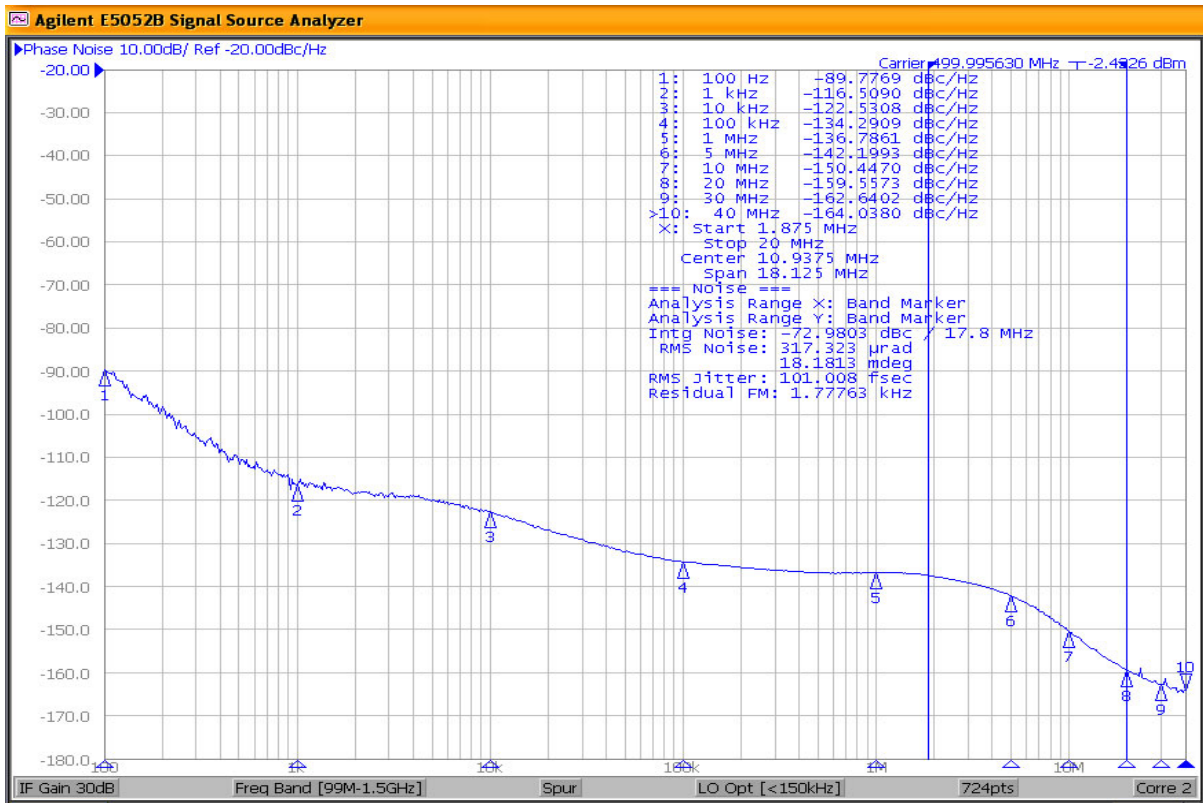


Figure 1. LVDS Output 500MHz 1.875MHz-20MHz 101fs

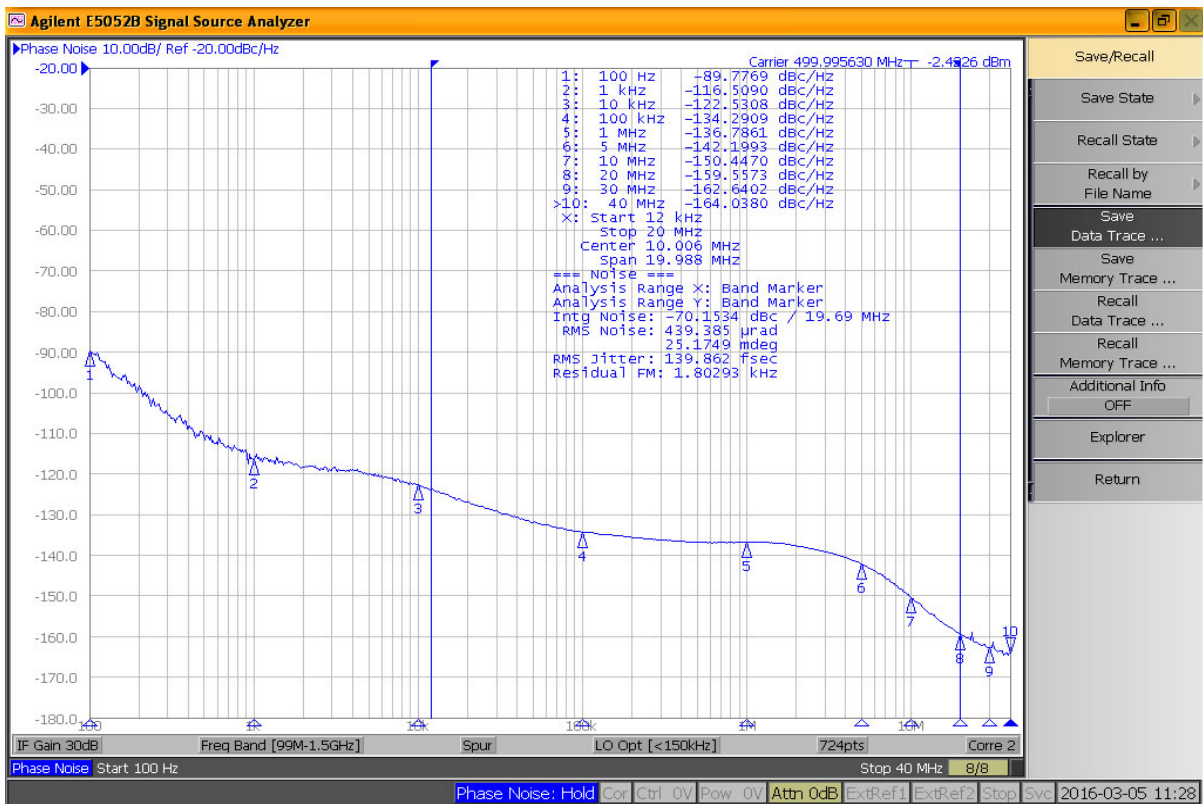


Figure 2. LVDS Output 500MHz 12kHz-20MHz 140fs

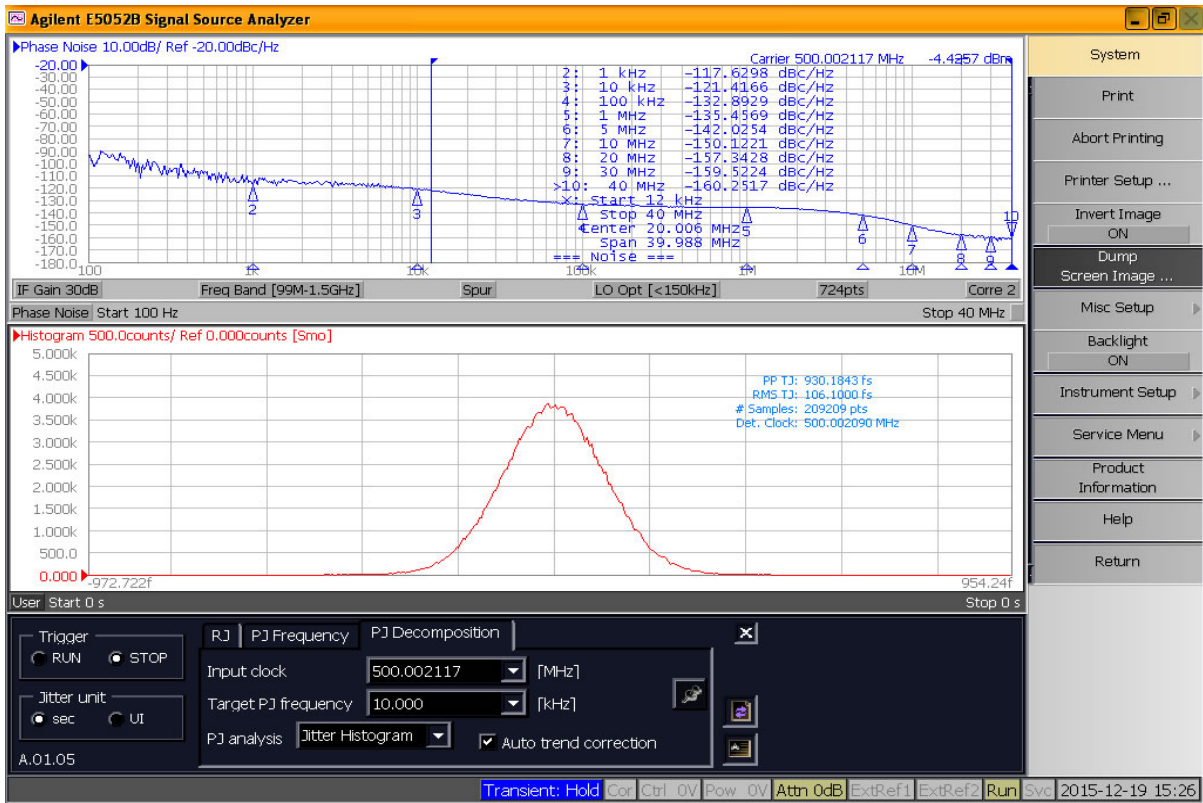
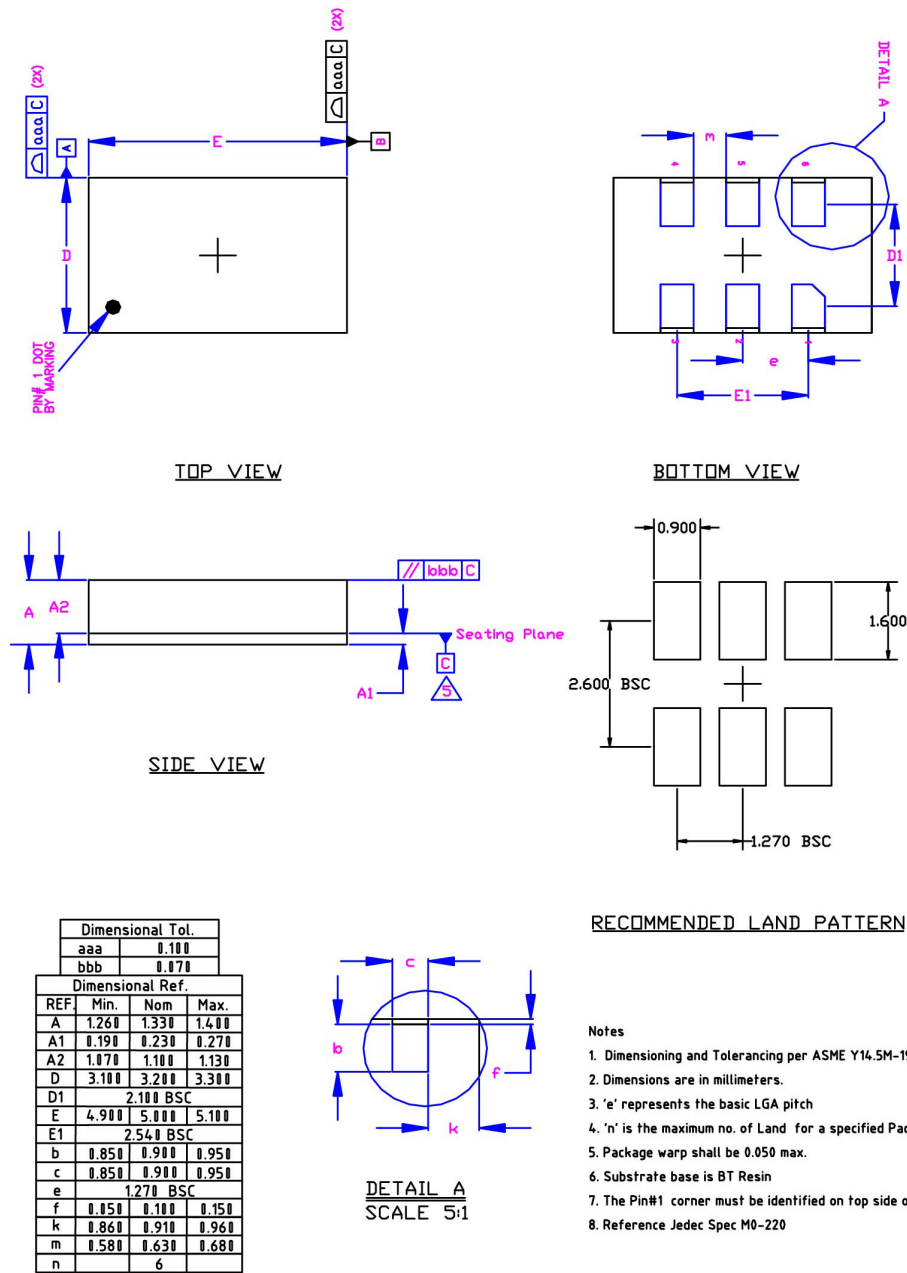


Figure 3. E5001A Period Jitter @ 500MHz LVDS, RMS TJ: 106fs, Pk-Pk TJ: 930fs

Package Information and Recommended Land Pattern for 6-Pin LGA³



RECOMMENDED LAND PATTERN

- Notes**
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
 2. Dimensions are in millimeters.
 3. 'e' represents the basic LGA pitch
 4. 'n' is the maximum no. of Land for a specified Package.
 5. Package warp shall be 0.050 max.
 6. Substrate base is BT Resin
 7. The Pin#1 corner must be identified on top side only.
 8. Reference Jecdec Spec M0-220

Note:

3. Package information is correct as of the publication date. For updates and most current information, go to www.microchip.com.

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