

CRYSTAL-LESS PCI-EXPRESS GEN 1 & GEN 2 DUAL OUTPUT CLOCK GENERATOR

Features

- Crystal-less clock generator with integrated CMEMS
- PCI-Express Gen 1/2 compliant
- Two PCIe 100 MHz differential HCSL outputs
- One 25 MHz single-ended LVCMOS output
- Supports Serial (ATA) at 100 MHz
- Low power differential output buffers
- No termination resistors required for differential output clocks
- Triangular spread spectrum profile for maximum EMI reduction (Si50122-A4)
- Industrial Temperature -40 to 85 °C
- 2.5 V, 3.3 V Power supply
- Small package 10-pin TDFN (2.0x2.5 mm)
- Si50122-A3 does not support spread spectrum outputs
- Si50122-A4 supports 0.5% down spread outputs

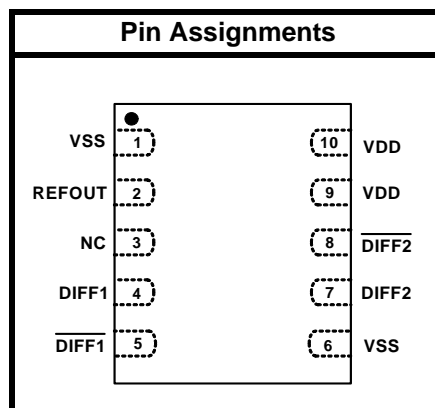
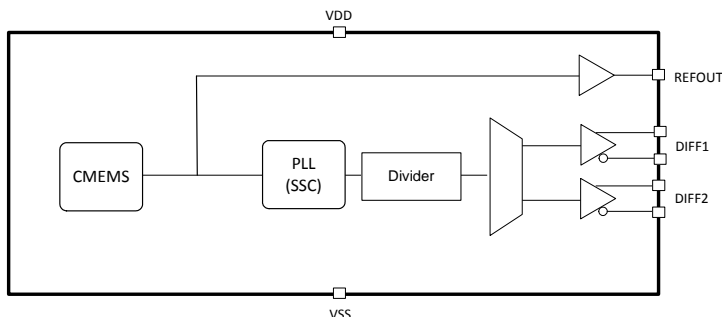
Applications

- Digital TV
- Set top box
- Solid State Drives (SSD)
- Wireless Access Point
- Home Gateway
- Network Attached Storage
- Multi-function Printer
- Wireless Access Point
- Digital Video Cameras

Description

Si50122-A3/A4 is a high performance, crystal-less PCIe clock generator that can generate two 100 MHz PCIe clock and one 25 MHz LVCMOS clock outputs. The differential clock outputs are compliant to PCIe Gen1 and Gen 2 specifications. The ultra-small footprint (2.0x2.5 mm) and industry leading low power consumption make Si50122-A3/A4 the ideal clock solution for consumer and embedded applications where board space is limited and low power is needed.

Functional Block Diagram



Patents pending

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
1. Electrical Specifications	4
2. Test and Measurement Setup	7
3. Pin Descriptions	9
4. Ordering Guide	10
5. Package Outlines	11
6. Recommended Design Guideline	13
Contact Information	14

Si50122-A3/A4

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage (3.3 V Supply)	V_{DD}	$3.3\text{ V} \pm 10\%$	2.97	3.3	3.63	V
Supply Voltage (2.5 V Supply)	V_{DD}	$2.5\text{ V} \pm 10\%$	2.25	2.5	2.75	V

Table 2. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage $_{V_{DD}=3.3\text{ V}}$	V_{DD}	$3.3\text{ V} \pm 10\%$	2.97	3.30	3.63	V
Operating Voltage $_{V_{DD}=2.5\text{ V}}$	V_{DD}	$2.5\text{ V} \pm 10\%$	2.25	2.5	2.75	V
Operating Supply Current	I_{DD}	Full active; $3.3\text{ V} \pm 10\%$	—	20	23	mA
		Full active; $2.5\text{ V} \pm 10\%$	—	18	21	mA
Input Pin Capacitance	C_{IN}	Input Pin Capacitance	—	3	5	pF
Output Pin Capacitance	C_{OUT}	Output Pin Capacitance	—	—	5	pF

Table 3. AC Electrical Specifications

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DIFF Clocks						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Skew	T_{SKEW}	Measured at 0 V differential	—	—	100	ps
Output Frequency	F_{OUT}	VDD = 3.3 V	—	100	—	MHz
Frequency Accuracy	F_{ACC}	All output clocks	—	—	100	ppm
Slew Rate	$t_{r/f2}$	Measured differentially from ± 150 mV	0.6	—	5.0	V/ns
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV
Voltage High	V_{HIGH}		—	—	1.15	V
Voltage Low	V_{LOW}		-0.3	—	—	V
Spread Range	S_{RNG}	Down Spread, -A4 only	—	—	-0.5	%
Modulation Frequency	F_{MOD}	-A4 only	30	31.5	33	kHz
DIFF Clocks Jitter Parameters, VDD = 3.3 V \pm 10%						
PCIe Gen1 Pk-Pk	$Pk-Pk_{GEN1}$	PCIe Gen 1	—	20.7	35	ps
PCIe Gen2 Phase Jitter	RMS_{GEN2}	10 kHz < F < 1.5 MHz	—	0.8	2.1	ps
		1.5 MHz < F < Nyquist	—	1.4	2.2	ps
DIFF Clocks Jitter Parameters, VDD = 2.5V \pm 10%						
PCIe Gen1 Pk-Pk	$Pk-Pk_{GEN1}$	PCIe Gen 1	—	25	40	ps
PCIe Gen2 Phase Jitter	RMS_{GEN2}	10 kHz < F < 1.5 MHz	—	0.9	2.9	ps
		1.5 MHz < F < Nyquist	—	1.7	3.0	ps
25 MHz at 3.3 V						
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	—	55	%
Output Rise Time	t_r	$C_L = 10$ pF, 20% to 80%		1.2	3.0	ns
Output Fall Time	t_f	$C_L = 10$ pF, 20% to 80%		1.2	3.0	ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	—	250	ps
Long Term Accuracy	L_{ACC}	Measured at 1.5 V	—	—	100	ppm
Powerup Time						
Clock Stabilization from Powerup	T_{STABLE}	First powerup to first output	—	—	10	ms
Note: Visit www.pcisig.com for complete PCIe specifications.						

Si50122-A3/A4

Table 4. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature, Storage	T_S	Non-functional	-65		150	°C
Temperature, Operating Ambient	T_A	Functional	-40		85	°C
Temperature, Junction	T_J	Functional	—		150	°C
Dissipation, Junction to Case	θ_{JC}	JEDEC (JESD 51)	—		38.3	°C/W
Dissipation, Junction to Ambient	θ_{JA}	JEDEC (JESD 51)	—		90.4	°C/W

Table 5. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD_3.3V}$		—		4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	-0.5		4.6	V_{DC}
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000		—	V
Flammability Rating	UL-94	UL (Class)	V-0			

Note: While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during powerup. Power supply sequencing is NOT required.

2. Test and Measurement Setup

Figures 1–3 show the test load configuration for the differential clock signals.

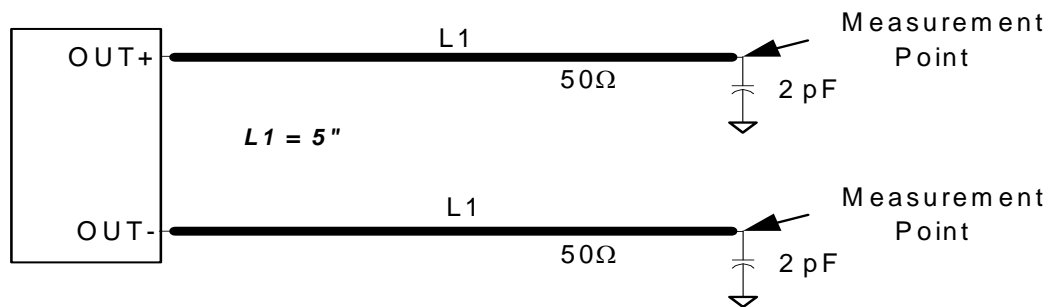
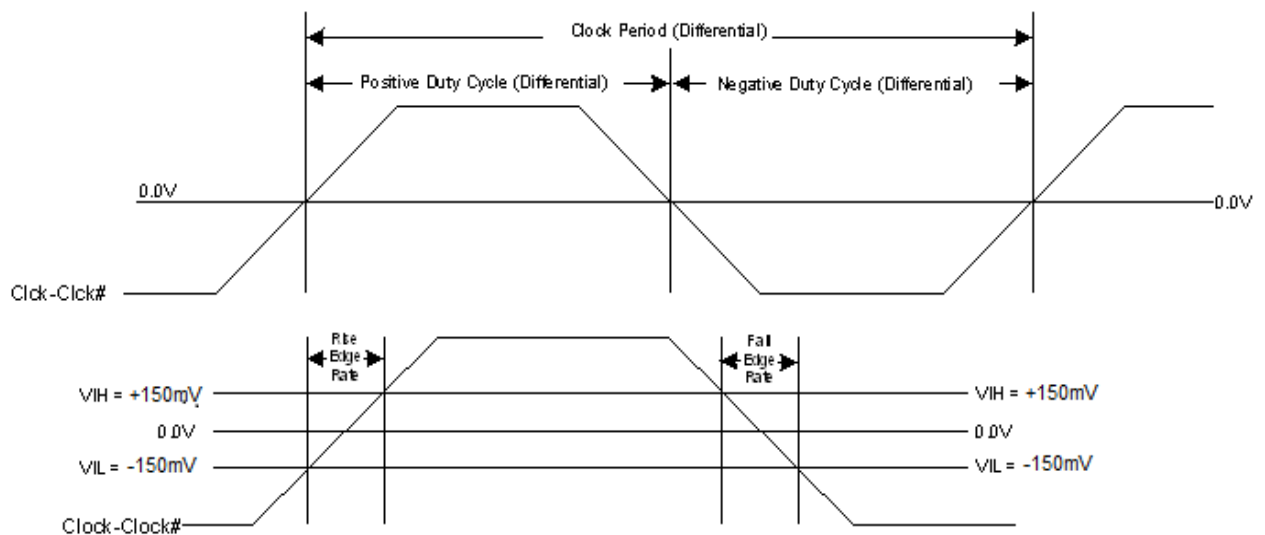


Figure 1. 0.7 V Differential Load Configuration



**Figure 2. Differential Measurement for Differential Output Signals
(for AC Parameters Measurement)**

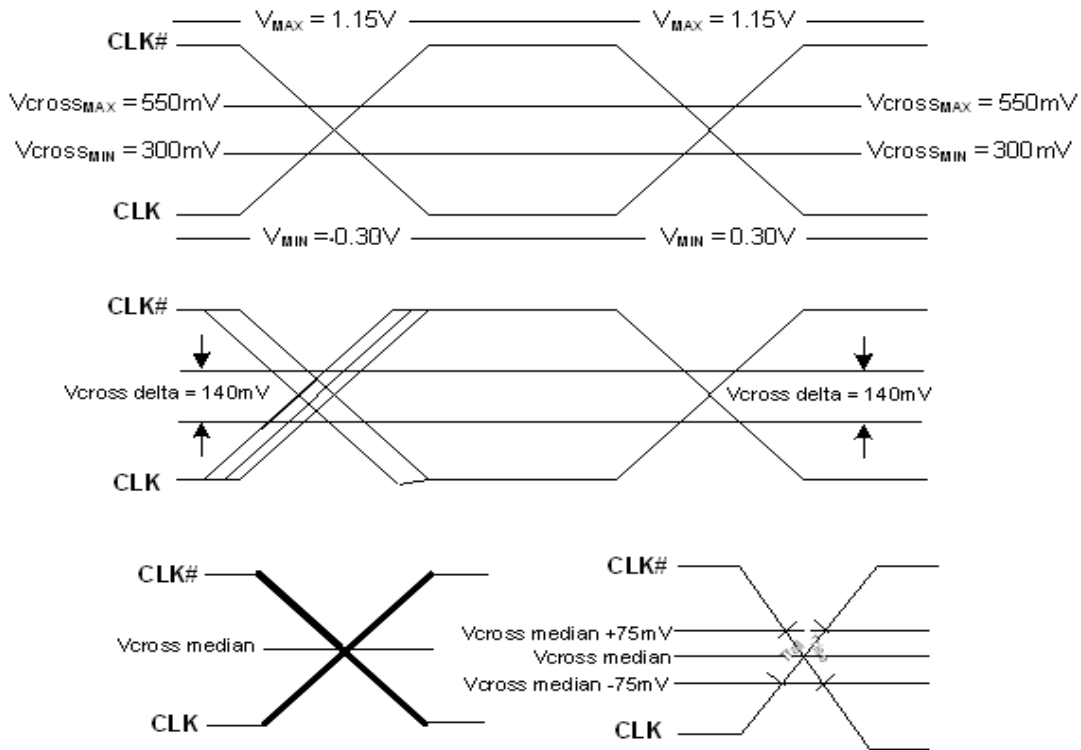


Figure 3. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

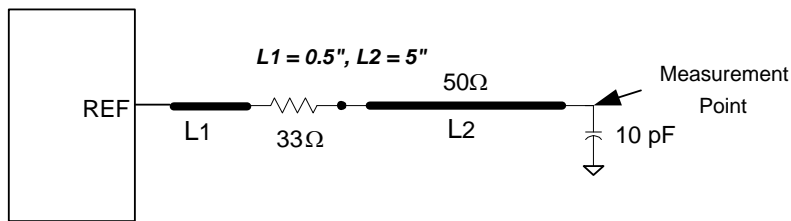


Figure 4. Single-ended Clocks with Single Load Configuration

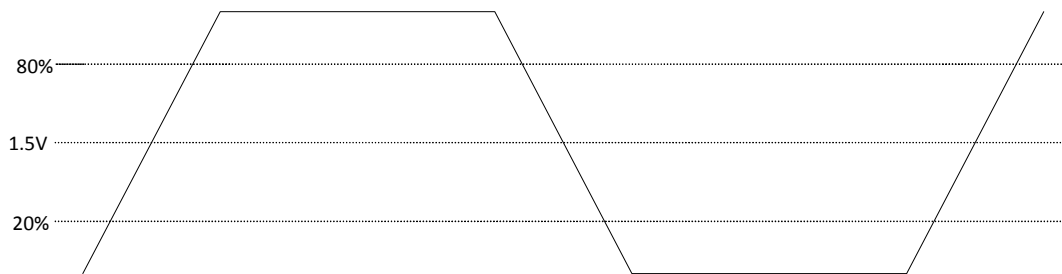


Figure 5. Single-ended Output Signal (for AC Parameter Measurement)

3. Pin Descriptions

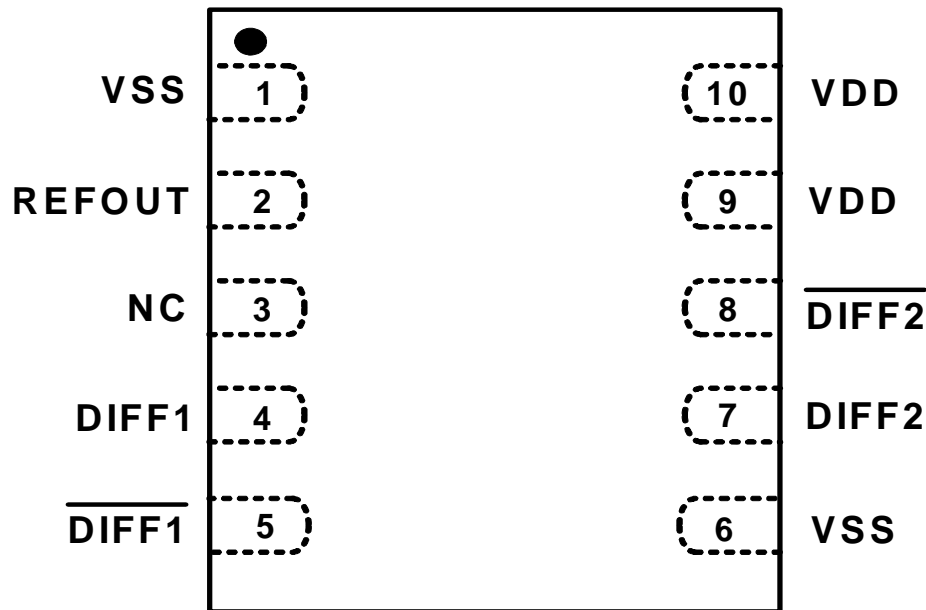


Figure 6. 10-Pin TDFN

Table 6. Si50122-Ax-GM 10-Pin TDFN Descriptions

Pin #	Name	Type	Description
1	VSS	GND	Connect to Ground
2	REFOUT	O, SE	25 MHz LVCMOS clock output
3	NC	NC	No Connect. Do not connect this pin to anything.
4	DIFF1	O, DIF	0.7 V, 100 MHz differential clock output
5	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock output
6	VSS	GND	Connect to Ground
7	DIFF2	O, DIF	0.7 V, 100 MHz differential clock output
8	$\overline{\text{DIFF2}}$	O, DIF	0.7 V, 100 MHz differential clock output
9	VDD	PWR	Power supply
10	VDD	PWR	Power supply

Si50122-A3/A4

4. Ordering Guide

Part Number	Spread Option	Package Type	Temperature
Si50122-A3-GM	No Spread	10-pin TDFN	Industrial, -40 to 85 °C
Si50122-A3-GMR	No Spread	10-pin TDFN—Tape and Reel	Industrial, -40 to 85 °C
Si50122-A4-GM	-0.5% Spread	10-pin TDFN	Industrial, -40 to 85 °C
Si50122-A4-GMR	-0.5% Spread	10-pin TDFN—Tape and Reel	Industrial, -40 to 85 °C

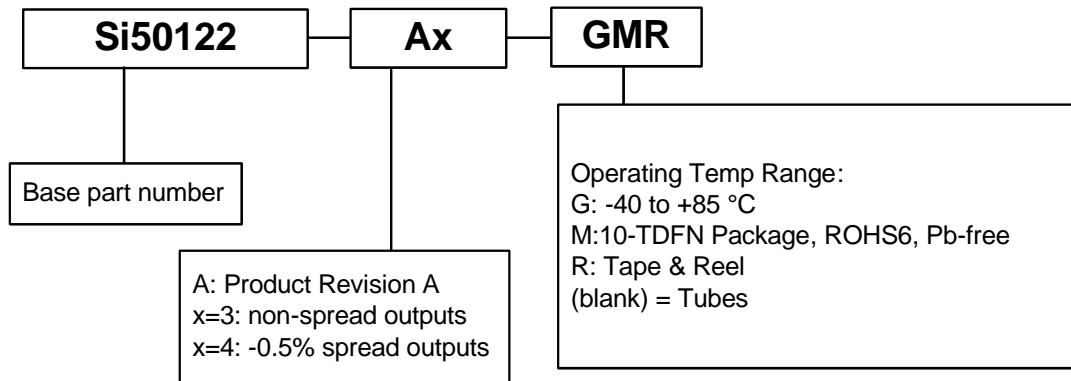


Figure 7. Ordering Information

5. Package Outlines

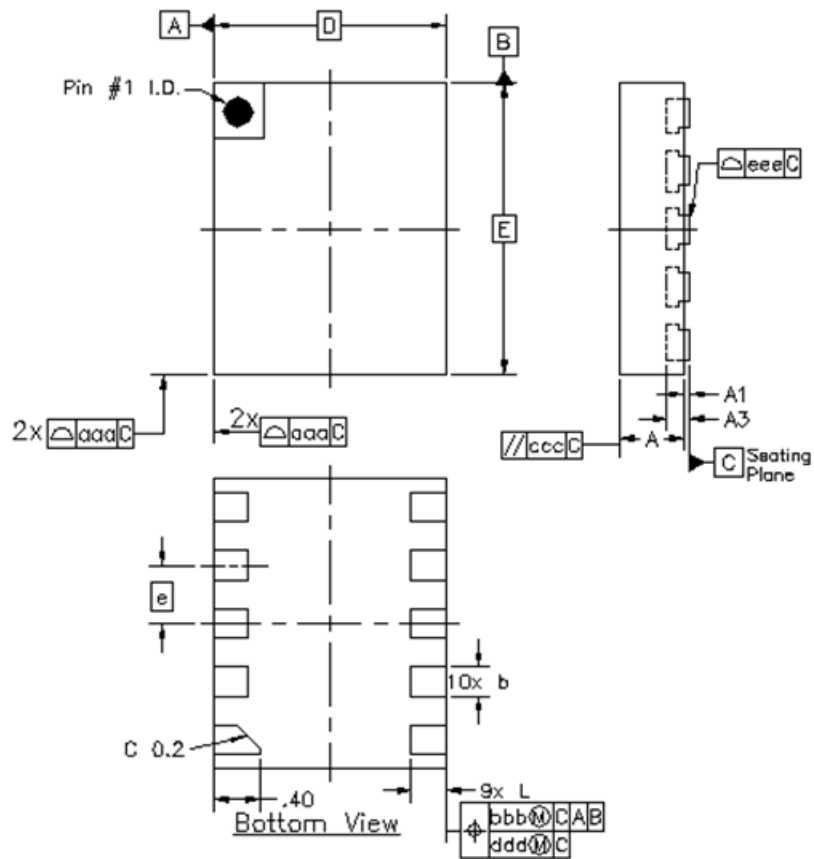
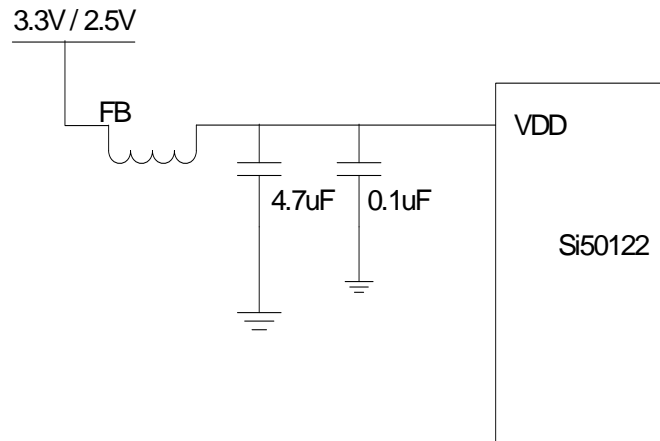


Figure 8. 10-Pin TDFN Package Drawing

Table 7. Package Diagram Dimensions

Symbol	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	—	0.05
A3	0.203 REF		
b	0.20	0.25	0.30
D	2.00 BSC		
e	0.50 BSC		
E	2.50 BSC		
L	0.35	0.4	0.45
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
Notes: <ol style="list-style-type: none">1. All dimensions shown are in millimeters (mm) unless otherwise noted.2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			

6. Recommended Design Guideline



Note: FB Specifications:
DC resistance 0.1–0.3 Ω
Impedance at 100 MHz $\geq 1000 \Omega$

Figure 9. Recommended Application Schematic



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro



Timing Portfolio
www.silabs.com/timing



SW/HW
www.silabs.com/CBPro



Quality
www.silabs.com/quality



Support and Community
community.silabs.com

Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>