AVAGO TECHNOLOGIES | EXPRESS SWITCHING BY PLX

Product Snapshot

PCI Express® Switches, Bridges and ExpressFabric® Platform

Worldwide Leader in PCIe® Switching Technology

Avago ExpressFabric® Technology, the High-Speed Backbone for Data Center Connectivity

To meet the needs of data-intensive applications and hyperscale computing, modern data centers require solutions that offer maximum performance with minimal power consumption. While compute and storage devices have native PCIe for internal communication, they all use a different technologies, such as Ethernet or InfiniBand, to connect externally. Now Avago, the leader in PCI Express switching with over 100 million ports shipped, is driving an evolution of the data center with the PEX9700 series of switches. These new switches, based on PCIe Gen3, can dramatically increase performance and availability by allowing each device in a rack to communicate over PCIe, eliminating the inherent latency and power usage caused by components required to convert host PCIe data for other protocols. The result is a rack of devices that have converged into a single high-performance, scalable and high-availability compute solution.

PEX9700 Series featuring ExpressFabric Technology

ExpressFabric PCIe Gen3 Device Family / PCI-SIG® Base Spec. r3.0

Part Number	Lanes	Ports	Latency (ns)	HPC*	TWC* Ports	SSC*	Dedicated x1 mCPU Port	DMA Multicast	Shared I/O	Ethernet DMA (NIC DMA*)	DPC/eDPC*	Read Tracking	SRIS*	MSI-X*	Power Typ. (W)	Pkg. (mm²)
PEX9797	97	25	150	6	24	24	✓	✓	✓	✓	✓	✓	✓	✓	23.9	35x35
PEX9781	81	21	150	5	20	20	✓	✓	✓	✓	✓	✓	✓	✓	21.5	35x35
PEX9765	65	17	150	4	16	16	✓	✓	✓	✓	✓	✓	✓	✓	15.9	35x35
PEX9749	49	13	150	4	12	12	✓	✓	✓	✓	✓	✓	✓	✓	13.5	27x27
PEX9733	33	9	150	2	8	8	✓	✓	✓	✓	✓	✓	✓	✓	7.9	27x27
PEX9716	16	5	154	1	4	4	—	✓	✓	✓	✓	✓	✓	✓	4.0	19x19
PEX9712	12	5	158	1	4	4	—	✓	✓	✓	✓	✓	✓	✓	3.5	19x19

* **Acronym Guide**: DMA = Direct Memory Access; HPC = Hot-Plug Controllers; TWC = Tunneled Window Connection (Multi-Host Communication); SSC = Spread Spectrum Clock Isolation; MSI-X = Message Signaled Interrupts; SRIS = Separate Refclk Independent SSC Architecture; DPC = Downstream Port Containment; eDPC = Enhanced DPC; Temperature range = 0 +70 (C°)

PCIe to USB Controllers

SuperSpeed USB 3.0 Controllers / PCI-SIG® Base Spec. r3.0

Part Number	CPU Interface	USB Interface	Performance	Active Power	Suspended Power	I/O Voltage	Package Size (mm²)
USB3380	One Port (Endpoint or Root Complex) PCIe x1 Gen2 (5GT/s)	SuperSpeed USB 3.0 Peripheral	420 Mbytes/s	800mW	4.6mW	3.3V	10x10 88-pin, QFN
USB3382	Two Ports (Multi-Configuration) PCIe x1 Gen2 (5GT/s)	SuperSpeed USB 3.0 Peripheral	420 Mbytes/s	820mW	6.1mW	3.3V	10x10 136-pin, aQFN

ExpressLane™ Switches (PCIe Gen3)

Part Number	Lanes	Ports	Latency (ns)	Multi-Root/ Multi-Host	Multicast or Dual-cast	Read Pacing	ACS/ ARI*	NT*	DMA*	HPC*	VCs*	SSC*	Power Typ. (W)	Temp. (C°)	Package (mm²)
PEX8796	96	24	150	4	MC	No	Yes	2	—	6	1	24	18.6	-40 +85	35x35
PEX8780	80	20	150	4	MC	No	Yes	2	—	5	1	20	16.6	-40 +85	35x35
PEX8764	64	16	150	4	MC	No	Yes	2	—	4	1	16	12.4	-40 +85	35x35
PEX8750	48	12	150	3	MC	No	Yes	2	—	4	1	12	10.3	-40 +85	27x27
PEX8749	48	18	126	6	MC	Yes	Yes	2	4	3	2	12	7.3	0 +70	27x27
PEX8748	48	12	126	6	MC	Yes	Yes	1	—	3	1	—	7.3	0 +70	27x27
PEX8747	48	5	126	—	MC	Yes	Yes	—	—	—	1	—	7.3	0 +70	19x21
PEX8734	32	8	150	2	MC	No	Yes	2	—	2	1	8	6.2	-40 +85	27x27
PEX8733	32	18	132	4	MC	Yes	Yes	2	4	3	2	8	6.4	0 +70	27x27
PEX8732	32	8	132	4	MC	Yes	Yes	1	—	3	1	—	5.8	0 +70	27x27
PEX8725	24	10	132	4	MC	Yes	Yes	2	4	3	2	6	5.4	0 +70	19x19
PEX8724	24	6	132	4	MC	Yes	Yes	1	—	3	1	—	5.4	0 +70	19x19
PEX8718	16	5	154	1	MC	No	Yes	1	—	1	1	4	2.9	-40 +85	19x19
PEX8717	16	10	138	2	MC	Yes	Yes	2	4	3	2	4	4.9	0 +70	19x19
PEX8716	16	4	138	2	MC	Yes	Yes	1	—	3	1	—	4.3	0 +70	19x19
PEX8714	12	5	158	1	MC	No	Yes	1	—	1	1	4	2.7	-40 +85	19x19
PEX8713	12	10	138	2	MC	Yes	Yes	2	4	3	2	3	4.7	0 +70	19x19
PEX8712	12	3	138	2	MC	Yes	Yes	1	—	3	1	—	4.1	0 +70	19x19

* **Acronym Guide:** ACS = Access Control Service; ARI = Alternative Routing-ID Interpretation; NT = Non-Transparency; DMA = Direct Memory Access channels; HPC = Hot-Plug Controllers; ^^ = Hot-Plug control via I^2C; VCs = Virtual Channels; SSC = Spread Spectrum Clock Isolation. PCIe Gen3 devices are recommended for all new designs.

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Product Snapshot

PCI Express® Switches, Bridges and ExpressFabric® Platform

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ExpressLane™ Switches (PCIe Gen2)

Part Number	Lanes	Ports	Latency (ns)	Multi-Root/ Multi-Host	Multicast or Dual-cast	Read Pacing	ACS/ ARI*	NT*	DMA*	HPC*	VCs*	SSC*	Power Typ. (W)	Temp. (C°)	Package (mm²)
PEX8696	96	24	176	8	MC	Yes	Yes	1	—	4	1	—	10.2	–5 +85	35x35
PEX8680	80	20	176	6	MC	Yes	Yes	1	—	4	1	—	9.0	–5 +85	35x35
PEX8664	64	16	176	5	MC	Yes	Yes	1	—	4	1	—	7.9	–5 +85	35x35
PEX8649	48	12	176	4	MC	Yes	Yes	1	—	3	1	—	6.7	–5 +85	27x27
PEX8648	48	12	140	—	DC	Yes	Yes	1	—	3	1	—	3.5	–40 +85	27x27
PEX8647	48	3	140	—	DC	Yes	Yes	—	—	—	1	—	3.5	–5 +85	27x27
PEX8636	36	24	200	8	MC	Yes	Yes	1	—	4	1	—	8.1	–5 +85	35x35
PEX8632	32	12	145	—	DC	Yes	Yes	1	—	3	1	—	2.9	–40 +85	27x27
PEX8625	24	24	200	8	MC	Yes	Yes	1	—	4	1	—	7.7	–5 +85	35x35
PEX8624	24	6	145	—	DC	Yes	Yes	1	—	3	1	—	2.6	–40 +85	19x19
PEX8619	16	16	140	—	DC	Yes	Yes	1	4	^^	2	1	2.0	–40 +85	19x19
PEX8618	16	16	140	—	DC	Yes	Yes	1	—	^^	2	1	1.9	–10 +85	19x19
PEX8617	16	4	140	—	DC	Yes	Yes	1	—	^^	2	1	1.9	–40 +85	19x19
PEX8616	16	4	150	—	DC	Yes	Yes	1	—	2	1	—	2.3	–5 +85	19x19
PEX8615	12	12	140	—	DC	Yes	Yes	1	4	^^	2	1	1.8	–40 +85	19x19
PEX8614	12	12	140	—	DC	Yes	Yes	1	—	^^	2	1	1.7	–10 +85	19x19
PEX8613	12	3	140	—	DC	Yes	Yes	1	—	^^	2	1	1.7	–40 +85	19x19
PEX8612	12	3	150	—	DC	Yes	Yes	1	—	2	1	—	2.2	–5 +85	19x19
PEX8609	8	8	140	—	DC	Yes	Yes	1	4	^^	2	1	1.6	–40 +85	15x15
PEX8608	8	8	140	—	DC	Yes	Yes	1	—	^^	2	1	1.4	–10 +85	15x15
PEX8606	6	6	190	—	DC	Yes	Yes	1	—	^^	2	1	1.3	–40 +85	15x15
PEX8605	4	4	250	—	—	—	Yes	—	—	—	1	—	0.8	–40 +85	10x10
PEX8604	4	4	190	—	DC	Yes	Yes	1	—	^^	2	1	1.3	–40 +85	15x15
PEX8603	3	3	250	—	—	—	Yes	—	—	—	1	—	0.7	–40 +85	10x10

*** Acronym Guide:** ACS = Access Control Service; ARI = Alternative Routing-ID Interpretation; NT = Non-Transparency; DMA = Direct Memory Access channels; HPC = Hot-Plug Controllers; ^^ = Hot-Plug control via I^2C; VCs = Virtual Channels; SSC = Spread Spectrum Clock Isolation. PCIe Gen3 devices are recommended for all new designs.

PCIe Bridges

ExpressLane PCIe to PCI and PCI-X Bridges / PCI-SIG® Base Spec. r1.0a

Part Number	Lanes	Bus Interface	Reverse Mode	Forward Mode	Power	PCI Masters	GPIO	Package Size (mm²)
PEX8112	1	PCIe to PCI	✓	✓	400mW	4	4	10x10
								13x13
PEX8114	4	PCIe to PCI-X	✓	✓	2W	4	—	17x17

ExpressLane PCIe to Local Bus Bridge / PCI-SIG® Base Spec. r1.0a

Part Number	Lanes	Description	DMA Channels	Integrated SerDes	Power	Root Complex Mode	Package Size (mm²)
PEX8311	1	8/16/32-bit, 66 MHz	2	Yes	1W	Yes	21x21

PCIe to USB Controllers

Hi-Speed USB 2.0 Controllers / PCI-SIG® Base Spec. r2.0

Part Number	CPU Interface	USB Interface	Performance	Active Power	Suspended Power	I/O Voltage	Package Size (mm²)
USB2380	One Port (Endpoint) PCIe x1 Gen1 (2.5Gbps)	Hi-Speed USB 2.0 Peripheral	41 Mbytes/s	600mW	2.3mW	3.3V	10x10 88-pin, QFN

For product information and a complete list of distributors, please visit our website:

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