EQCO850SC.3-HS and EQCO875SC.3-HS Single Coax Transceiver for LVDS and Gigabit Ethernet applications

1.1 Features

- Combined transmitter and receiver with an integrated equalizer to form a full-duplex bidirectional connection over a single 50Ω coax cable (EQCO850SC-HS) or 75Ω coax cable (EQCO875SC-HS)[1]
- Internal LVDS termination resistors for low external discrete count
- Allows power distribution over the coax, on top of the data signals
- Single 3.3 V supply
- 16-pin, 0.65 mm pin pitch, 4 mm QFN package
- Pb-free and RoHS compliant

1.2 Applications

This solution is useful and economical for many markets and applications, including the following:

- Camera networks - Home Security, Surveillance, industrial/inspection, medical cameras
- Coax Cable-Distribution infrastructure

1.3 Typical Equalization Performance

Bit Rate	EQCO850SC.3-HS range using		
	RG174 (∅ 2.8 mm)	RTK (∅ 2.8 mm)	RG58 (∅ 5 mm)
125Mbps	40 m	70 m	70 m
250Mbps	30 m	60 m	70 m
500Mpbs	25 m	40 m	50 m
1Gbps	15 m	25 m	30 m

Table 1: Typical Equalization Performance

For other cable types, the length that can be reached in full-duplex may have maximally -12dB insertion loss at 625 MHz, for a bit rate of 1.25 Gbps. Equalizer performance works up to much higher levels in half-duplex. For lower bit-rates slightly longer cable lengths can be achieved.

[1] EQCO850SC.3-HS works for 50Ω coax and the EQCO875SC.3-HS works for 75Ω coax. Everything is the same except the part number, the used coax and the characteristic impedance of transmission lines and connectors between the chip and the edge of the boards. See also section 5.1 about the typical application circuit.

2 Functional Description

2.1 Overview

The EQCO850SC-HS single coax transceiver is designed to simultaneously transmit and receive signals on a single 50 Ω coax cable. A sister product, the EQCO875SC-HS can achieve similar performance when used in 75 Ω coaxial systems.

The EQCO850SC-HS (EQCO875SC-HS) is ideally suited for simplex and duplex LVDS connections over 50 Ω (75 Ω) coax cable between 125 Mbps and 1.25 Gbps. For correct operation the signals must be NRZ (non-return-to-zero) encoded, DC balanced with a maximum run length of 10 bits. Excellent EMI/RFI shielding of coax cable allows for good EMI properties.

The EQCO850SC-HS operates with all kinds of 50 Ω coax cable, including the cost effective 2.8 mm diameter RTK cable (e.g. Leoni Dakar 302), which is the type of coax cable used for radio and navigation antennas in automotive. This cable fits well with the Standardized (DIN and USCAR), high-performance, cost-effective RF connectors - SAE/USCAR-18 “FAKRA/SMB RF Connector”.

The EQCO875SC-HS is typically useful in situations where legacy 75 Ω cables are present.

Fig. 1 illustrates a typical LVDS Coaxial connection. It can be used for Gigabit Ethernet connections over a single coax cable.

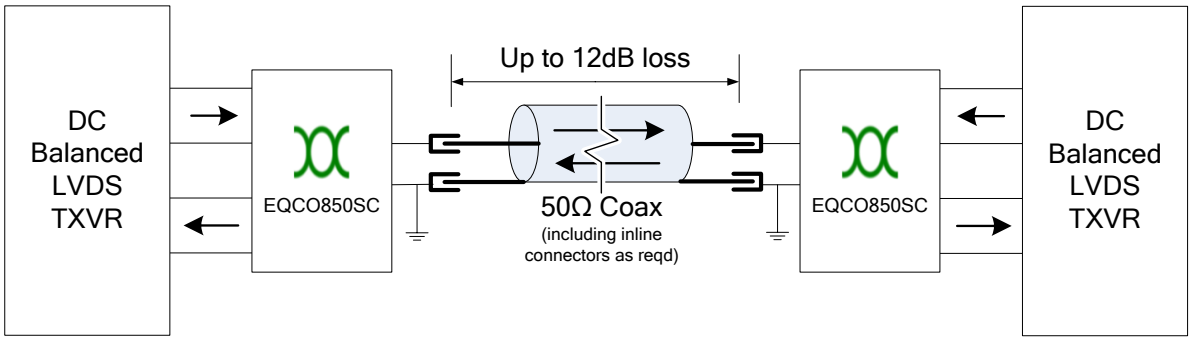

Figure 1: Typical LVDS Link using EQCO850SC-HS

2.2 Package and Pinout

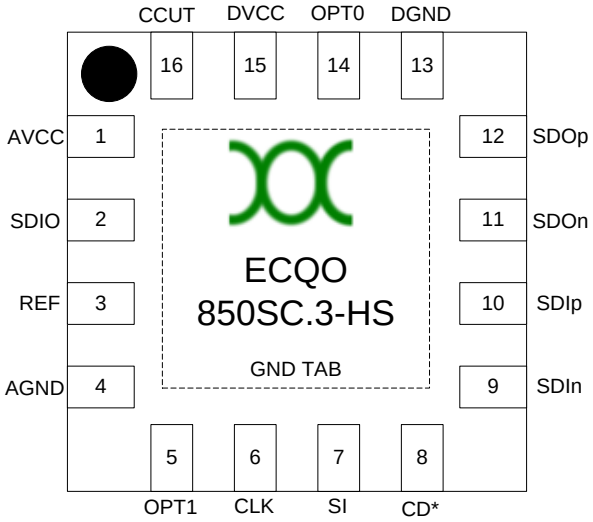

Figure 2: EQCO850SC.3-HS (EQCO875SC.3-HS) Pin Layout (viewed from top)[2]

2.3 Pin Descriptions

Pin Number	Pin Name	Signal Type	Description
(TAB)	GND	Power	Connect to ground of power supply
15	DVCC	Power	Connect to +3.3 V of power supply
13	DGND	Power	Connect to ground of power supply
1	AVCC	Power	Analog VCC Connect to +3.3 V of power supply via RF choke and capacitor to cable outer screen
4	AGND	Power	Analog GND Connect to cable outer screen
2	SDIO	Bidirectional	Serial Input Output Connect to centre conductor of 50 Ω coax cable.
3	REF	Bidirectional	Reference Connect through 50Ω resistor (or impedance matched to cable) to cable outer screen
8	CD*	Output (open drain)	Leave unconnected. Use of this pin is not advised in practice.
10, 9	SDIp/SDIn	Input	Serial Input Positive/Negative Differential serial input. Connect to the LVDS output
12, 11	SDOp/SDOn	Output	Serial Output Positive/Negative Differential serial output. Connect to the LVDS input
14, 5	OPT0, OPT1	Input	Connect Opt0 and Opt1 both to DVCC (3.3V) for correct mode selection.
6, 7	CLK, SI	Input	Used for Production test, Connect to DGND
16	CCUT	Analog	Not used in LVDS applications. Connect to pin 15 DVCC

Table 1: Device Pin List

[2] Devices named EQCO850SC.2 can be used for all applications contained in this data-sheet. They are the same in all aspects.

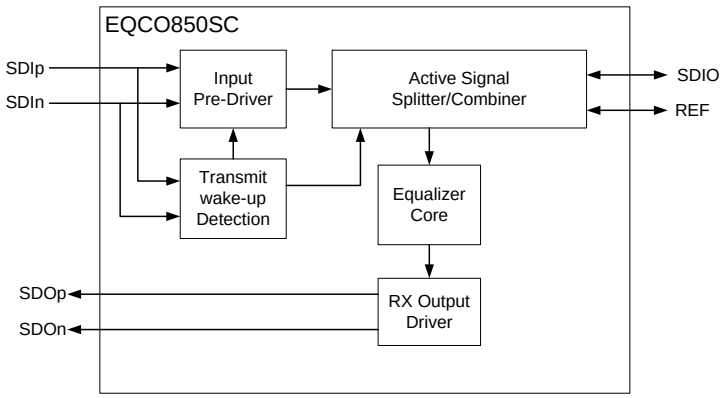

Figure 3: EQCO850SC-HS block diagram showing electrical connections

2.3.1 SDIp/SDIn

SDIp/SDIn together form a differential input pair. The serial data received on these pins will be transmitted on SDIO. The Input Pre-Driver automatically corrects for variations in signal levels and different edge slew rates at these inputs before they go into the Active Splitter/Combiner for transmission over the coax.

SDIp and SDIn inputs are differentially terminated by 100 Ω on chip. The center of the 100 Ω is connected to DGND with a 10 kΩ resistor for DC biasing. The inputs also have protection diodes to ground for ESD purposes. Always AC-couple these inputs to the outputs of the LVDS driver.

A Transmit Wake-up detection circuit puts both the Input Pre-Driver and the Active Signal Splitter/Combiner into a low power mode when no signal is detected on the SDIp/SDIn signal pair (except in mode B, where transmit circuit is permanently ON).

2.3.2 SDIO/REF

The signal on the SDIO pin is the sum of the incoming signal (i.e. the signal transmitted by the EQCO850SC-HS on the far end side of the coax) and the outgoing signal (i.e. the signal created based on SDIp/SDIn). The far end signal is extracted by subtraction of the near end signal and it is this voltage that the equalizer analyses and adaptively equalizes for level and frequency response based on the knowledge that the originating signal is DC balanced and Run length encoded before transmission.

The REF signal carries a precise anti-phase current to the transmit current on SDIO. REF must be connected directly to AGND **at the connector** (see Figure) via a resistor precisely matched to the impedance of the coaxial cable used.

2.3.3 SDOp/SDOn

SDOp/SDOn together form a differential pair outputting the reconstructed far end transmit signal. The EQCO850SC-HS uses LVDS drivers with source matching for a 100 Ω transmission line. This LVDS signal can normally be connected (subject to input common mode requirements) directly to the RX signal pair of a standard LVDS receiver.

2.3.4 CLK, SI

These pins are used for production test and/or reserved for future options. For normal operation connect them to DGND as indicated in Table 1.

2.4 Circuit Operation

2.4.1 Pre-driver

The Pre-driver removes any dependency on LVDS transmitter for the amplitude and rise time of the outgoing signal on SDIO.

2.4.2 Active signal splitter/combiner

The active splitter/combiner [1] controls the amplitude and rise time of the outgoing coax signal and transmits it via a precise 50Ω output termination resistor. The output resistor when balanced with the coax characteristic impedance also forms part of a hybrid splitter circuit which subtracts the TX output from the signal on the SDIO output to give yield the far end TX signal. The return loss of the coax termination is a key factor in the performance of the line hybrid.

2.4.3 Equalizer Core

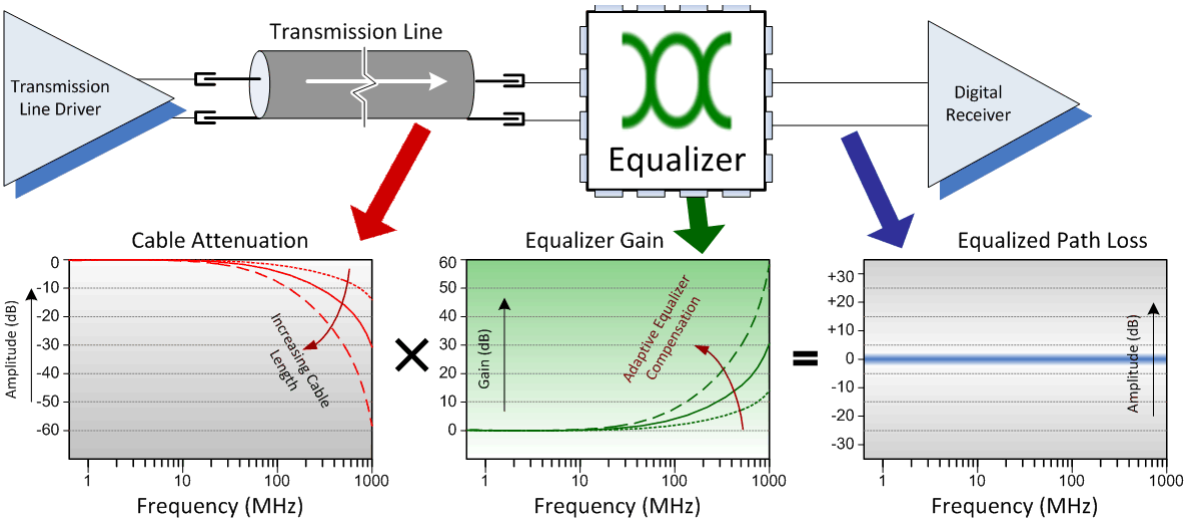

Figure 5: Principal of Equalizer Operation

The EQCO850SC-HS has an embedded high speed equalizer [2] in the receive path with unique characteristics:

- Auto-adaptive

  The equalizer controls a multiple pole analog filter which compensates for attenuation of the cable, as illustrated in Figure 5. The filter frequency response needed to restore the signal is automatically determined by the device using a time-continuous feedback loop that measures the frequency components in the signal. Upon the detection of a valid signal, the control loop converges within a few microseconds.

- Variable gain

  EQCO850SC-HSs are used in pairs; one at each end of the coax. The EQCO850SC-HS can be used with any LVDS driver with a differential transmit amplitude in the range of 300 mV to 800 mV; the transmit amplitude on the coax is regulated by the input pre-driver. The receiver equalizer has variable gain to compensate for attenuation through the coax.

Example equalizer performance measurements can be found in Appendix 1.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under this section may cause permanent damage to the device. These are stress ratings only and are not tested. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Conditions	Min	Typ	Max	Units
Storage Temperature		-65		+150	°C
Ambient Temperature	Power Applied	-55		+125	°C
Operating Temperature	Normal Operation (VCC=3.3 V±5%)	-40		+85	°C
Supply Voltage to Ground		-0.5		+4.0	V
DC Input Voltage		-0.5		+4.0	V
DC Voltage to Outputs		-0.5		+4.0	V
Output current into Outputs	Outputs Low			90	mA
Electro Static Discharge (ESD) HBM	JEDEC EIA/JESD-A114A	>3.3			kV
Electro Static Discharge (ESD) contact	IEC 61000-4-2	>8			kV
Latch-Up Current		>200			mA(DC)

Table 2: Absolute Maximum Ratings

3.2 Electrical Characteristics

Parameter	Description	Min	Typ	Max	Unit
Power supply					
V_{CC}	Supply Voltage	3.135	3.3	3.465	V
I_s	Supply Current, both transmitting and receiving[2]	47.5	62.5	75.5	mA
I_{sr}	Supply Current when only receiving[2]	25	35	43	mA
SDIp/SDIn Inputs (LVDS like)					
ΔV_i	Input amplitude $V_{SDIp,n}$[2]	250		800	mV
V_{turnon}	Minimal ΔV_i to turn on transmit function	80	140	200	mV
V_{cmin}	Common-mode input voltage (terminated to DGND via 10 kΩ and with protection diodes)[3]	Note 4	0	Note 4	V
R_{input}	Differential input termination[2]	93	104	117	Ω
SDIO connection to Coax					
Z_{coax}	Coax Cable Characteristic Impedance	48 (72)	50 (75)	52 (78)	Ω
R_{SDIO}	Input impedance between SDIO and AGND[2]	46 (69)	51 (76)	55 (82)	Ω
R_{loss}	Coax Return Loss as seen on SDIO pin Frequency range = 10 MHz-625 MHz	15			dB
ΔV_{TX}	Transmit Amplitude	270	325	380	mV

Parameter	Description	Min	Typ	Max	Unit
t_{rise_tx}	Rise/fall time 20% to 80% of ΔV_{TX} [3]	350	450	550	ps
Att_{max}	Cable Attenuation Budget @ 625MHz (S800) [3]		12		dB
$\Delta V_{RX\ min}$	Minimum input for fully reconstructed output [3]		40		mV
SDOp/SDOn Outputs (LVDS compatible)					
ΔV_o	Output amplitude $V_{SDOp,n}$ [2]	300	350	400	mV
V_{cmout}	Common-mode output voltage [2]	1.1	1.2	1.3	V
ΔV_{o_off}	Output amplitude $V_{SDOp,n}$ with equalizer OFF [3]	-20	0	20	mV
R_{output}	Differential termination between SDOp and SDOn [2]	92	102	115	Ω
t_{rise_o}	Rise /fall time 20% to 80% of $V_{SDOp,n}$	150	240	350	ps

Table 3: Electrical Characteristics (see notes), EQCO850SC.3-HS and (EQCO875.3-HS)

[1] Over full VCC range

[2] Over full VCC range and full operating temperature range (-40 ^{o}C to 85 ^{o}C)

[3] Guaranteed by design

[4] SDI Inputs are protected by silicon input diodes, clamping their maximum input voltage to $\pm$ 0.6V

3.3 Jitter Performance

Parameter	Conditions	Min	Typ	Max	Units
Jitter peak to peak on SDO	1 m RG174 coax; over full Vcc, $\Delta V_{TX,}$ and Temp range; 125-1250Mbps ; pattern PRBS7		70	230	ps
Jitter peak to peak on SDO	16 m RG174 coax; over full Vcc, $\Delta V_{TX,}$ and Temp range; 125-1250Mbps ; pattern PRBS7		170	300	ps

Table 4: Jitter at SDO.

4 Package Drawing

A 16 pin Micro Lead frame Package (MLP) also known as Quad Flat No Lead (QFN) package is used. The package outline conforms to JEDEC MO-220.

Dimensions in Figure 6 and Figure 7 are in millimeters.

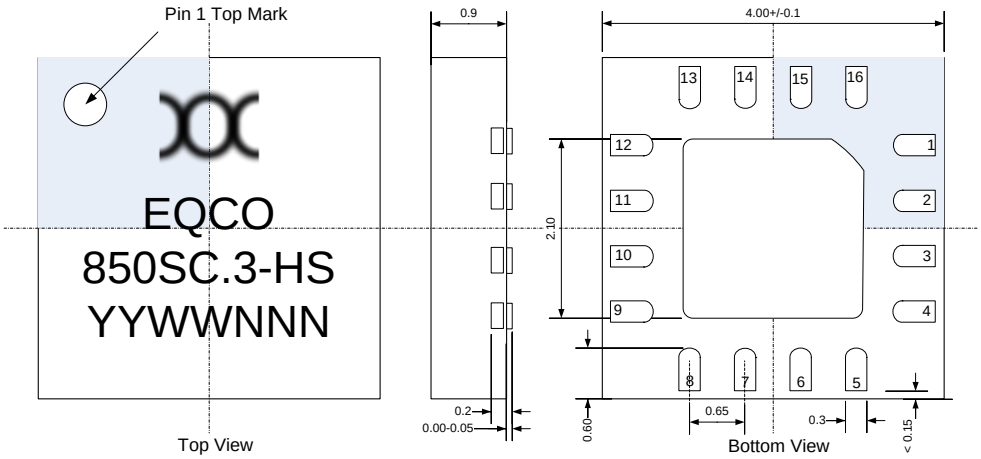

Figure 6: Package Drawings

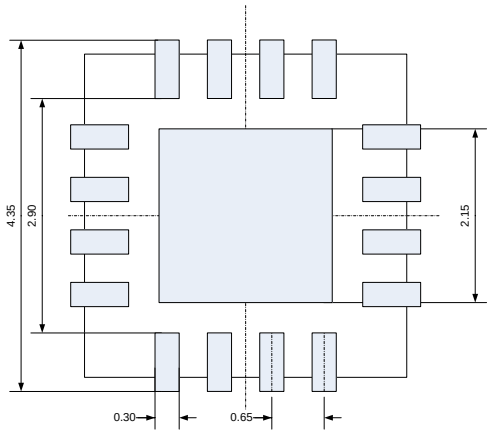

Figure 7: Recommended PCB Footprint for both types of packages

5 Application Information

5.1 Typical Application Circuit

Figure illustrates a typical schematic implementation:

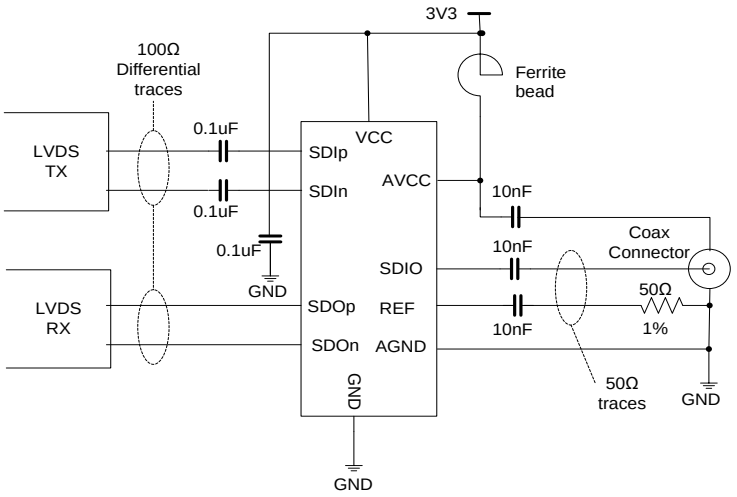

Figure 8: Example Schematic Implementation for EQCO850SC.3-HS.
For EQCO875SC.3-HS replace the two 50Ω references with two times 75Ω.

To improve isolation from noise on the board power plane and improve EMC immunity and emissions, it is recommended to power the transmit side of equalizer (AVCC) through a ferrite bead. A 0.1-µF decoupling capacitor should be placed as close as possible to the chip between the VCC pin and the GND pin. Ground vias should be placed as close as possible to the device GND pins to minimize inductance.

In full duplex, the maximum length performance depends on the level of near-end cross-talk and far-end return-loss. Therefor it is recommended for full duplex operation to position the chip close to the used connector. Also one has to choose for either a 50-Ω system or a 75-Ω system.

All the elements need then to have impedances according to that choice: the chips used on both sides, the impedances between the chip and the connector, the PCB connector itself (!), the connectors on the coax cable, and the coax. If one impendance is wrong (e.g. a 75-Ω BNC connector in a 50-Ω system) this impedance discontinuity will give a sligh or a strong reflection, limiting the performance of the full-duplex maximum cable reach.

5.2 PCB layout

Because signals are strongly attenuated by a long cable, special attention must be paid on the PCB layout between the coaxial connector and the EQCO850SC-HS. The EQCO850SC-HS should be as close as is practical to the coaxial connector. The trace between the coaxial connector and the EQCO850SC-HS (EQCO875SC-HS) must be a 50-Ω (75-Ω) trace referenced to GND. To avoid noise pickup, other traces carrying digital signals or fast switching signals should be placed as far away as possible from this trace.

The following diagram shows the layout of the critical section of the PCB, from the coax connector to the twin differential input pairs:

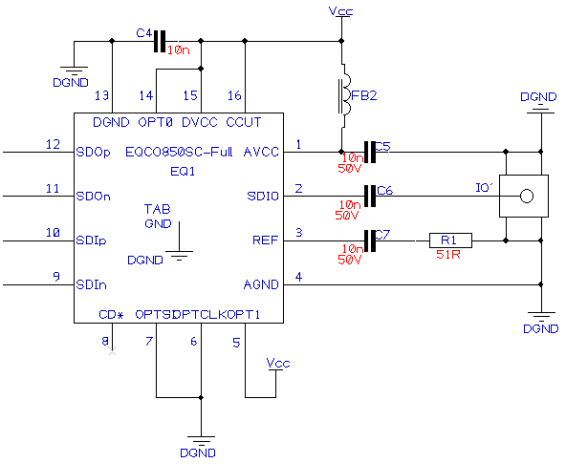

Figure 9: Circuit diagram (part)

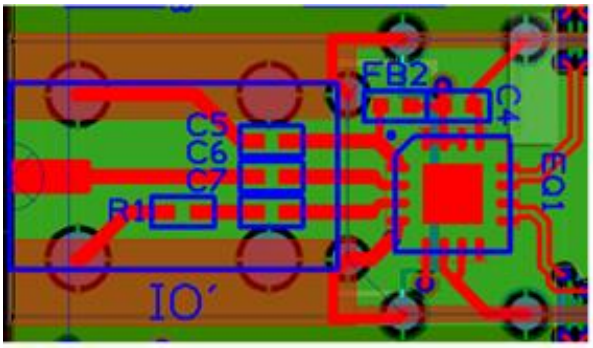

Figure 10: Recommended Layout

The ground layout on the EQCO850SC.3-HS is critical to the EMC and EMI performance of the circuit. The AGND connection should be made directly to the body of the connector as shown in Figure 9. It should not be connected directly to the GND tab of the chip. Similarly AVCC should be decoupled directly to the connector body (see position of C5). The termination resistor (R1 in Figure 9 and Figure 10) must have its ground connection at the connector body and the C7, the connection between R1 and the connector must be kept as short as possible. The impedance of all the traces must be well controlled, including on the connector itself.

The SDIp/SDIn and SDOp/SDOn differential traces should be matched in length to minimize time of arrival skew. For traces longer than a few mm the impedance of the differential transmit and receive signals should be laid out as 100Ω differential traces and the termination to the PHY should be placed close to the PHY, not to the EQCO850SC.3-HS.

EqcoLogic N.V. can design a PCB-layout that allows to reach maximum cable length for any combination of impedance system (50Ω or 75 Ω) and coax connector (SMA, BNC, DIN, SMB…) on request.

6 Document Control

6.1 Version History

Version	Date	Author	Comments
2v0	28 Jan 2014	M. Kuijk	Targeting datasheet for LVDS and Gigabit Ethernet applications. Merging 50 Ω and 75 Ω systems in one datasheet. Temperature limits set to -45 °C … 85°C
1v0	30 Apr 2010	S. E. Ellwood/M. Kuijk	Based on EQCO800SC Generic Datasheet, adapted for LVDS.

6.2 Document References

[1] Patents & Patents Pending: EP2237419A1, US8164358B2, EP2237435B1 US8488685B2
[2] Patents: EP2182688B1 & US7894515B2

6.3 Ordering Information

Order Code	Application	Production	Package Type	Operating Range
EQCO850SC.2	50 Ω Coax	End of Life	16 Pin, 4 mm QFN	-45°C…+85°C
EQCO875SC.2	75 Ω Coax	End of Life	16 Pin, 4 mm QFN	-45°C…+85°C
EQCO850SC.3-HS	50 Ω Coax	In Qualification	16 Pin, 4 mm QFN	-45°C…+85°C
EQCO875SC.3-HS	75 Ω Coax	In Qualification	16 Pin, 4 mm QFN	-45°C…+85°C

EQCO850SC.2 and EQCO850.3-HS consist of the same silicon and the same package.
EQCO875SC.2 and EQCO875.3-HS consist of the same silicon and the same package.

6.4 Disclaimer:

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Appendix 1: Typical Operating Characteristics

All measurements at VCC = 3.3 V, Temp = +25ºC, data pattern = PRBS9, 630 mV PHY Transmit amplitude

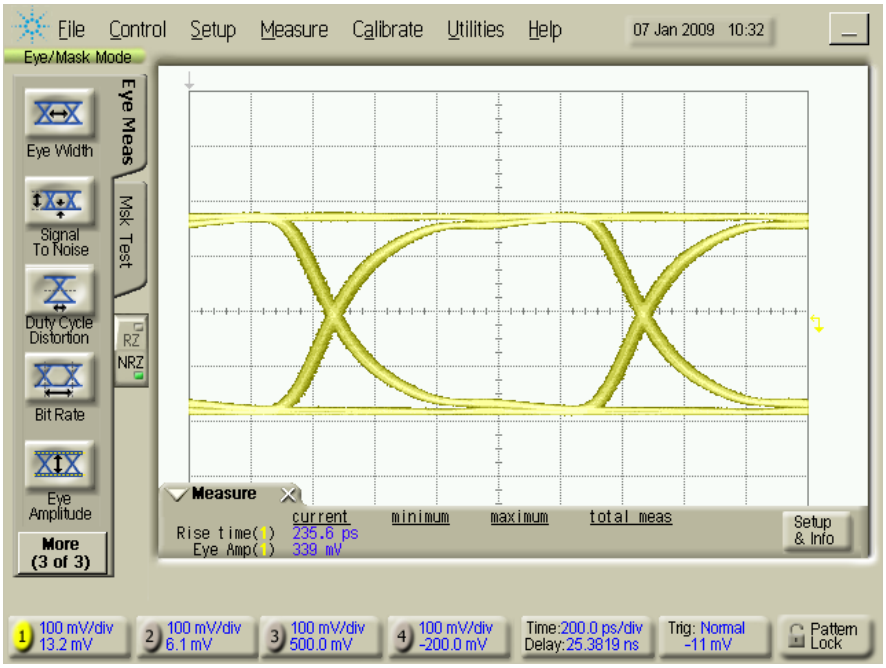


Fig. 11. Typical eye at SDO_p with a 1 m Coax type RG174.

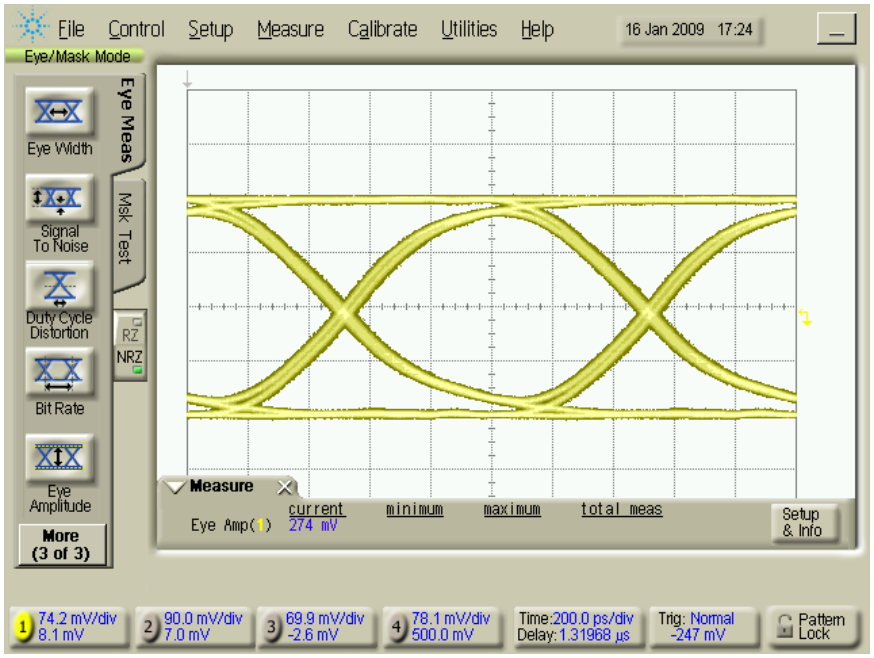


Fig. 12. Typical eye at SDIO output through 1 m COAX cable.

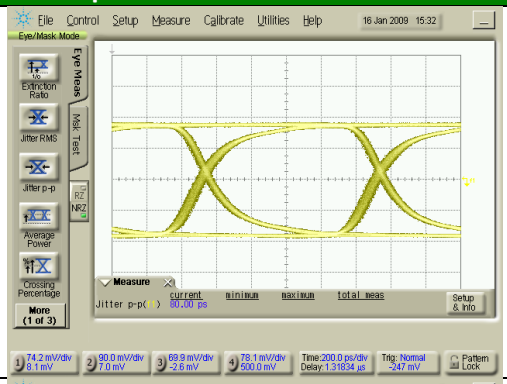
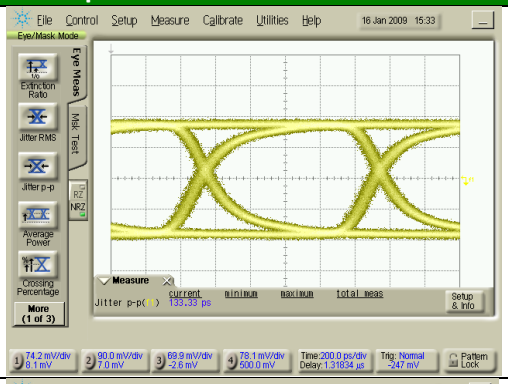
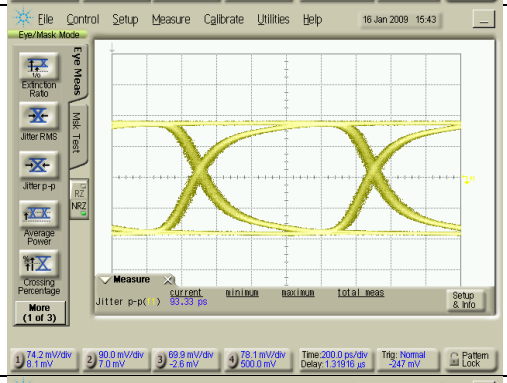
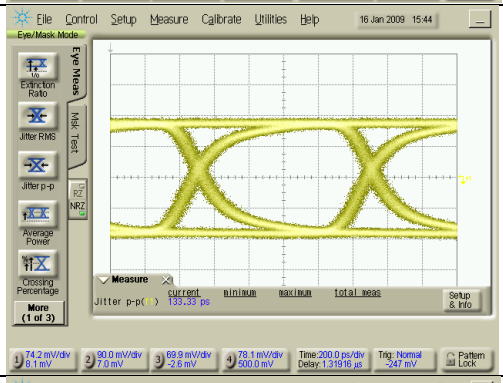
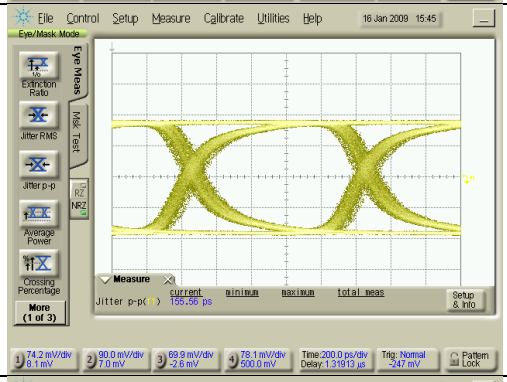
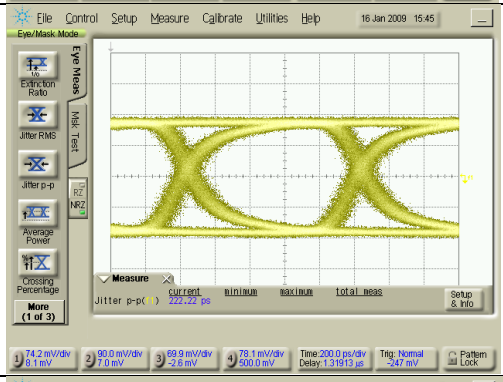
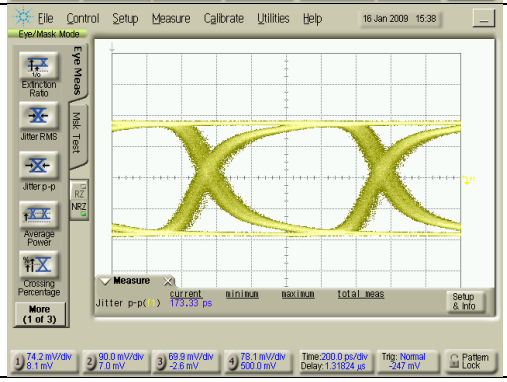
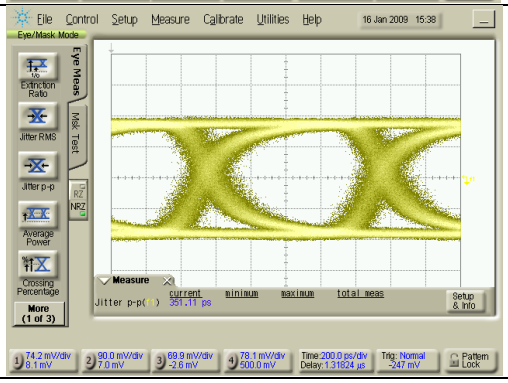
	Half duplex	Full duplex
1 m RG174		
5 m RG174		
10 m RG174		
20 m RG174		

Fig. 13. Typical system link EYE-diagram at room temperature through a variable cable length full and half duplex. Shown is the differential output, i.e. V_{SDOp}-V_{SDOn}.
The Duty Cycle Distortion is due to the used shielded twisted pair cable/connector. DCD is normally very small.

