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October 2015

FDN86501LZ

N-Channel Shielded Gate PowerTrench® MOSFET 60 V, 2.6 A, 116 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 116 mΩ at V_{GS} = 10 V, I_D = 2.6 A
- Max $r_{DS(on)}$ = 173 mΩ at V_{GS} = 4.5 V, I_D = 2.1 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL tested
- RoHS Compliant

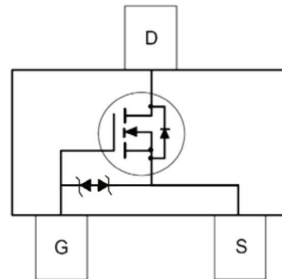
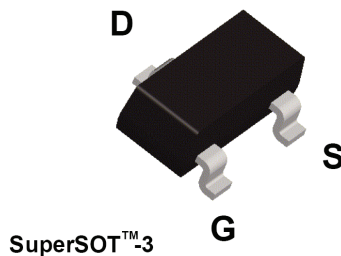


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Applications

- Primary DC-DC Switch
- Load Switch



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Ratings | Units |
|----------------|--|---------------|-------|
| V_{DS} | Drain to Source Voltage | 60 | V |
| V_{GS} | Gate to Source Voltage | ±20 | V |
| I_D | -Continuous | (Note 1a) 2.6 | A |
| | -Pulsed | (Note 4) 24 | |
| E_{AS} | Single Pulse Avalanche Energy | (Note 3) 6 | mJ |
| P_D | Power Dissipation | (Note 1a) 1.5 | W |
| | Power Dissipation | (Note 1b) 0.6 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|-----------------|---|--------------|------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) 75 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) 80 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|------------|---------|-----------|------------|------------|
| 8650 | FDN86501LZ | SSOT-3 | 7" | 8 mm | 3000 units |

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|--------|-----------|-----------------|------|------|------|-------|
|--------|-----------|-----------------|------|------|------|-------|

Off Characteristics

| | | | | | | |
|--------------------------------------|---|---|----|----|----------|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$ | 60 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ | | 68 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$ | | | 1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | | | ± 10 | μA |

On Characteristics (Note 2)

| | | | | | | |
|--|--|---|-----|-----|-----|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$ | 1.0 | 1.9 | 2.4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$ | | -5 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10\text{ V}, I_D = 2.6\text{ A}$ | | 89 | 116 | m Ω |
| | | $V_{GS} = 4.5\text{ V}, I_D = 2.1\text{ A}$ | | 121 | 173 | |
| | | $V_{GS} = 10\text{ V}, I_D = 2.6\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | | 152 | 198 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 10\text{ V}, I_D = 2.6\text{ A}$ | | 8 | | S |

Dynamic Characteristics

| | | | | | | |
|-----------|------------------------------|--|-----|-----|-----|----------|
| C_{iss} | Input Capacitance | $V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$ | | 236 | 335 | pF |
| C_{oss} | Output Capacitance | | | 77 | 110 | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 4.9 | 10 | pF |
| R_g | Gate Resistance | | 0.1 | 0.8 | 2.0 | Ω |

Switching Characteristics

| | | | | | | | |
|--------------|-------------------------------|--|---|-----|-----|-----|----|
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD} = 30\text{ V}, I_D = 2.6\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$ | | 4.4 | 10 | ns | |
| t_r | Rise Time | | | 1.2 | 10 | ns | |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 9.6 | 20 | ns | |
| t_f | Fall Time | | | 1.2 | 10 | ns | |
| Q_g | Total Gate Charge | | $V_{GS} = 0\text{ V to } 10\text{ V}$ | | 3.8 | 5.4 | nC |
| Q_g | Total Gate Charge | $V_{GS} = 0\text{ V to } 4.5\text{ V}$ | $V_{DD} = 30\text{ V},$ $I_D = 2.6\text{ A}$ | | 1.9 | 2.7 | nC |
| Q_{gs} | Gate to Source Gate Charge | | | | 0.7 | | nC |
| Q_{gd} | Gate to Drain "Miller" Charge | | | | 0.6 | | nC |

Drain-Source Diode Characteristics

| | | | | | | |
|----------|---------------------------------------|--|--|-----|-----|----|
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 2.6\text{ A}$ (Note 2) | | 0.9 | 1.3 | V |
| t_{rr} | Reverse Recovery Time | $I_F = 2.6\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | | 31 | 50 | ns |
| Q_{rr} | Reverse Recovery Charge | | | 19 | 31 | nC |

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $80\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $180\text{ }^\circ\text{C/W}$ when mounted on a minimum pad.

2. Pulse Test: Pulse Width < $300\text{ }\mu\text{s}$, Duty cycle < 2.0%.

3. E_{AS} of 6 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 2\text{ A}$, $V_{DD} = 60\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 9\text{ A}$.

4. Pulsed I_d please refer to Fig 11 SOA graph for more details.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

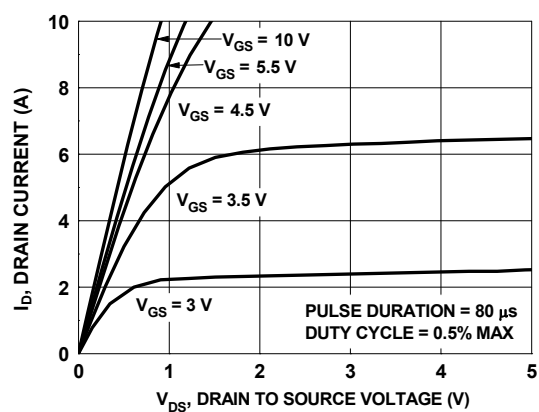


Figure 1. On Region Characteristics

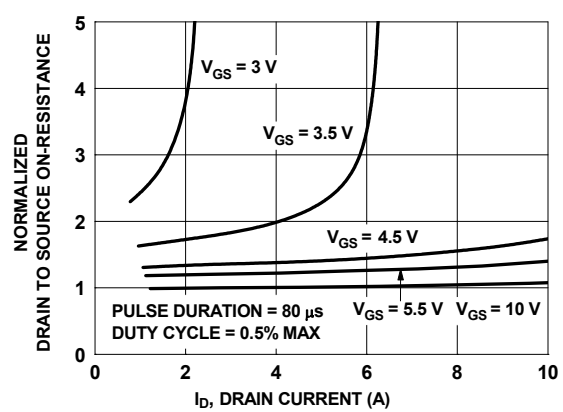


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

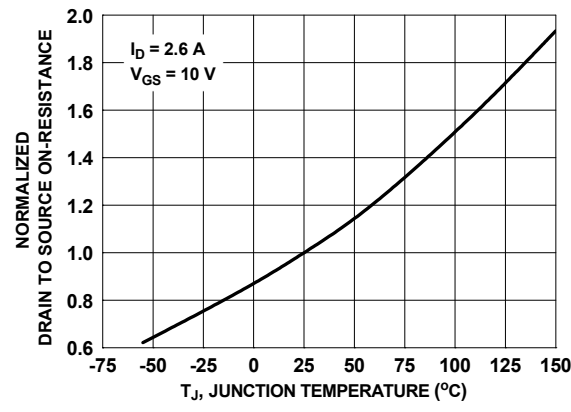


Figure 3. Normalized On Resistance vs. Junction Temperature

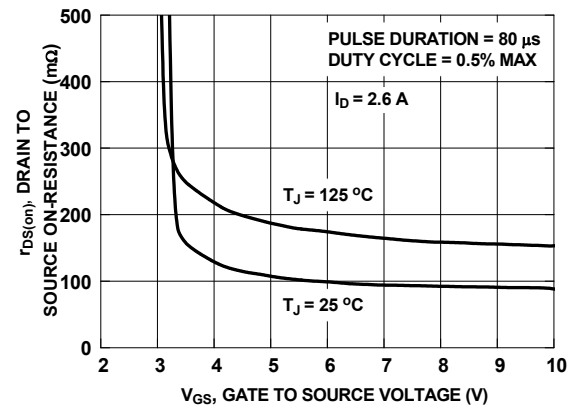


Figure 4. On-Resistance vs. Gate to Source Voltage

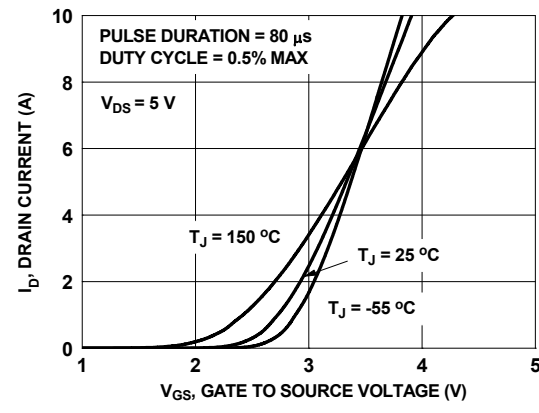


Figure 5. Transfer Characteristics

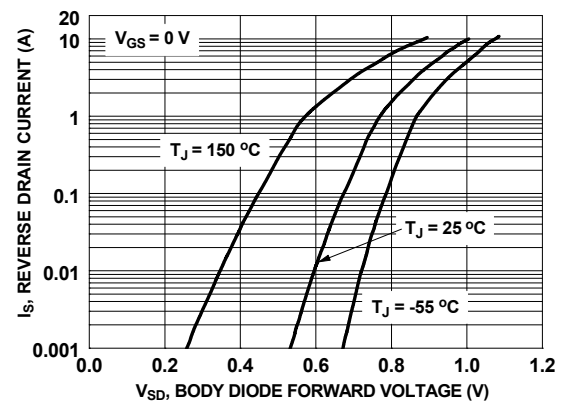


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

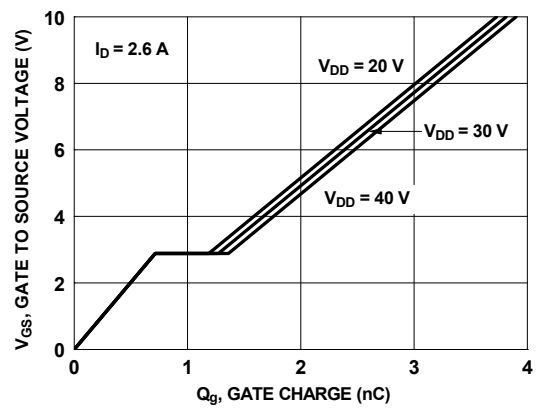


Figure 7. Gate Charge Characteristics

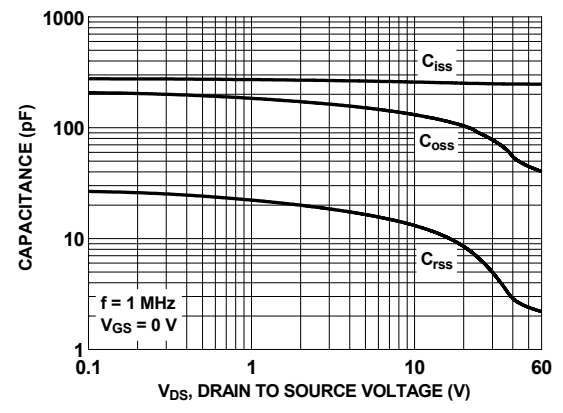


Figure 8. Capacitance vs. Drain to Source Voltage

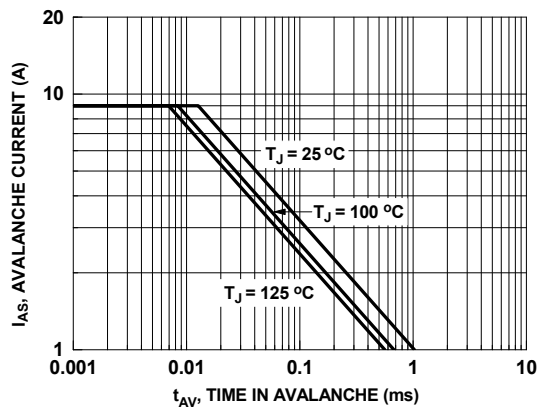


Figure 9. Unclamped Inductive Switching Capability

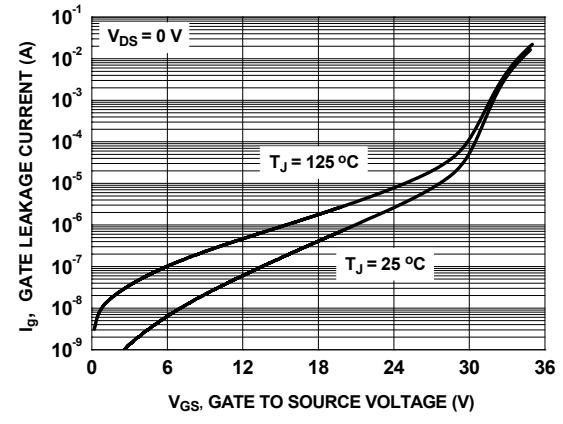


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

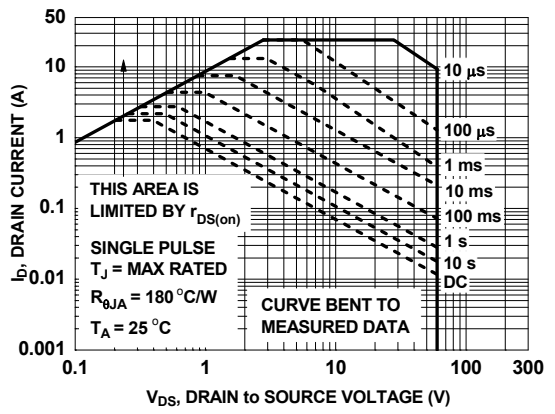


Figure 11. Forward Bias Safe Operating Area

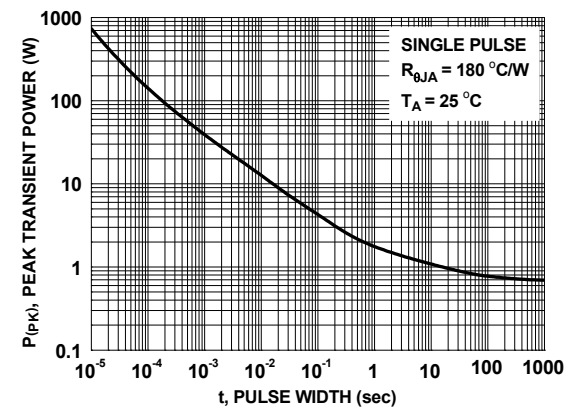


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

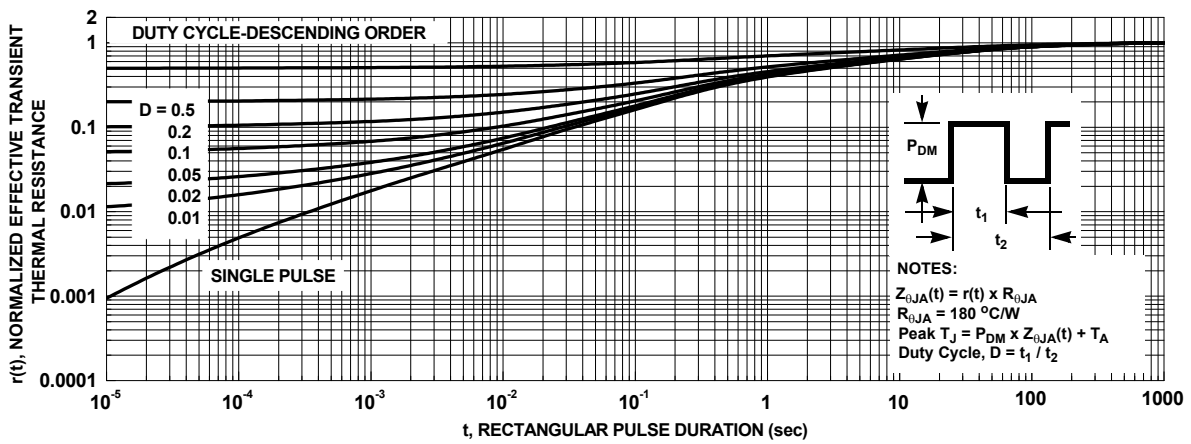
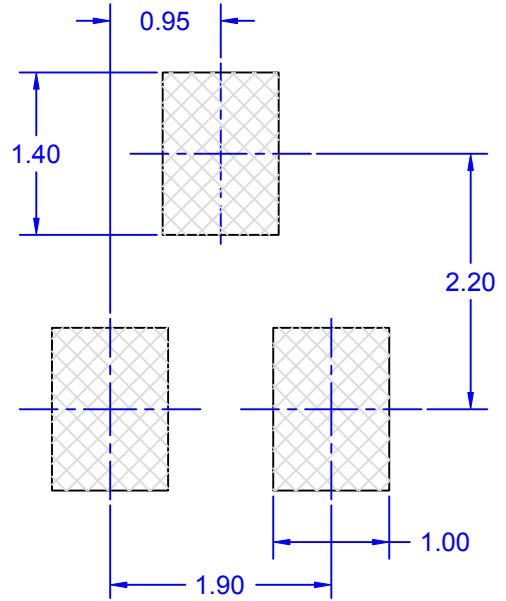
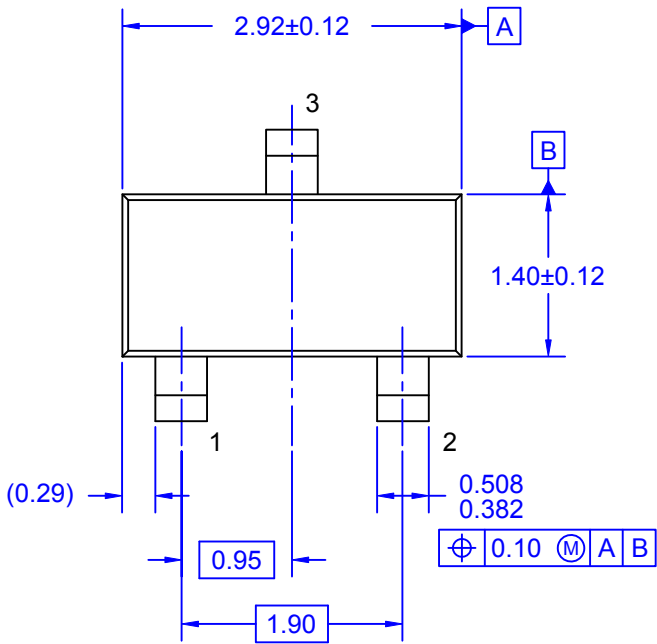
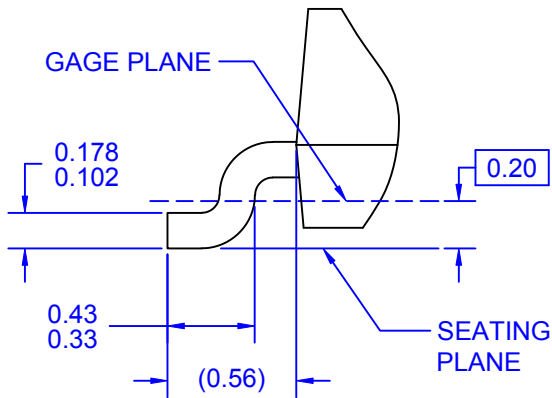
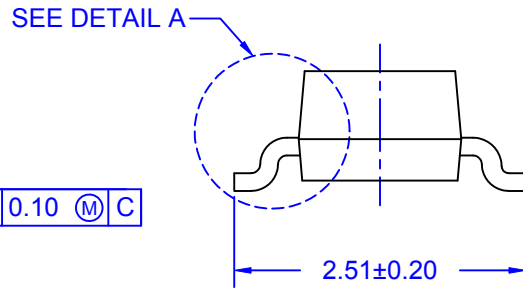
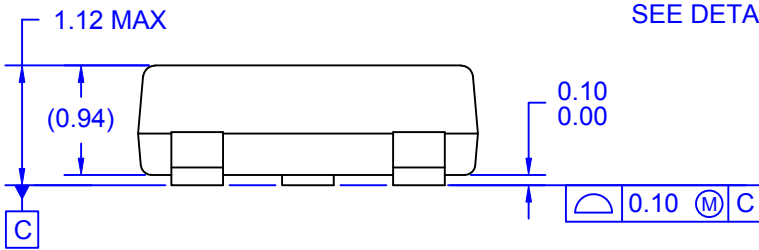


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



LAND PATTERN RECOMMENDATION



DETAIL A
 SCALE: 50:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A) NO JEDEC REFERENCE AS OF AUGUST 2003
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
- E) DRAWING FILE NAME: MKT-MA03BREV3



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