SPECTRUM DIGITAL INCORPORATED

OMAP-L137 Evaluation Module

Technical Reference

2008 ***DSP Development Systems***

OMAP-L137 Evaluation Module Technical Reference

511345-0001 Rev. A
November 2008

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Contents

About This Manual

This document describes the board level operations of the OMAP-L137 Evaluation Module (EVM). The EVM is based on the Texas Instruments OMAP-L137 Processor.

The OMAP-L137 Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the OMAP-L137 processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The OMAP-L137 Evaluation Module will sometimes be referred to as the OMAP-L137 EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding the OMAP-L137 can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Beta

Table 2: Board History

PWB Revision	History
D	Beta Release

Chapter 1

Introduction to the OMAP-L137 EVM

Chapter One provides a description of the OMAP-L137 EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The OMAP-L137 EVM is a standalone development platform that enables users to evaluate and develop applications for the OMAP-L137 processor. Schematics and application notes are available to ease hardware development and reduce time to market.

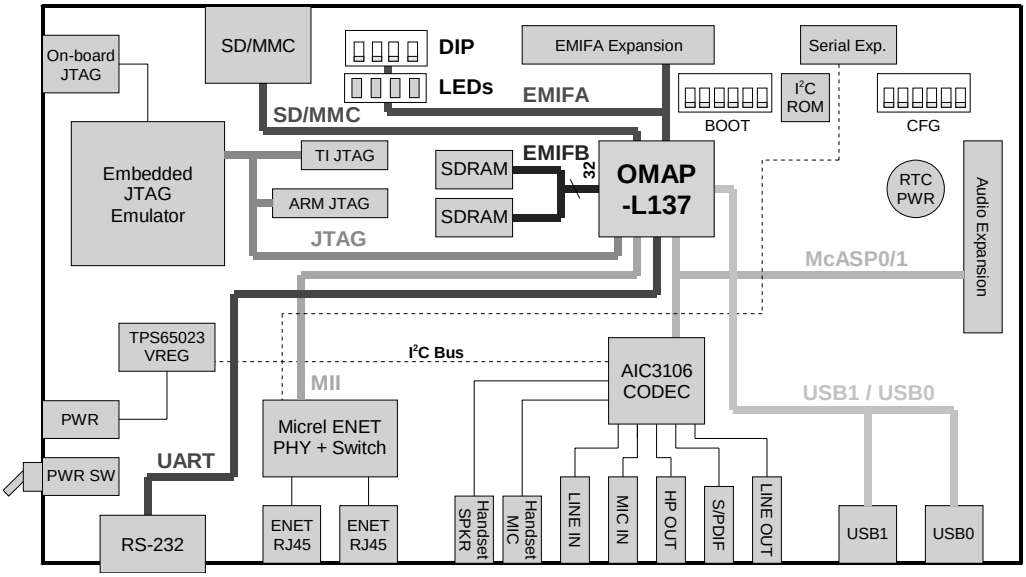

Figure 1-1, Block Diagram OMAP-L137 EVM

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments OMAP-L137 device with a C674x VLIW DSP floating point processor and an ARM926EJ-S processor operating up to 300 Mhz.
- 64 Megabytes SDRAM
- SPI Boot EEPROM
- 2 Port Ethernet Phy/switch
- SD/MMC/MMC Plus media card interfaces
- TLV320AIC3106 Stereo Codec
- USB 1.1 High speed interface
- USB2 2.0 Full speed interface
- RS-232 Interface

- On chip real time clock
- Configurable boot load options
- 4 user LEDs/4 position user DIP switch
- Single voltage power supply (+5V)
- Expansion connectors for daughter card use
- Embedded JTAG Emulation
- 14 Pin TI JTAG/20 Pin ARM JTAG Interfaces

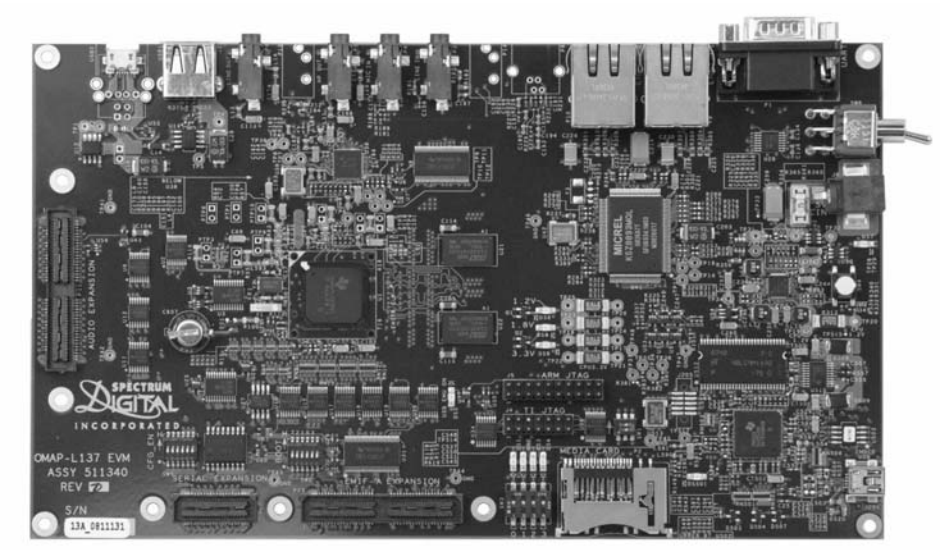

Figure 1-2, OMAP-L137 EVM

1.2 Functional Overview of the OMAP-L137 EVM

The OMAP-L137 on the EVM interfaces to on-board peripherals through the 16-bit wide multiplexed EMIF interface pins. The SDRAM memory is connected to its own dedicated 32 bit wide bus.

An on-board AIC3106 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McASP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, headphone output, line input, and line output.

The EVM includes 4 user LEDs, a 4 position user DIP switch, and on chip real time clock. On board multi-plexing allows ease of interfacing to the daughter cards.

An included +5V external power supply is used to power the board. On-board switching voltage regulators provide the CPU core voltage, +3.3V, +1.8V for peripheral interfacing. The board is held in reset by the on board power controller until these supplies are within operating specifications.

Code Composer Studio communicates with the EVM through an embedded emulator or via the TI 14 pin or ARM 20 pin external JTAG connectors.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio IDE™, or MontaVista tool environments. Code Composer communicates with the board through an on board JTAG emulator. This EVM is shipped with an EVM specific Code Composer Studio environment. To start, follow the instructions in the Quick Start Guide to install Code Composer. This process will install all of the necessary development tools, documentation and drivers.

1.4 Memory Map

The OMAP-L137 processor has a byte addressable address space. However, there are some limitations to byte addressing determined by peripheral interconnection to the OMAP-L137 device. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The memory map shows the address space of a generic OMAP-L137 processor on the left with specific details of how each region is used on the right. By default, the internal memory sits at the beginning of the address space. Portions of memory can be remapped in software as L2 cache rather than fixed RAM.

The part incorporates a dual EMIF interface. One dedicated EMIF, EMIF-B, directly interfaces to the SDRAM memory. EMIF-A has 3 separate addressable regions called chip enable spaces (CE0, CS2, CS3), however the EVM uses this interface as a peripheral interface to daughter card connectors. The memory map of the OMAP-L137 EVM is shown in the table below.

Table 1: OMAP-L137 EVM Memory Map

Start Address	End Address	ARM Mem Map	DSP Mem Map
0x0080 0000	0x0083 FFFF		DSP L2 RAM
0x00E0 0000	0x00f0 7FFFF		DSP L1P RAM
0x00F0 0000	0x00F0 8000		DSP L1D RAM
0x0184 0000	0x0184 FFFF		DSP Memory System
0x1180 0000	0x1183 FFFF	DSP L2 RAM	
0x11E0 0000	0x11E0 7FFF	DSP L1P RAM	
0x1FF0 0000	0x11F0 7FFF	DSP L1D RAM	
0x8000 0000	0x8001 FFFF	Shared RAM	
0xB000 0000	0xB000 7FFF		EMIFB control regs
0xC000 0000	0xDFFF FFFF		EMIFB SDRAM Data
0xFFFE E000	0xFFFE FFFF	ARM Interrupt Controller	
0xFFFF 0000	0xFFFF 1FFF	ARM Local RAM	

1.5 Boot Switch Settings

The EVM has a 5 position switch that allow users to configure the operational state of the processor when it is released from reset and determine the source for processor booting. Switch SW2 configures the boot mode that will be used when the DSP starts executing. By default the switches are configured to serial EEPROM boot. The table below shows the boot mode sources and their respective switch positions.

Table 2: SW2, Boot Mode Select

Pos 1 Boot[7]	Pos 2 Boot[2]	Pos 3 Boot[1]	Pos 4 Boot[0]	Pos 5 Boot[3]	Boot Pin BTMODE[7,2,1,0,3]	Boot Mode
OFF	OFF	OFF	ON	NA	0 0 0 1 x	NOR
OFF	OFF	ON	OFF	NA	0 0 1 0 x	HPI
OFF	ON	OFF	ON	NA	0 1 0 1 x	SPI0 Flash
OFF	ON	ON	OFF	NA	0 1 1 0 x	SPI1 Flash
OFF	ON	ON	ON	NA	0 1 1 1 x	NAND 8-bit
OFF	OFF	OFF	OFF	OFF	0 0 0 0 0	I^2C0 Master
OFF	OFF	OFF	OFF	ON	0 0 0 0 1	I^2C0 Slave
OFF	OFF	ON	ON	OFF	0 0 1 1 0	I^2C1 Master
OFF	OFF	ON	ON	ON	0 0 1 1 1	I^2C1 Slave
OFF	ON	OFF	OFF	OFF	0 1 0 0 0	SPI0 EEPROM *
OFF	ON	OFF	OFF	ON	0 1 0 0 1	SPI1 EEPROM
ON	OFF	OFF	ON	OFF	1 0 0 1 0	SPI0 Slave
ON	OFF	OFF	ON	ON	1 0 0 1 1	SPI1 Slave
ON	OFF	ON	ON	OFF	1 0 1 1 0	UART0
ON	OFF	ON	ON	ON	1 0 1 1 1	UART1
ON	OFF	ON	OFF	OFF	1 0 1 0 0	UART2 *****
ON	ON	ON	ON	OFF	1 1 1 1 0	Emulation Debug *****

***** Supported on Standalone EVM

1.6 Power Supply

The EVM operates from a single +5V external power supply connected to the main power input (J6), a 2.5 MM. barrel-type plug. Internally, the +5V input is converted into core voltage, +1.8V and +3.3V using Texas Instruments TPS65023 Power Management Unit. The +3.3V and +1.8V supply are used for the DSP's I/O buffers and other chips on the board.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the OMAP-L137 EVM.

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2.1 EMIF-A Interfaces

A separate 16 bit EMIF with three chip enables divide up the address space and allow for asynchronous accesses on the EVM. The EVM uses this interface for peripheral interfaces to the daughter card.

2.1.1 EMIF-B SDRAM Memory Interface

The OMAP-L137 device incorporates a dedicated 32 bit wide SDRAM memory bus. The EVM uses two 256 Megabit, 16 bit wide memories on this bus, for a total of 64 megabytes of memory for program, data, and video storage. The internal SDRAM controller uses a PLL to control the SDRAM memory timing. Memory refresh for SDRAM is handled automatically by the OMAP-L137 internal SDRAM controller.

2.1.2 Memory Card Interface

The EVM supports SD/MMC/MMC PLUS media card interfaces. This interface is multiplexed with other function the EMIFA bus.

2.1.3 UART Interface

The internal UART2 on the OMAP-L137 device is driven to connector P1. The UART's interface is routed to the RS-232 line drivers prior to being brought out to a DB-9 connector, P1.

2.1.4 USB Interface

The OMAP-L137 incorporates two on chip USB controllers. The USB 2.0 interface is brought out to a micro A/B connector. A jumper is provided to make a flexible host, peripheral, and USB on the go interface. The second USB 1.1 interface is brought out to an A type host interface connector.

2.2 AIC3106 Interface

The EVM incorporates a Texas Instruments TLV320AIC3106 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the AIC3106's control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

McASP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec is clocked via a 24.576 Mhz oscillator. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the OMAP-L137 EVM.

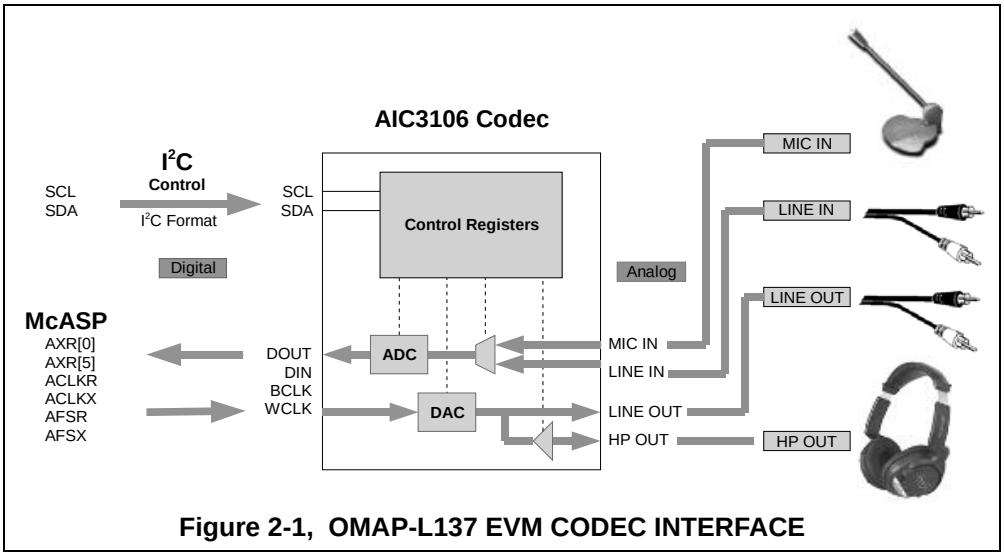

Figure 2-1, OMAP-L137 EVM CODEC INTERFACE

2.3 Ethernet Interface

The OMAP-L137 incorporates an ethernet MAC which interfaces to a Micrel KSZ8893MQL ethernet switch. The multi-port 10/100 Mbit interface is isolated and brought out to two RJ-45 standard ethernet connectors, P9, P10. The ethernet addresses is stored in the on board I^2C EEPROM. The 2 ethernet addresses stored in the EEPROM are the first address and the address + 1. The first address should always be an even number. The I^2C bus is also used to control configuration registers in the switch that are not accessible via the MDIO module.

Two ports provide the ability to input and pass data for Voice Over IP (VOIP) or other daisy chained applications. Connector P9 is the primary port for normal operation.

The RJ-45 jacks have 2 LEDs integrated into their connector. The LEDs are green and yellow and provide link and transmit status from the ethernet controller.

The MAC address for each EVM is also written on a label on the bottom of the board. The figure below shows an examples of this.

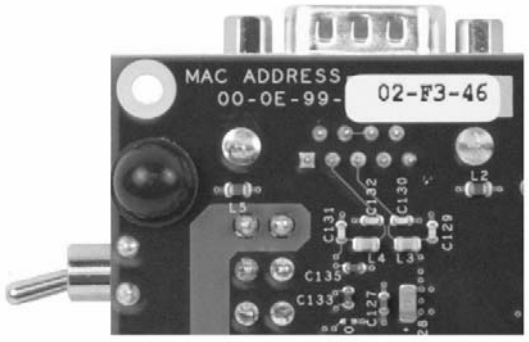

Figure 2-2, OMAP-L137 MAC Address

2.4 I²C0 Interface

The I²C0 bus on the OMAP-L137 is ideal for interfacing to the control registers of many devices. On the OMAP-L137 EVM the I²C0 bus is used to configure the ethernet phy and Codec. An I²C ROM is also interfaced via the serial bus. The format of the bus is shown in the figure below.

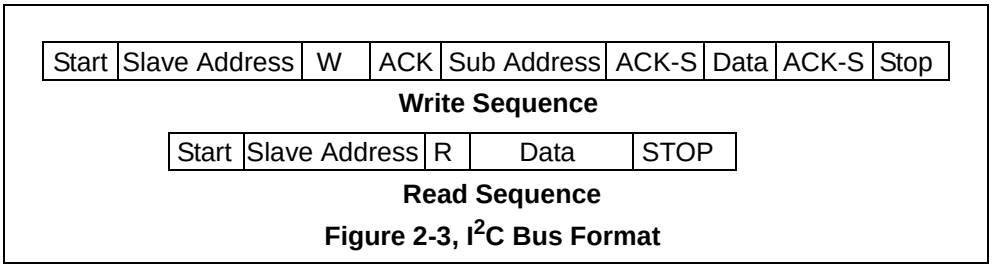

Figure 2-3, I²C Bus Format

The addresses of the on board peripherals are shown in the table below.

Table 1: I²C0 Memory Map

Device	Address	R/W	Function
KSZ8893MQL	0x5D	R/W	Ethernet Switch
TLV320AIC3106	0x1B	R/W	CODEC
I²C EEPROM	0x25	R/W	I²C EEPROM

2.5 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are interfaces which include McASP, and serial I/O expansion. The EMIF-A signals are brought out as LCD, peripheral, or EMIF signals.

The daughter card connectors used on the EVM are shown in the table below.

Table 2: Daughter Card Connectors

Reference Designator	Part Numbers Used On EVM	Manufacturer
P11	QSE-040-01-L-D-A-K	Samtec
P12	QSE-020-01-L-D-A-K	Samtec
P13	QSE-040-01-L-D-A-K	Samtec

One of the compatible mating daughter card connectors used to interface to the EVM are shown in the table below (other heights are available).

Table 3: Mating Daughter Card Connectors

Reference Designator	Part Numbers Used On EVM	Manufacturer
XP11	QTE-040-02-L-D-A-K	Samtec
XP12	QTE-020-02-L-D-A-K	Samtec
XP13	QTE-040-02-L-D-A-K	Samtec

Chapter 3

Physical Description

This chapter describes the physical layout of the OMAP-L137 EVM and its interfaces.

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3.1 Board Layout

The OMAP-L137 EVM is a 5.0 x 8.55 inch (127 x 217 mm.) ten (10) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the top side of the OMAP-L137 EVM.

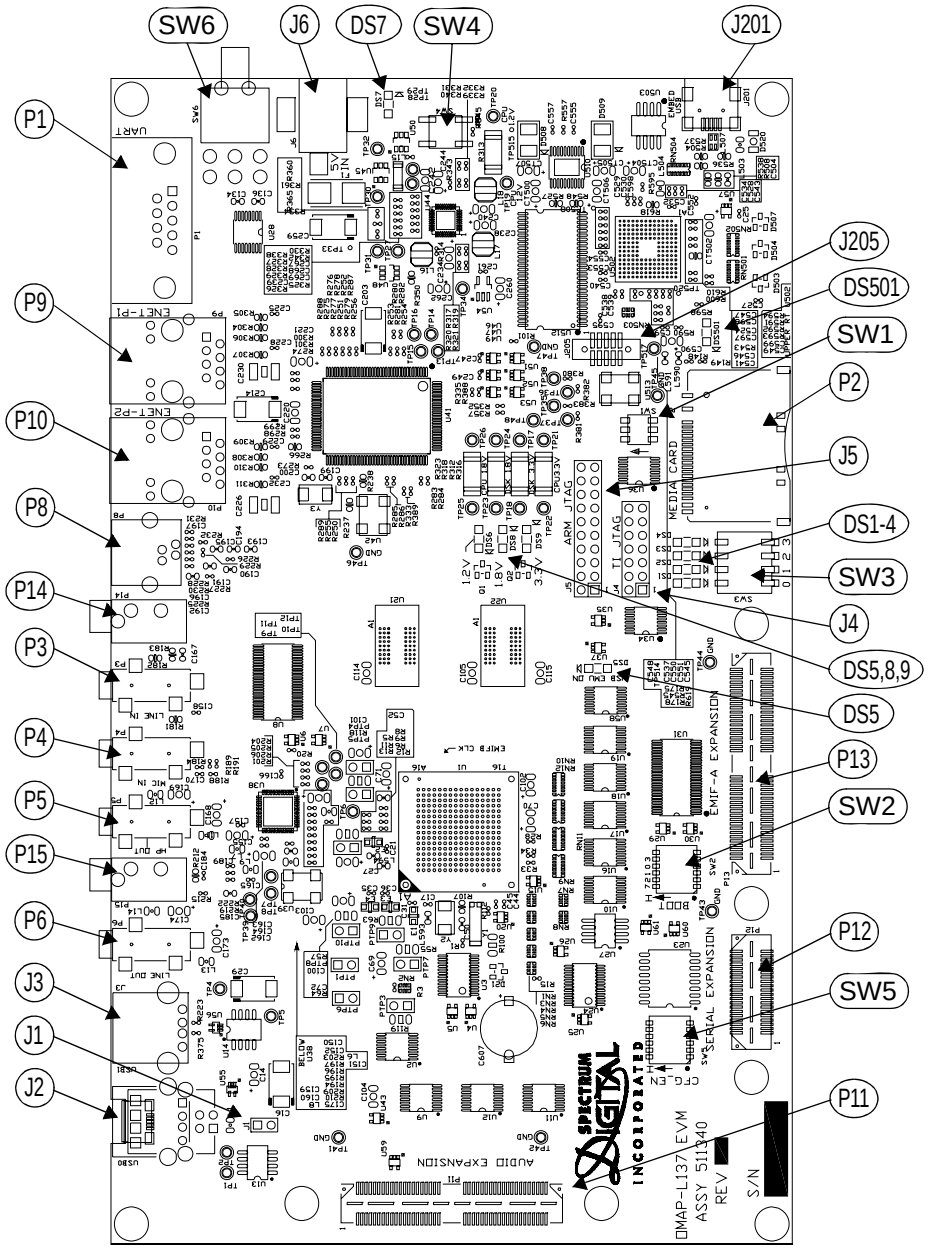


Figure 3-1, OMAP-L137 EVM, Interfaces Top Side

3.2 Connectors

The EVM has numerous connectors and option jumpers to control and provide connections to various peripherals. These connectors and jumpers are described in the following sections.

Table 1: Connectors

Connector	Size	Function
J1	1 x 2	USB Capacitance Select
J2	2	USB Interface
J3	6	USB Interface
J4	2 x 7	TI 14 Pin JTAG
J5	2 x 8	ARM JTAG Emulation Header
J6	2	+5V In
P1	9	RS-232 UART
P2	28	SD/MMC Connector
P3	4	Line In
P4	4	Microphone In
P5	4	Headphone Out
P6	4	Line Out
P8	4	RJ9 Connector
P9	12	Ethernet
P10	12	Ethernet
P11	2 x 45	Audio Expansion Connector
P12	2 x 22	Expansion 2
P13	2 x 45	Expansion 3
P14	3	Phono Jack
P15	3	Phono Jack
J201		Embedded JTAG Interface
J205	2 x 5	Not populated, factory use only

3.2.1 J1, USB Capacitance Select

Connector J1 is a jumper is used to provide more capacitance when the USB connector is used in the host mode. When the jumper is shorted the extra capacitance is provided. These open and shorted position are shown below.

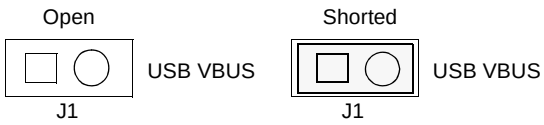


Figure 3-2, J1, USB Capacitance Select

Table 2: J1, USB Capacitance Select

Position	Function
Open	6.8 uF Capacitance
Shorted	106.8 uF Capacitance

3.2.2 J2, USB 2.0 Connector and Jumpers

Connector J2 is a micro A/B USB connector. The pinout for the J2 connector is shown in the table below.

Table 3: J2, USB Connector

Pins	Signal
1	USB_VBUS
2	USB_DM
3	USB_DP
4	USB_ID
5-9	USB_SHIELD

* Use internal register to swap DM/DP pair. This feature was used to improve printed circuit board routing.

The EVM supplies up to 500 ma of current to the USB_VBUS via a TPS2065. This is enabled via the OMAP-L137's DRV_VBUS pin. J1 supplies extra capacitance for host mode operations. Remove J1 for "USB On The Go" operations.

3.2.3 J3, USB 1.1 Connector

Connector J3 is a USB-A connector. This connector is connected directly to the OMAP L137 processor. A TPS2065 switches on host power via the L137 GPIO[15]. The pinout for the J3 connector is shown in the table below.

Table 4: J3, USB Connector

Pins	Signal
1	VBUS
2	D-, USB1_DM
3	D+, USB1_DP
4	GND, Ground
5	USB_Shield
6	USB_Shield

3.2.4 J4, 14 Pin External JTAG Connector

Connector J4 is a 2 x 7 double row male header. This is the standard interface used by JTAG emulators to interface to Texas Instruments DSPs. The pinout for the connector is shown in the figure below.

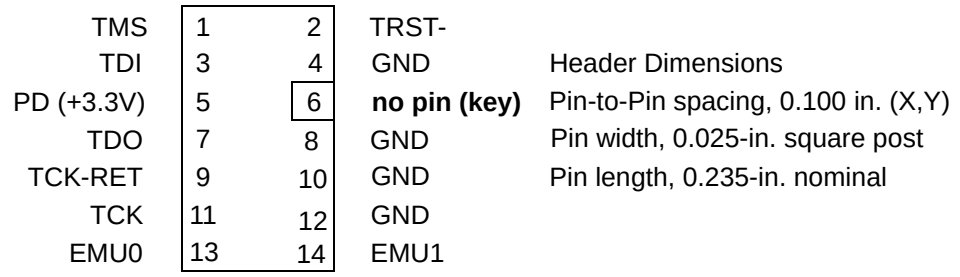


Figure 3-3, 14 Pin External JTAG Connector

3.2.5 J5, ARM JTAG Emulation Header

The J5 emulation header is located on the top side of the board and is used to provide an interface to ARM compatible JTAG emulators. The pinout for this connector is shown in the table below.

Table 5: J5, ARM JTAG Emulation Header

Pin #	Signal	Pin #	Signal
1	VCC_3V3	2	VCC_3V3
3	ARM_TRSTn	4	Ground
5	ARM_TDI	6	Ground
7	ARM_TMS	8	Ground
9	ARM_TCK	10	Ground
11	ARM_TCKRET	12	Ground
13	ARM_TDO	14	Ground
15	ARM_RSTn	16	Ground
17	NC	18	Ground
19	NC	20	Ground

3.2.6 J6, +5V Input

Connector J6 is the input power connector. This connector brings in +5 volts to the EVM. This is a 2.5mm. jack. The inside of the jack is tied to through a fuse to VCC_5V. The other side is tied to ground and LED DS7. The figure below shows this connector as viewed from the card edge.

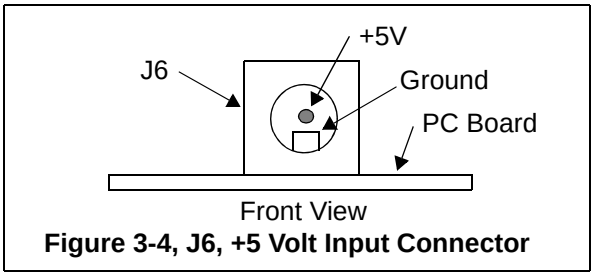


Figure 3-4, J6, +5 Volt Input Connector

3.2.7 P1, RS-232 UART

The P1 connector is a 9 pin male D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U28) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

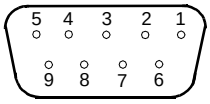


Figure 3-5, P1, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 6: P1, RS-232 Pinout

Pin #	Signal Name
1	NC
2	R_IN, Rx Data
3	T_OUT, Tx Data
4	NC
5	GND
6	NC
7	Pin 8
8	Pin 7
9	NC

3.2.8 P2, MMC/SD Connector

The P2 MMC/SD connector is located on the top side of the board and is used to provide an interface to the following interfaces: MMC+, SD, and MMC. The pinout for the P2 connector is shown in the table below.

Table 7: P2, MMC/SD Connector

Pin #	Signal
1	MMC_SD_DATA3 - #1_MMC+/MMC/SD
2	MMC_SD_CMD - #2_MMC+/MMC/SD
3	GND - #3_MMC+/MMC/SD
4	DSK_3V3 - #4_MMC+/MMC/SD
5	MMC_SD_CLK - #5_MMC+/MMC/SD
6	GND - #6_MMC+/MMC/SD
7	MMC_SD_DATA0 - #7_MMC+/MMC/SD
8	MMC_SD_DATA1 - #8_MMC+/SD
9	MMC_SD_DATA2 - #9_MMC+/SD
10	MMC_SD_DATA4 - #10_MMC+
11	MMC_SD_DATA5 - #11_MMC+
12	MMC_SD_DATA6 - #12_MMC+
13	MMC_SD_DATA7 - #13_MMC+/
14	MMC_SD_WP - SD_WP
15	MMC_SD_INS - CD
16	Reserved
17	Reserved
18	GND
19	DSK_3V3
20	Reserved
21	GND
22	Reserved
23	Reserved
24	Reserved
25	NC -
26	NC -
27	GND
28	GND

3.2.9 P3, Line In

Connector P3 is an stereo audio line input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

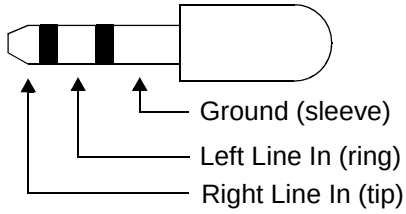


Figure 3-6, P3, Audio Line In Stereo Jack

Table 8: P3, Line In Interface

Pin #	AIC3106 Signal
1 (sleeve)	GND_AC
2 (ring)	LINE1L+
3 (tip)	LINE1R+
4 (sleeve)	GND_AC

3.2.10 P4, Microphone In

Connector P4 is an stereo microphone line input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

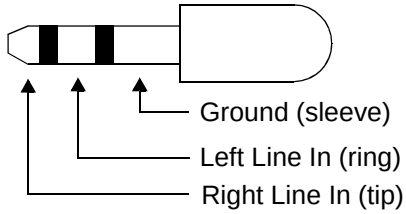


Figure 3-7, P4, Microphone In Stereo Jack

Table 9: P4, Microphone In Interface

Pin #	AIC3106 Signal
1 (sleeve)	GND_AC
2 (ring)	MIC3L/MIC3R
3 (tip)	MIC3L/MIC3R
4 (sleeve)	GND_AC

3.2.11 P5, Headphone Out

The P5 connector is a 3.5 mm. stereo headphone output from the TVL320AIC3106 on the EVM. The signals on the mating plug are shown in the figure below The signals present on this connector are defined in the following table.

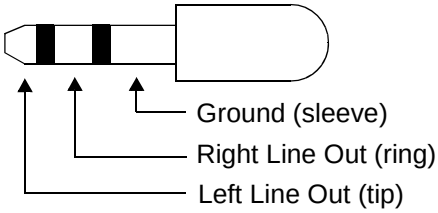


Figure 3-8, P5, Headphone Out Stereo Jack

Table 10: P5, Headphone Out Interface

Pin #	AIC3106 Signal
1(sleeve)	GND_AC
2(ring	HPLOUT
3(tip)	HPROUT
4	NC

3.2.12 P6, Line Out

The audio line out connector P6, is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

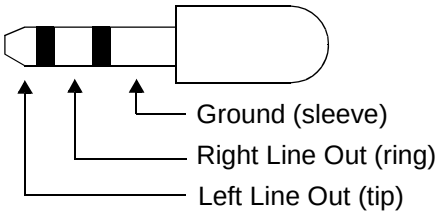


Figure 3-9, P6, Audio Line Out Stereo Jack

Table 11: P6, Audio Line Out Stereo Jack

Pin #	AIC33 Signal
1 (sleeve)	GND_AC
2 (ring)	LEFT_LO+
3 (tip)	RIGHT_LO+
4 (sleeve)	NC

3.2.13 P8, RJ9 Connector

The headset interface, P8, is a standard RJ9-4 connector which is not populated as shipped.

3.2.14 P9, Ethernet Interface

The P9 connector is located on the top side of the board and is used to provide an Ethernet interface. P9 integrates the magnetics and standard RJ-45 connector. The two tables below show the signals present on the magnetics interface and the connector side.

Table 12: P9, Magnetics/LEDs Interface Signals

Pin #	Signal	Pin #	Signal
1	TXP1 (TXD+)	2	TXM1 (TXD-)
3	RXP1 (RXD+)	4	ENET_VDDATR (TXD-CT)
5	ENET_VDDATR (RXD-CT)	6	RXM1 (RXD-)
7	NC1	8	GND
9	VCC_3V3(LED1+)	10	P1LED2(LED1-)
11	DSK_3V3(LED2+)	12	P1LED3(LED2-)

The ethernet connector incorporates 2 LEDs which give link and transmit status from the ethernet controller.

Table 13: P9, RJ-45 Connector

Pin #	Signal	Pin #	Signal
1	TX_DATA+	2	TX_DATA-
3	RX_DATA+	4	NC
5	NC	6	RX_DATA-
7	NC	8	NC

3.2.15 P10, Ethernet Interface

The P10 connector is located on the top side of the board and is used to provide an Ethernet interface. P10 integrates the magnetics and standard RJ-45 connector. The two tables below show the signals present on the magnetics interface and the connector side.

Table 14: P10, Magnetics/LEDs Interface Signals

Pin #	Signal	Pin #	Signal
1	TXP2 (TXD+)	2	TXM2 (TXD-)
3	RXP2 (RXD+)	4	ENET_VDDATR (TXD-CT)
5	ENET_VDDATR (RXD-CT)	6	RXM2 (RXD-)
7	NC1	8	GND
9	VCC_3V3(LED1+)	10	P2LED2(LED1-)
11	DSK_3V3(LED2+)	12	P2LED3(LED2-)

The ethernet connector incorporates 2 LEDs which give link and transmit status from the ethernet controller.

Table 15: P10, RJ-45 Connector

Pin #	Signal	Pin #	Signal
1	TX_DATA+	2	TX_DATA-
3	RX_DATA+	4	NC
5	NC	6	RX_DATA-
7	NC	8	NC

3.2.16 Expansion Connector Overview

The EVM has three expansion connectors which allow the user to interface to other logic which is unique to his application

Some of the signals on the EVM are multiplexed with an on board resource or they have multiple options on the L137 device. To enable these signals there are several control lines on the expansion connector. Pulling the control lines high enables the functions marked in the Mux_Ctl column tables. The number in the Mux_Ctl column indicates which pins it controls. An ‘N’ in front of the column indicates the pin is available when the control line is not pulled high. Each control line is pulled down on the EVM, therefore a pull-up resistor of approximately 500 ohms is required to enable the control line to a logic ‘1’. A ‘*’ in the Mux_Ctl column indicates this is a control line on the expansion connectors.

The next 3 tables indicate the interface signal and the appropriate control line on the pins of the expansion connectors.

3.2.16.1 P11, Audio / Expansion Connector

Table 16: P11, Audio / Expansion Connector

Pin	Signal	Mux_Ctl	Pin	Signal	Mux_Ctl
2	VCC_5V		1	VCC_5V	
4	VCC_5V		3	VCC_5V	
6	NC		5	I2C0_SDA	
8	SEL_ENETn_MCASP0	* 1	7	I2C0_SCL	
10	T_AMUTE0		9	EXP_ACHLKR0	1
12	Ground		11	Ground	
14	EXP1_AFSX0		13	T_AFSR0	
16	Ground		15	Ground	
18	T_ACLKX0		17	T_ACLKR0	
20	Ground		19	Ground	
22	EXP_AXR0[0]	1	21	EXP_AXR[8]	1
24	EXP_AXR0[1]	1	23	EXP_AXR0_9	N7
26	EXP_AXR0[2]	1	25	EXP_AXR0_10	N7
28	EXP_AXR0[3]	1	27	EXP1_AXR0_12	N11
30	EXP_AXR0[4]	1	29	EXP1_AXR0_13	N11
32	EXP_AXR0[5]	1	31	EXP1_AXR0_14	N11
34	EXP_AXR0[6]	1	33	EXP1_AXR0_15	N11
36	EXP_AXR0[7]	1	35	T_AXR0_11/AXR2_0/GPIO3_11	
38	Ground		37	Ground	
40	AHCLKR2		39	EXP1_AMUTE2_8	N12
42	EXP1_SPI1_SCSn	3	41	EXP1_SPI1_ENAn	3
44	EXP1_SPI1_CLK		43	EXP1_SPI1_SIMO	
46	EXP_RESETn		45	EXP1_SPI1_SOMI	
48	Ground		47	Ground	
50	T_AMUTE1		49	EXP_AHCLKX1	2
52	Ground		51	Ground	
54	EXP_AFSX1	2	53	T_AFSR1	
56	Ground		55	Ground	
58	EXP_ACLKX1	2	57	T_ACLKR1	
60	Ground		59	Ground	
62	EXP_AXR1[0]	2	61	T_AXR1[6]	
64	EXP_AXR1[1]		63	T_AXR1[7]	
66	EXP_AXR1[2]		65	T_AXR1[8]	
68	EXP_AXR1[3]	N5	67	T_AXR1[9]	
70	EXP_AXR1[4]	N5	69	T_AXR1[10]	
72	EXP_AXR1[5]	2	71	T_AXR1[11]	
74	EXP1_SEL_MCASP1	* 2	73	SEL_SPI1_EXP1	* 3
76	NC		75	NC	
78	VCC_5V		77	VCC_5V	
80	VCC_5V		79	VCC_5V	
82	Ground		81	Ground	
84	Ground		83	Ground	
86	Ground		85	Ground	
88	Ground		87	Ground	
90	NC		89	NC	

* 1 Control line for Mux_Ctl 1 signals, * 2 Control line for Mux_Ctl 2 signals
* 3 Control line for Mux_Ctl 3 signals, * N5 is not control signal 5 (default)
* N7 is not control signal 7 (default), * N11 is not control signal 11 (default)
* N12 is not control signal 12 (default)

3.2.16.2 P12, Expansion 2 Connector

Table 17: P12, Expansion 2 Connector

Pin	Signal	Mux_Ctl	Pin	Signal	Mux_Ctl
2	VCC_5V		1	VCC_5V	
4	VCC_5V		3	VCC_5V	
6	Ground		5	Ground	
8	EXP_SPI1_SOMI	9	7	EXP2_SPI0_SOMI	6
10	EXP2_SPI1_SIMO	9	9	EXP2_SPI0_SOMO	6
12	EXP_SPI1_CLK	9	11	EXP2_SPI0_CLK	6
14	EXP2_SPI1_SCSn	4	13	EQEP0A	6
16	EXP2_SPI1_ENAn	4	15	EQEP0B	6
18	Ground		17	Ground	
20	SEL_SPI1_EXP2	* 4	19	IC20_SCL	
22	EXP_EQEP1A	5	21	IC20_SDA	
24	EXP_EQE1B	5	23	NC	
26	SEL_EXP2_QEP1	* 5	25	SEL_EXP2_QEP0	* 6
28	EXP2_UART1_RXD	7	27	EXP2_TMP640_OUT12	9
30	EXP2_UART1_TXD	7	29	EXP2_TMP640_IN12	9
32	Ground		31	Ground	
34	SEL_EXP2_UART1	* 7	33	SEL_SPI1_EXP2_B	* 8
36	EXP_RESETn		35	SEL_EXP2_TIMER	* 9
38	VCC_5V		37	VCC_5V	
40	VCC_5V		39	VCC_5V	
42	Ground		41	Ground	
44	Ground		43	Ground	

* 4 Control line for Mux_Ctl 4 signals
* 5 Control line for Mux_Ctl 5 signals
* 6 Control line for Mux_Ctl 6 signals
* 7 Control line for Mux_Ctl 7 signals
* 8 Control line for Mux_Ctl 8 signals
* 9 Control line for Mux_Ctl 9 signals

3.2.16.3 P13, Expansion 3 Connector

Table 18: P13, Expansion 3 Connector

Pin	Signal	Mux_Ctl	Pin	Signal	Mux_Ctl
2	VCC_5V		1	VCC_5V	
4	VCC_5V		3	VCC_5V	
6	EXP3_SEL_MEMD0_7	* 10	5	NC	
8	EXP3_SEL_MEM	* 11	7	EXP3_SEL_MEM_CTL	* 12
10	Ground		9	Ground	
12	EXP_EMIFA_D0	10	11	EXP_EMIFA_D1	10
14	EXP_EMIFA_D2	10	13	EXP_EMIFA_D3	10
16	EXP_EMIFA_D4	10	15	EXP_EMIFA_D5	10
18	EXP_EMIFA_D6	10	17	EXP_EMIFA_D7	10
20	Ground		19	Ground	
22	EXP_EMIFA_D8	13	21	EXP_EMIFA_D9	13
24	EXP_EMIFA_D10	13	23	EXP_EMIFA_D11	13
26	EXP_EMIFA_D12	14	25	EXP_EMIFA_D13	14
28	EXP_EMIFA_D14	14	27	EXP_EMIFA_D15	14
30	Ground		29	Ground	
32	EXP3_SEL_MEMD8_D11	* 13	31	EXP_EMIFA_WEn_DQM0	11
34	EXP3_SEL_MEMD12_D16	* 14	33	EXP_EMIFA_WEn_DQM1	11
36	Ground		35	Ground	
38	EXP3_EMIFA_CLK		37	EMIFA_SDCKE	
40	Ground		39	Ground	
42	Ground		41	Ground	
44	EXP3_EMIFA_OEn	11	43	EMIFA_CS4n	10
46	EXP3_EMIFA_WEn	11	45	EMIFA_CS5n	10
48	Ground		47	NC	
50	EMIFA_WAIT0		49	EMIFA_CS2n	
52	EMIFA_CS0n		51	EXP3_EMIFA_CS3n	12
54	NC		53	NC	
56	EMIFA_BA0		55	EMIFA_BA1	
58	EMIFA_A0		57	EXP_EMIFA_A1	10
60	EXP_EMIFA_A2	10	59	EMIFA_A4	
62	EMIFA_A3		61	EMIFA_A6	
64	EMIFA_A5		63	EMIFA_A8	
66	EMIFA_A7		65	EMIFA_A10	
68	EMIFA_A9		67	EMIFA_A12	
70	EMIFA_A11		69	NC	
72	Ground		71	Ground	
74	EXP_RESETn		73	NC	
76	NC		75	NC	
78	VCC_5V		77	VCC_5V	
80	VCC_5V		79	VCC_5V	
82	Ground		81	Ground	
84	Ground		83	Ground	
86	Ground		85	Ground	
88	Ground		87	Ground	
90	NC		89	NC	

* 10 Control line for Mux_Ctl 10 signals
* 11 Control line for Mux_Ctl 11 signals
* 12 Control line for Mux_Ctl 12 signals
* 13 Control line for Mux_Ctl 13 signals
* 14 Control line for Mux_Ctl 14 signals

3.2.17 P14, Phono Jack In

Connector P14 is a phono jack input. This connector is not populated as shipped.

3.2.18 P15, Phono Jack In

Connector P15 is a phono jack input. This connector is not populated as shipped.

3.2.21 J201, Embedded JTAG Emulation Interface

Connector J201 is a USB interface providing JTAG access to the processor. This allows the user to develop and debug using Code Composer Studio on a PC.

3.3 LEDs

The EVM has ten (10) LEDs which are located on the top side of the board. Information regarding the LEDs are shown in the table below.

Table 19: LEDs

LED #	Use	Color
DS1	User control, EMIFA D12	Green
DS2	User control, EMIFA D13	Green
DS3	User control, EMIFA D14	Green
DS4	User control, EMIFA D15	Green
DS5	USB-EMU ON/OFF	Green
DS6	VCC_1V2	Green
DS7	VCC_5V	Green
DS8	VCC_1V8	Green
DS9	VCC_3V3	Green
DS501	On board EMU status	Green

3.4 Switches

The EVM has six (6) switches. The function of these switches are shown in the table below.

Table 20: Switches

Switch	Function	Type
SW1	EMU0/EMU1 Control	4 Position DIP
SW2	Boot Mode Select	6 Position DIP
SW3	User Readable	4 Position DIP
SW4	RESET Switch	Push Button/Momentary
SW5	Pull Up Select	6 Position DIP
SW6	On/Off Power Switch	Toggle

3.4.1 SW1, EMU0/1 Select Switch

SW1 is a 2 position DIP switch providing 4 options in selecting the state of the EMU0 and EMU1 pins on the OMAP-L137 processor. This switch is not needed for the OMAP-L137 processor.

The default is to select pull ups on the EMU0 and EMU1.

3.4.2 SW2, Boot Mode Select Switch

Switch SW2 is a 6 position DIP switch. Only 5 of the positions are used. Note that only 5 combinations provide valid options. The boot mode options are described in the table below.

Table 21: SW2, Boot Mode Select DIP Switch

Position	Pins	Signal
1	1-12	BOOTMODE[7]
2	2-11	BOOTMODE[2]
3	3-10	BOOTMODE[1]
4	4-9	BOOTMODE[0]
5	5-8	BOOTMODE[3]
6	6-7	NC

The figure below shows the SW2 switch.

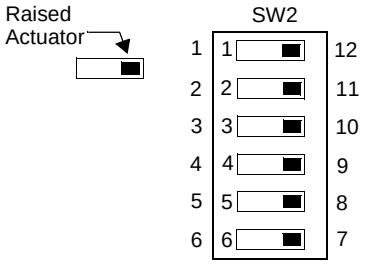


Figure 3-10, SW2, Boot Mode Select Switch

The table below shows the position settings which select the various boot modes.

Table 22: SW2, Boot Mode Select

Pos 1 Boot[7]	Pos 2 Boot[2]	Pos 3 Boot[1]	Pos 4 Boot[0]	Pos 5 Boot[3]	Boot Pin BTMODE[7,2,1,0,3]	Boot Mode
OFF	OFF	OFF	ON	NA	0 0 0 1 x	NOR
OFF	OFF	ON	OFF	NA	0 0 1 0 x	HPI
OFF	ON	OFF	ON	NA	0 1 0 1 x	SPI0 Flash
OFF	ON	ON	OFF	NA	0 1 1 0 x	SPI1 Flash
OFF	ON	ON	ON	NA	0 1 1 1 x	NAND 8-bit
OFF	OFF	OFF	OFF	OFF	0 0 0 0 0	I^2C0 Master
OFF	OFF	OFF	OFF	ON	0 0 0 0 1	I^2C0 Slave
OFF	OFF	ON	ON	OFF	0 0 1 1 0	I^2C1 Master
OFF	OFF	ON	ON	ON	0 0 1 1 1	I^2C1 Slave
OFF	ON	OFF	OFF	OFF	0 1 0 0 0	SPI0 EEPROM *****
OFF	ON	OFF	OFF	ON	0 1 0 0 1	SPI1 EEPROM
ON	OFF	OFF	ON	OFF	1 0 0 1 0	SPI0 Slave
ON	OFF	OFF	ON	ON	1 0 0 1 1	SPI1 Slave
ON	OFF	ON	ON	OFF	1 0 1 1 0	UART0
ON	OFF	ON	ON	ON	1 0 1 1 1	UART1
ON	OFF	ON	OFF	OFF	1 0 1 0 0	UART2 *****
ON	ON	ON	ON	OFF	1 1 1 1 0	Emulation Debug *****

***** Supported in standalone EVM

3.4.3 SW3, User Readable 4 Position DIP Switch

Switch SW6 is a 4 position DIP switch mapped to EMIFA data bus lines D8-D11 via a multiplexer. The table below shows what signal each position appears on.

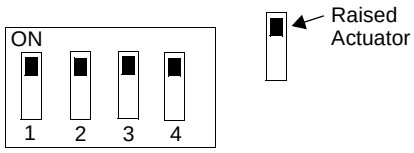


Figure 3-11, SW3, User Readable 4 Position DIP Switch

Table 23: SW3, User Readable 4 Position DIP Switch

Position	Signal
1	SW_DIP0, EMIFA - D8
2	SW_DIP1, EMIFA - D9
3	SW_DIP2, EMIFA - D10
4	SW_DIP3, EMIFA - D11

3.4.4 SW4, RESET Switch

Switch SW4 is a push button reset switch that will RESET the board.

3.4.5 SW5, Mux Control Switch

Switch SW5 is a 6 position DIP switch that allows mux control signals to be pulled up to +3.3 volts. This switch allows enabling on mux control signals. The six signals that can be pulled up are shown in the table below. Alternatively the multiplexer control lines can be enabled via daughter card connectors. Additional control lines are mapped to the daughter card connectors. Refer to the expansion connector sections 3.2.16.1 to 3.2.16.2 for more information.

Table 24: SW5, Pull-Up Switch

Position	Signal	Mux_Ctl
SW5-1	SEL_ENETn_MCASP0	* 1
SW5-2	SEL_EXP2_TIMER	* 9
SW5-3	SEL_EXP2_UART1	* 7
SW5-4	ON_BD_OFF_BD	U19 control for USB
SW5-5	EXP3_SEL_MEMD8-D11	* 13
SW5-6	EXP3_SEL_MEMD12-D15	* 14

The figure below shows the SW5 switch.

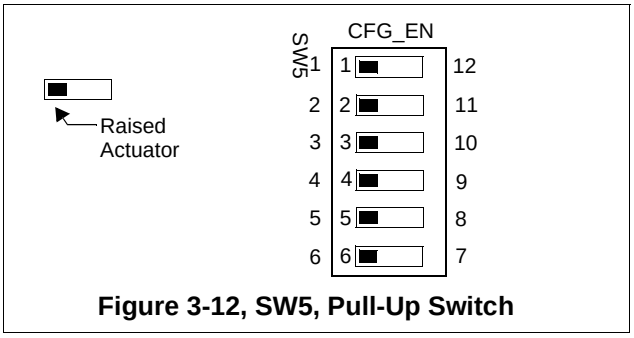


Figure 3-12, SW5, Pull-Up Switch

3.4.6 SW6, On/Off Switch

Switch SW6 is an on/off toggle switch that allows +5 volts from the J6 connector to be applied to the board.

3.5 Test Points

The EVM has 49 test points. All test points appear on the top of the board. The following figure identifies the position of each test point. The next table lists each test point and the signal appearing on that test point.

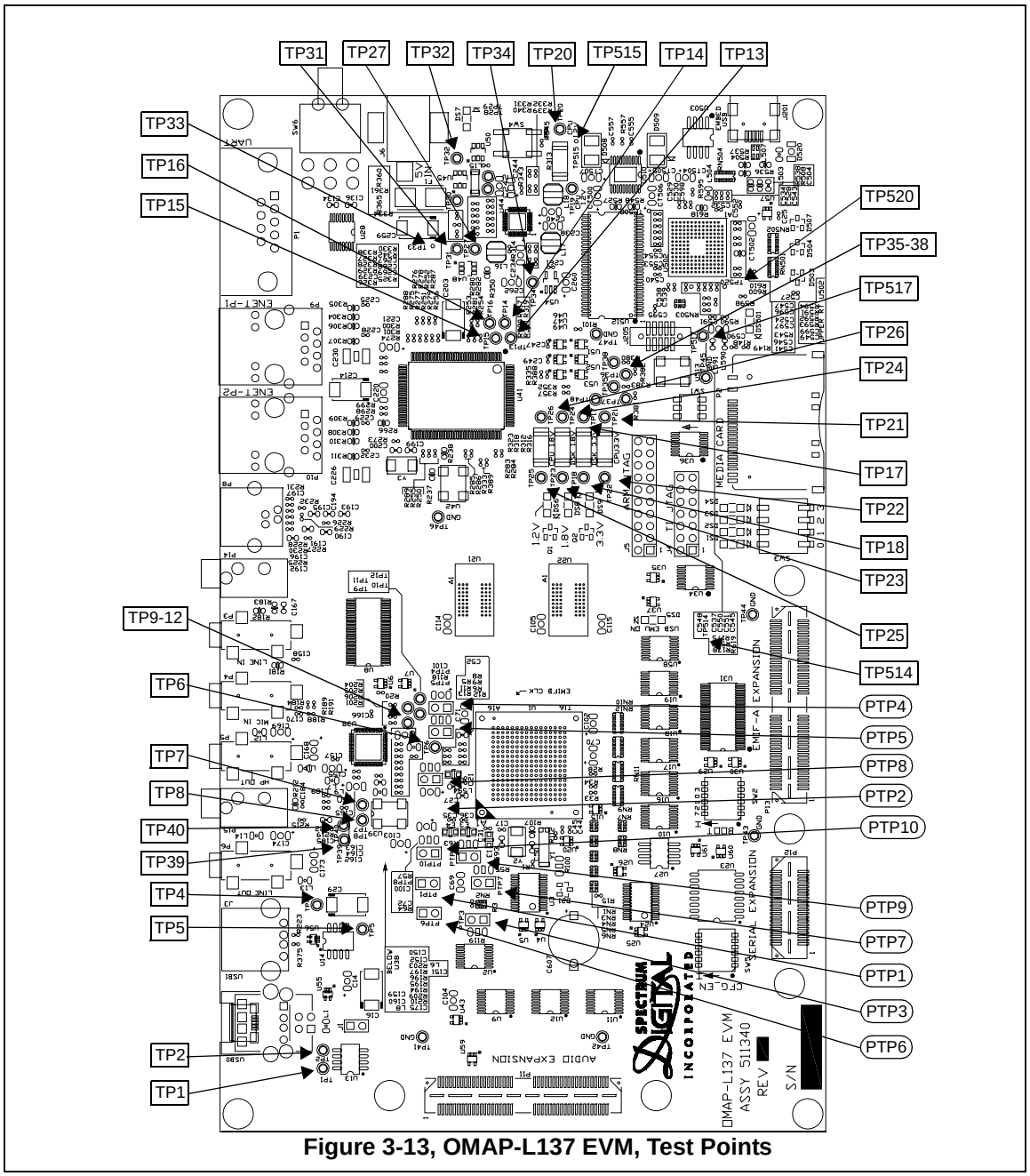


Figure 3-13, OMAP-L137 EVM, Test Points

Table 25: OMAP-L137 EVM Test Points

Test Point #	Signal	Test Point #	Signal
TP1	U13, Pin 6,7,8, VBUS From J2	TP16	U41, Pin 6, P2LED0
TP2	DSK_3V3, U13, Pin 5, OCn	TP27	U44, Pin 28, INTn
TP4	U14, Pin 6,7,8, VBUS from J3	TP28	U44, Pin 20, VLDO1
TP5	DSK_3V3, U14, Pin 5, OCn	TP29	U44, Pin 18, VLDO2
TP6	U1, F7, RSV1	TP33	VCC_5V
TP7	U38, Pin 35, GPIO1	TP34	U54, Pin 5, ALT_CPU_1V2
TP8	U38, Pin 35, GPIO2	TP35	USB1, TAIN0
TP9	U38, Pin 45, MFP0	TP36	USB1, TAIN1
TP10	U38, Pin 46, MFP1	TP37	USB1, TAIN2
TP11	U38, Pin 47, MFP2	TP38	USB1, TAIN3
TP12	U38, Pin 48, MFP3	TP39	U38, Pin 27, MONO_LO+
TP13	U41, Pin 2, P1LED1	TP40	U38, Pin 28, MONO_LO-
TP14	U41, Pin 3, P1LED0	TP515	Factory Use
TP15	U41, Pin 5, P2LED1	TP517	Factory Use
		TP520	Factory Use

There are 10 power test point pairs for major power domains on the EVM. These test points provide a convenient mechanism to check the EVM's multiple power supplies. The table below shows the voltages for each test point and what the supply is used for.

Table 26: Power Test Points

Access Test Points	Voltage	Shunt	Comments
TP17, TP18	DSK_3V3	0.025 ohms	All EVM 3.3V supplies except CPU
TP19, TP20	CPU_1V2	0.025 ohms	All CPU 1.2V supplies
TP21, TP22	CPU_3V3	0.025 ohms	All CPU 3.3V supplies
TP23, TP24	DSK_1V8	0.025 ohms	All EVM 1.8V supplies except CPU
TP25, TP26	CPU_1V8	0.025 ohms	All CPU 1.8V supplies

Furthermore the EVM has ten 2 pin power test points for specific power domains on the L137 device. These voltages are measured across a resistor which is why there are two points to each test position. The square pad is the ground. The round pad is the measured voltage. The figure below shows what a typical power test point looks like.

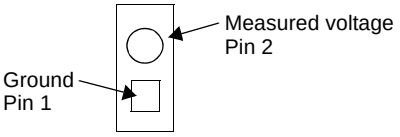


Figure 3-14, Power Test Point

The table below shows the power test points and the voltage measured.

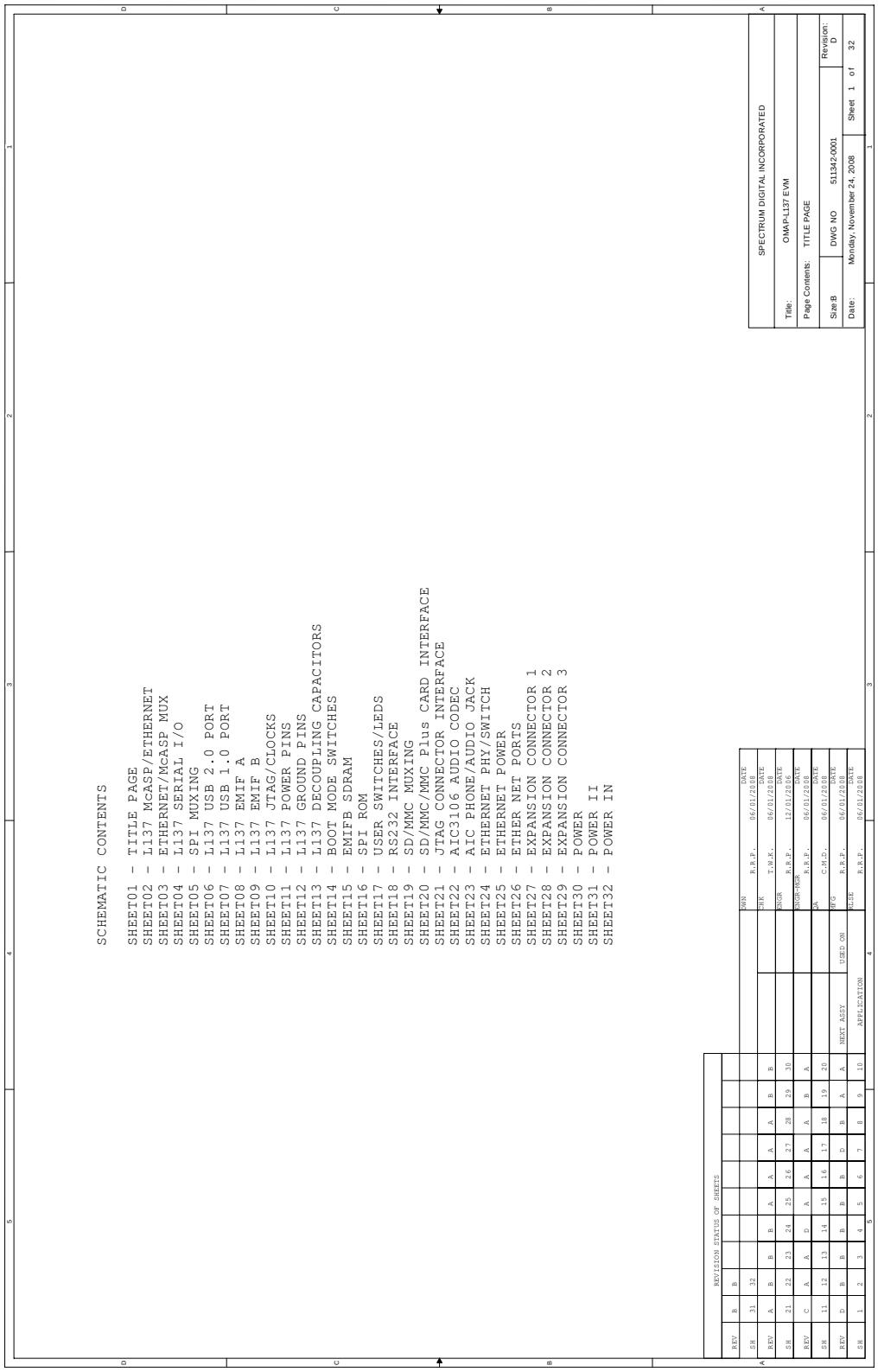
Table 27: Power Test Points

Power Test Point	Voltage Measured
PTP1	CPU_3V3
PTP2	CPU_1V2
PTP3	CPU_1V2
PTP4	CPU_1V2
PTP5	CPU_1V2
PTP6	CPU_1V2
PTP7	CPU_3V3
PTP8	CPU_1V8
PTP9	CPU_3V3
PTP10	CPU_1V8

Appendix A

Schematics

This appendix contains the schematics for the OMAP-L137 EVM.



SCHEMATIC CONTENTS

REVISION STATUS OF SHEETS

REV	B	B																													
SH	31	32																													
REV	A	B	B	B	A	A	A	A	B	B																					
SH	21	22	23	24	25	26	27	28	29	30																					
REV	C	A	A	D	A	A	A	A	B	A																					
SH	11	12	13	14	15	16	17	18	19	20																					
REV	D	B	B	B	B	B	D	B	A	A																					
SH	1	2	3	4	5	6	7	8	9	10																					

DWN	R.H.P.	06/01/2008	DATE
CHK	T.W.K.	06/01/2008	DATE
ENGR	R.H.P.	12/01/2006	DATE
ENGR-MGR	R.H.P.	06/01/2008	DATE
QA	C.M.D.	06/01/2008	DATE
APP'D	R.H.P.	06/01/2008	DATE
RELEASE	R.H.P.	06/01/2008	DATE

NEXT ASSY	USED ON	APPLICATION	

SPECTRUM DIGITAL INCORPORATED

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Page Contents: TITLE PAGE

Size:B | DWG NO 511342-0001 | Revision: D

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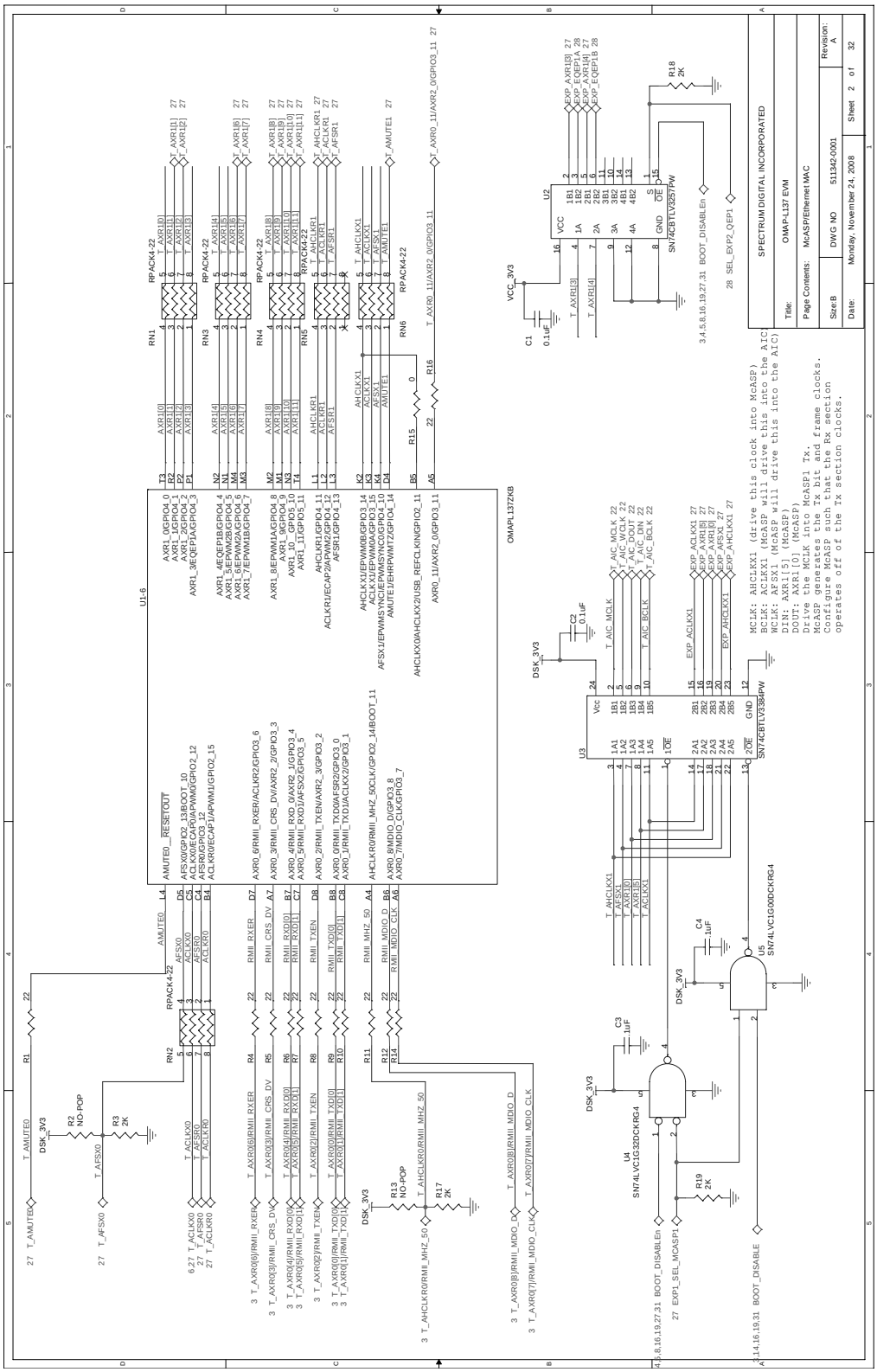
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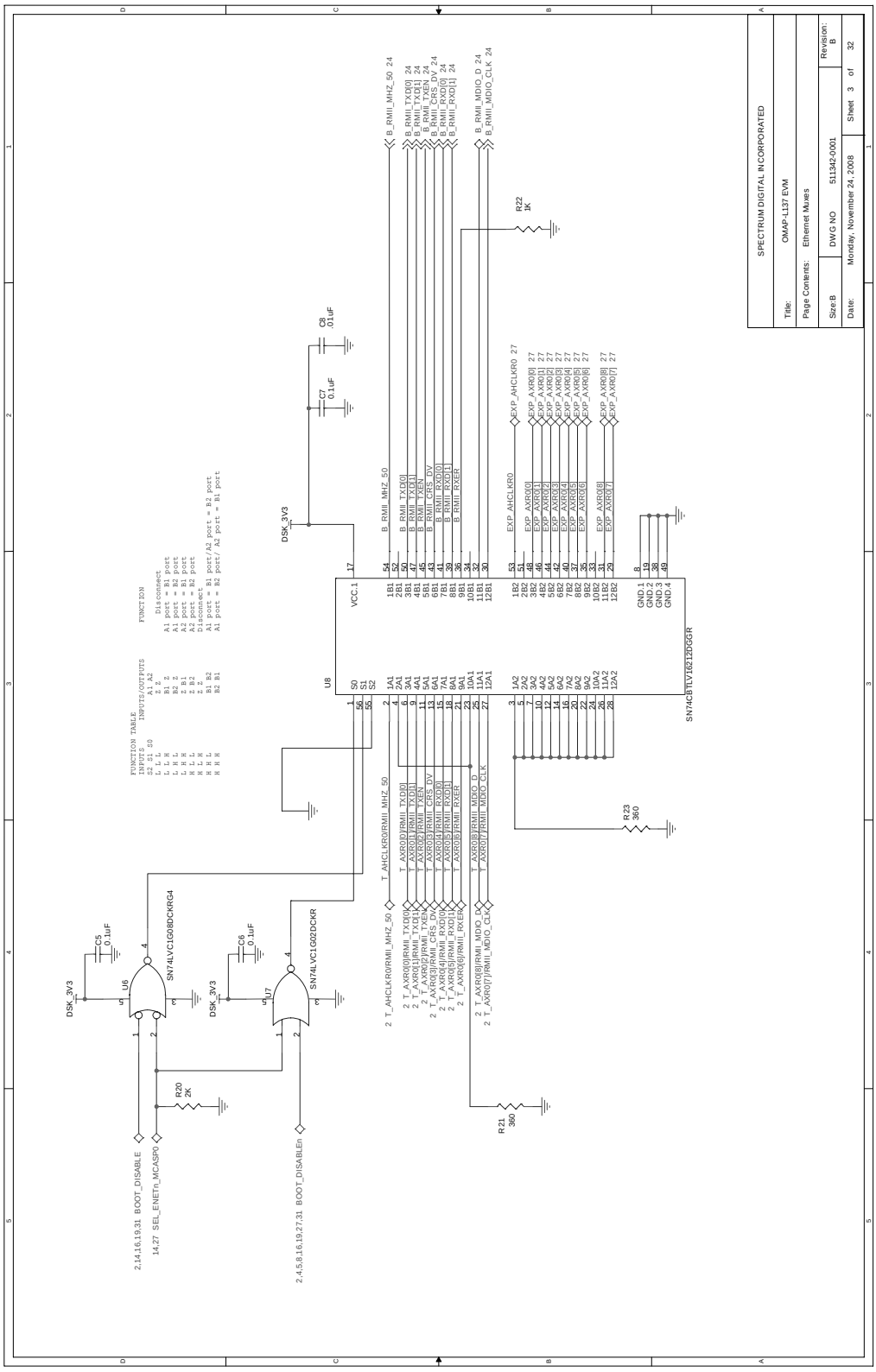
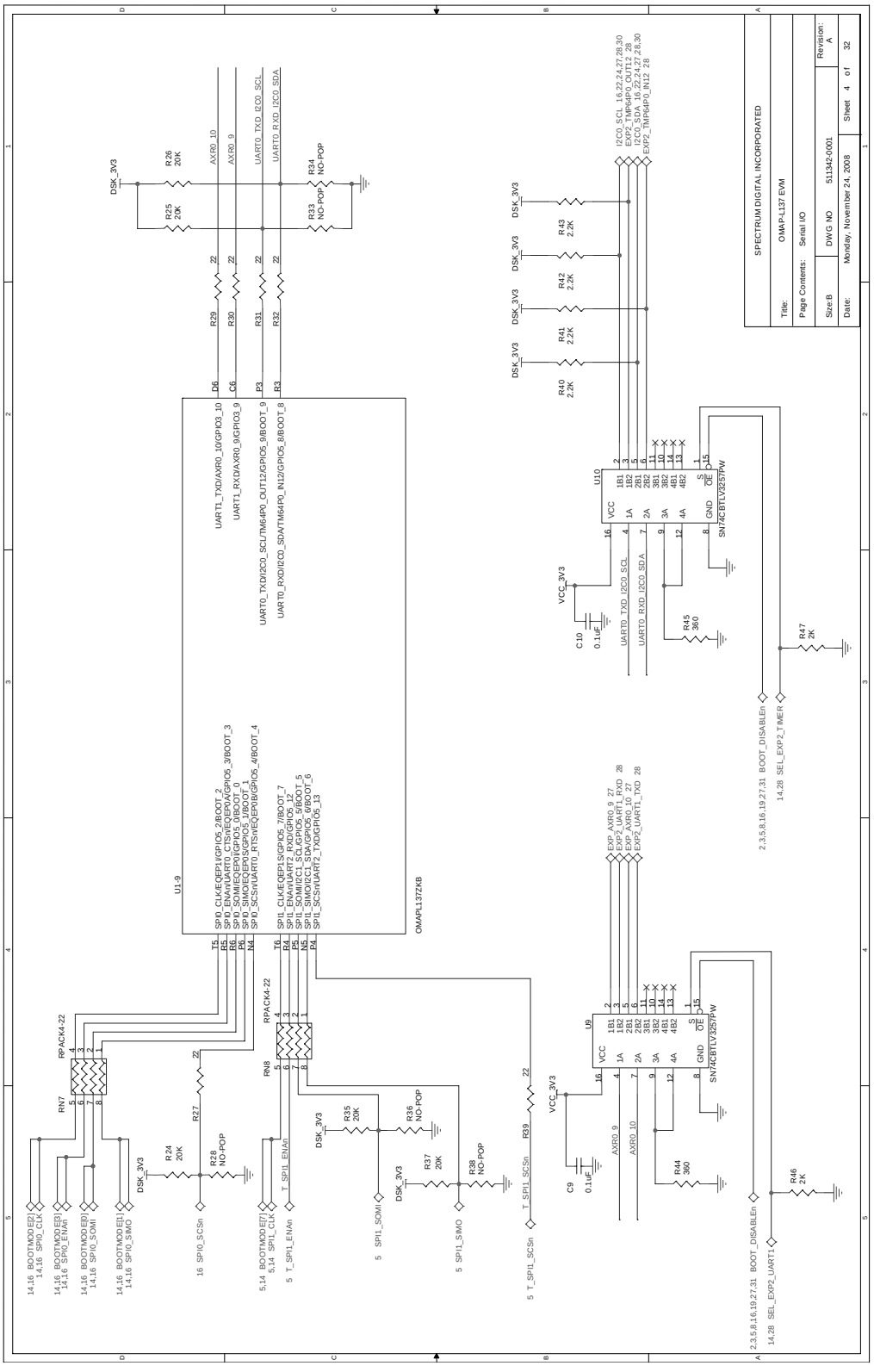
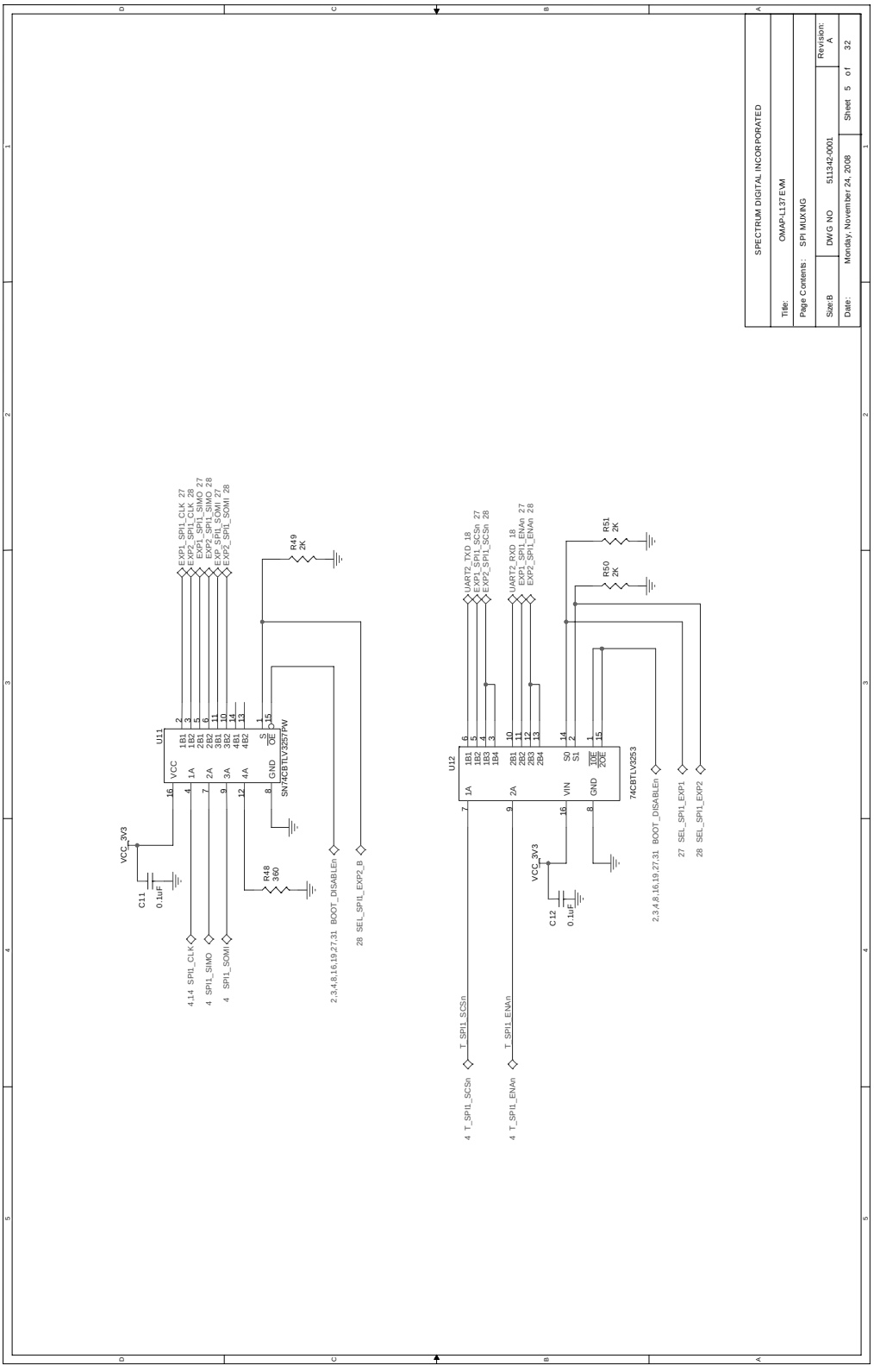
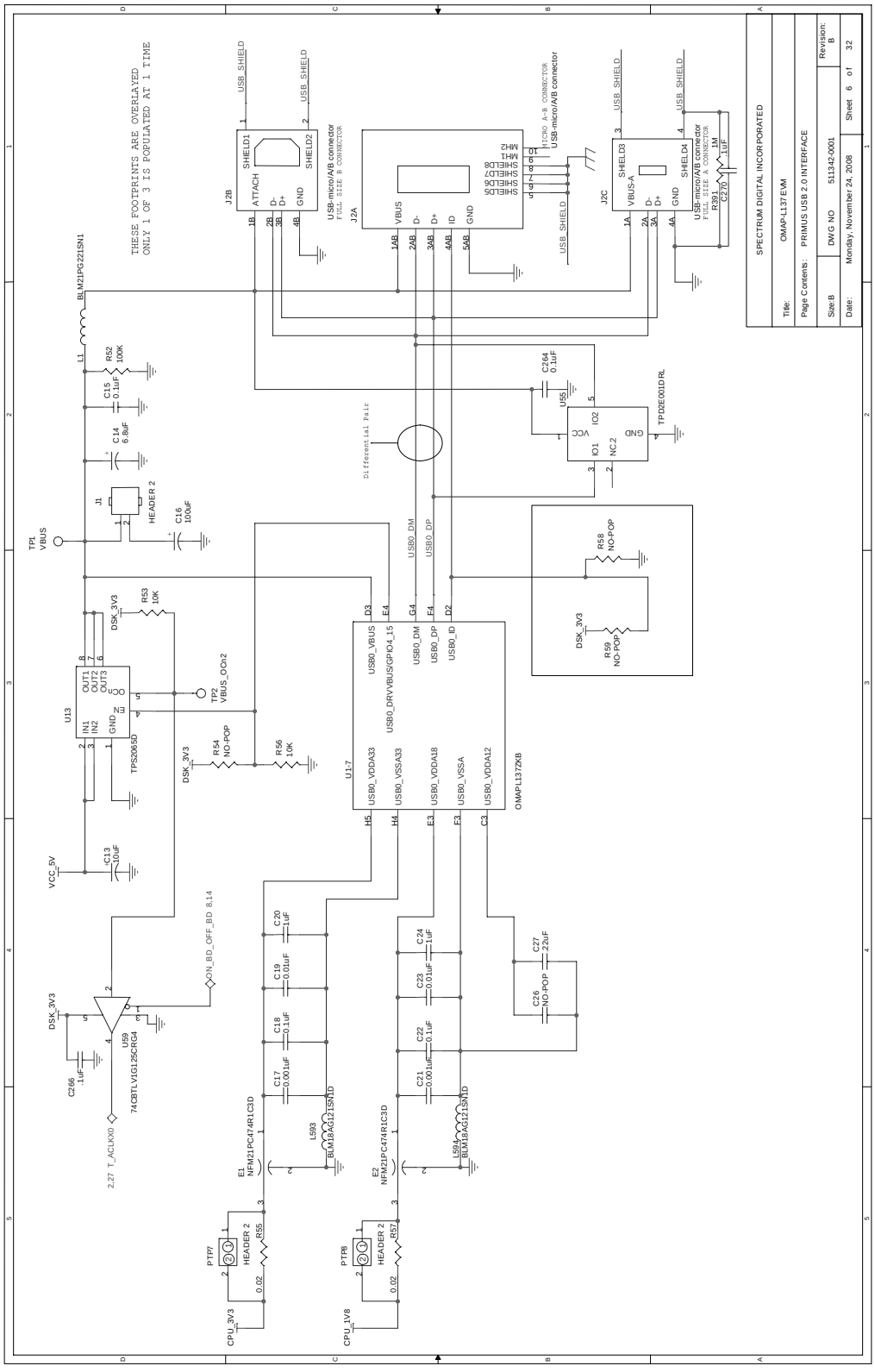
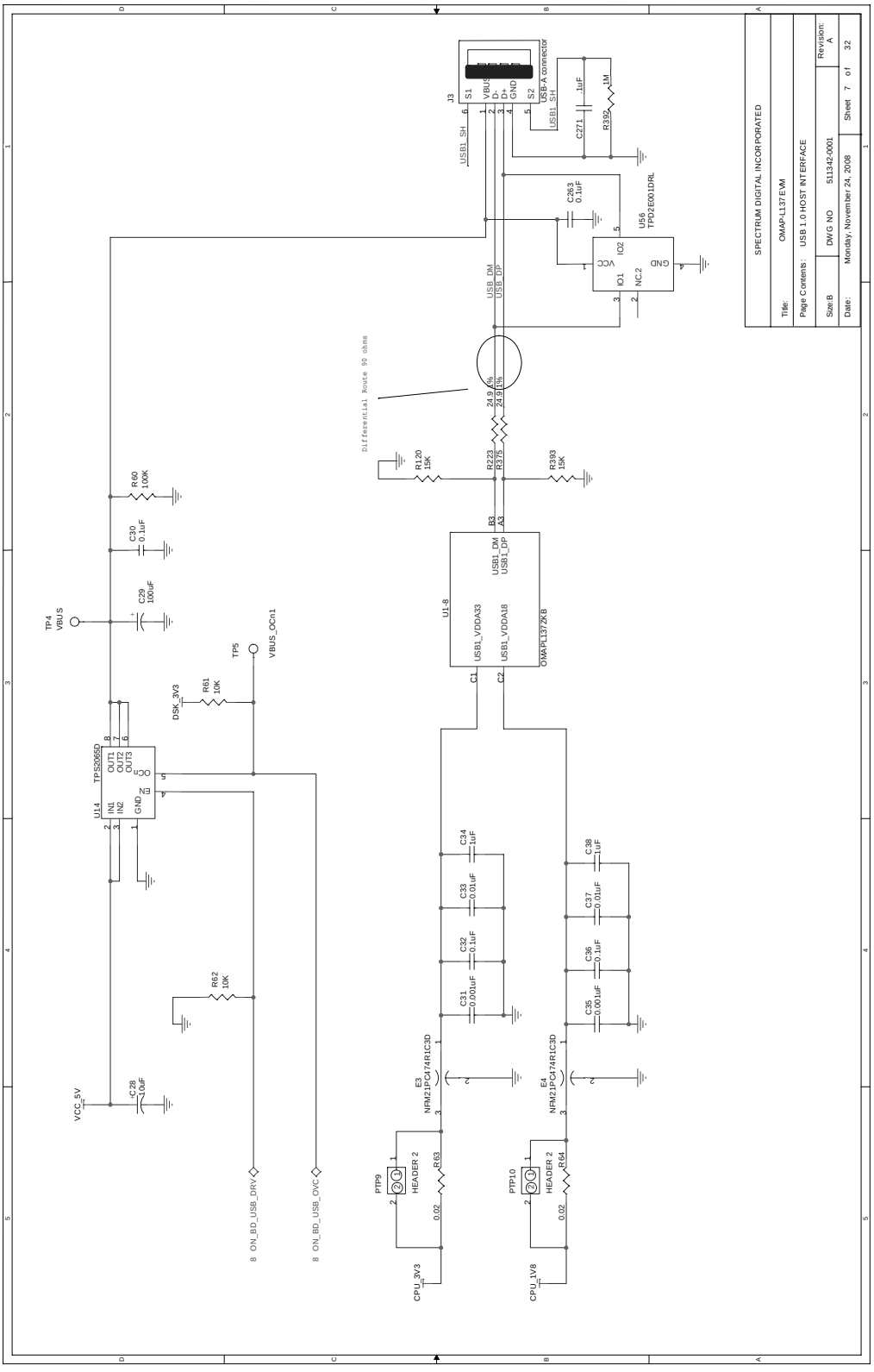
Page Contents: McASP/Ethernet MAC
Size:B DWG NO 511342-0001 Revision: A
Date: Monday, November 24, 2008 Sheet 2 of 32
MCLK: AHClkX1 (drive this clock into McASP)
BCLK: AClkX1 (McASP will drive this into the AIC)
MFSX: AFSX1 (McASP will drive this into the AIC)
DOUT: AXR1[0] (McASP)
Drive the MClK into McASP1 Tx.
McASP generates the Tx bit and frame clocks.
Configure McASP such that the Rx section
operates off of the Tx section clocks.
U1-6
OMAPL137ZKB
U2
SN74CBTLV3257PW
U3
SN74LVC1G00DCKRG4
U4
SN74LVC1G32DCKRG4
U5
SN74LVC1G00DCKRG4
RN1
RN2
RN3
RN4
RN5
RN6
RPACK4-22
VCC_3V3
DSK_3V3
BOOT_DISABLE
SEL_EXP2_QEP1
EXP1_SEL_MCASP1

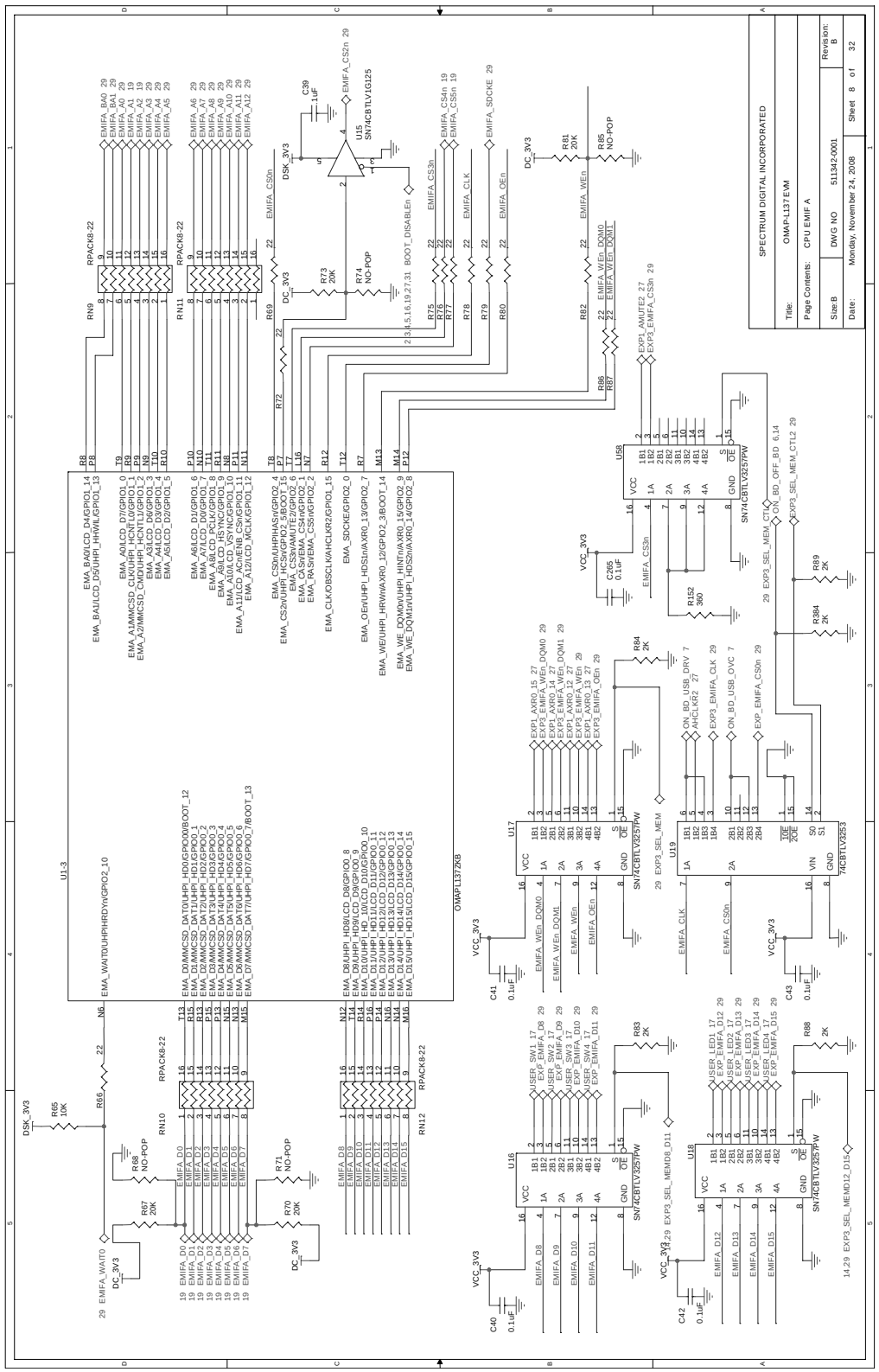

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: Ethernet Muxes
Size:B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 3 of 32
SN74CBTLV16212DGGR
SN74LVC1G08DCKRG4
SN74LVC1G02DCKR
B_RMII_MHZ_50
B_RMII_TXD[0]
B_RMII_TXD[1]
B_RMII_TXEN
B_RMII_CRS_DV
B_RMII_RXD[0]
B_RMII_RXD[1]
B_RMII_MDIO_D
B_RMII_MDIO_CLK
EXP_AHCLKR0
EXP_AXR0[0]
EXP_AXR0[1]
EXP_AXR0[2]
EXP_AXR0[3]
EXP_AXR0[4]
EXP_AXR0[5]
EXP_AXR0[6]
EXP_AXR0[8]
EXP_AXR0[7]
DSK_3V3
BOOT_DISABLE
SEL_ENETn_MCASP0
BOOT_DISABLEn
R20 2K
R21 360
R22 1K
R23 360
C5 0.1uF
C6 0.1uF
C7 0.1uF
C8 .01uF

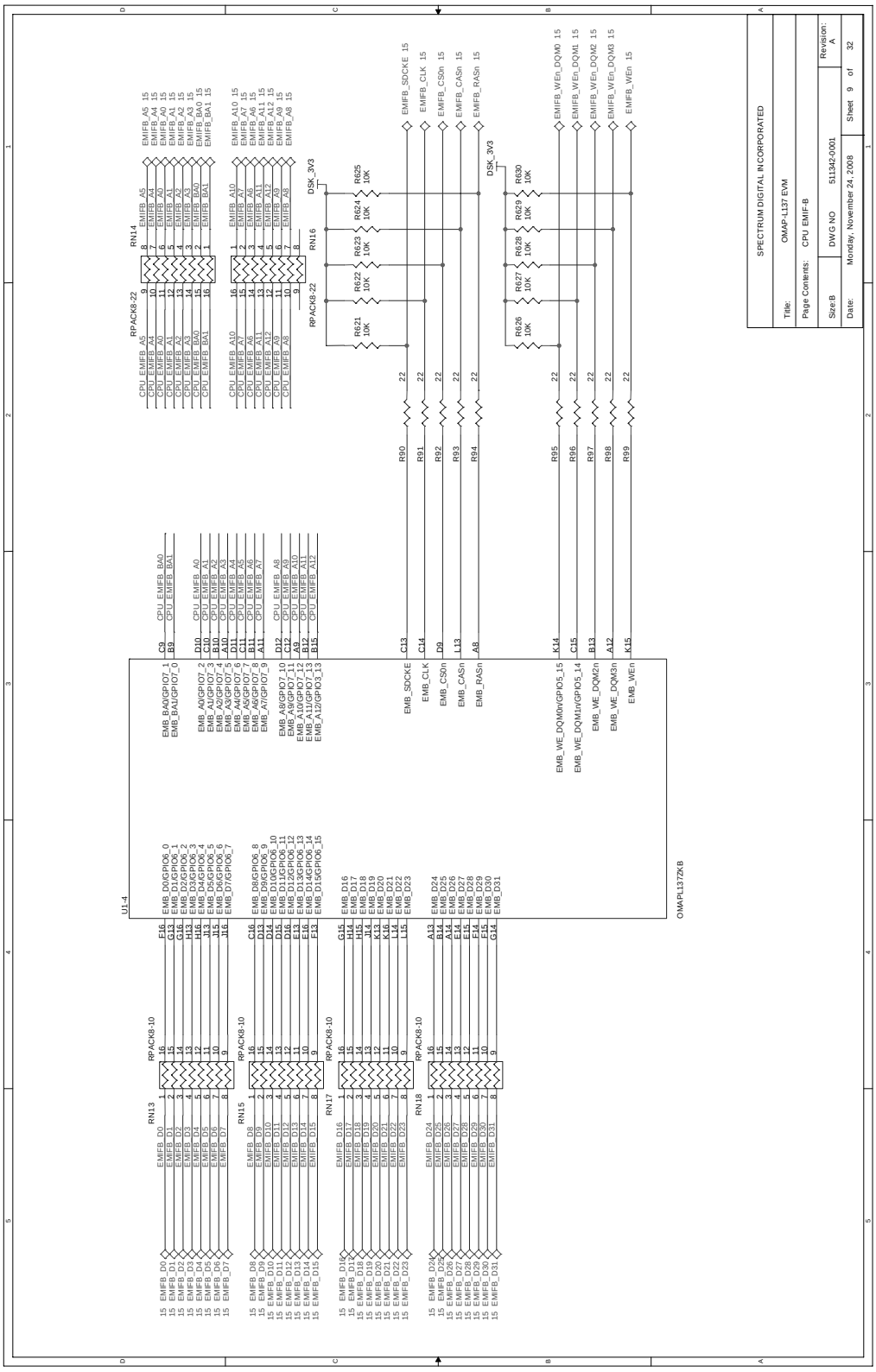

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: Serial I/O
Size:B DWG NO 511342-0001 Revision: A
Date: Monday, November 24, 2008 Sheet 4 of 32
U1-9
OMAPL1372KB
SPI0_CLK/EQEP1I/GPIO5_2/BOOT_2
SPI0_ENA/UART0_CTS/EQEP2I/AGPIO5_3/BOOT_3
SPI0_SOMI/EQEP0I/GPIO5_0/BOOT_0
SPI0_SIMO/EQEP0S/GPIO5_1/BOOT_1
SPI0_SCSn/UART0_RTS/nREQEP0B/GPIO5_4/BOOT_4
SPI1_CLK/EQEP1S/GPIO5_7/BOOT_7
SPI1_ENA/UART2_RXD/GPIO5_12
SPI1_SOMI/I2C1_SCL/AGPIO5_5/BOOT_5
SPI1_SIMO/I2C1_SDA/GPIO5_6/BOOT_6
SPI1_SCSn/UART2_TXD/GPIO5_13
UART1_TXD/AXR0_10/GPIO3_10
UART1_RXD/AXR0_9/GPIO3_9
UART0_TXD/I2C0_SCL/TM64P0_OUT12/GPIO5_9/BOOT_9
UART0_RXD/I2C0_SDA/TM64P0_IN12/GPIO5_8/BOOT_8
D6 C6 P3 R3
R29 R30 R31 R32 22
R25 20K
R26 20K
R33 NO-POP
R34 NO-POP
DSK_3V3
AXR0_10
AXR0_9
UART0_TXD I2C0_SCL
UART0_RXD I2C0_SDA
R40 2.2K
R41 2.2K
R42 2.2K
R43 2.2K
I2C0_SCL 16,22,24,27,28,30
EXP2_TMP64P0_OUT12 28,30
I2C0_SDA 16,22,24,27,28,30
EXP2_TMP64P0_IN12 28
U10
SN74CBTLV3257PW
VCC_3V3
C10 0.1uF
UART0_TXD I2C0_SCL
UART0_RXD I2C0_SDA
R45 360
R47 2K
2,3,5,8,16,19,27,31 BOOT_DISABLEn
14,28 SEL_EXP2_TIMER
RPACK4-22
RN7
RN8
R24 20K
R27 22
R28 NO-POP
R35 20K
R36 NO-POP
R37 20K
R38 NO-POP
R39 22
14,16 BOOTMODE[2] 14,16 SPI0_CLK
14,16 BOOTMODE[3] 14,16 SPI0_ENAn
14,16 BOOTMODE[0] 14,16 SPI0_SOMI
14,16 BOOTMODE[1] 14,16 SPI0_SIMO
16 SPI0_SCSn
5,14 BOOTMODE[7] 5,14 SPI1_CLK
5 T_SPI1_ENAn
5 SPI1_SOMI
5 SPI1_SIMO
5 T_SPI1_SCSn
U9
SN74CBTLV3257PW
VCC_3V3
C9 0.1uF
EXP_AXR0_9 27
EXP2_UART1_RXD 28
EXP_AXR0_10 27
EXP2_UART1_TXD 28
AXR0_9
AXR0_10
R44 360
R46 2K
2,3,5,8,16,19,27,31 BOOT_DISABLEn
14,28 SEL_EXP2_UART1

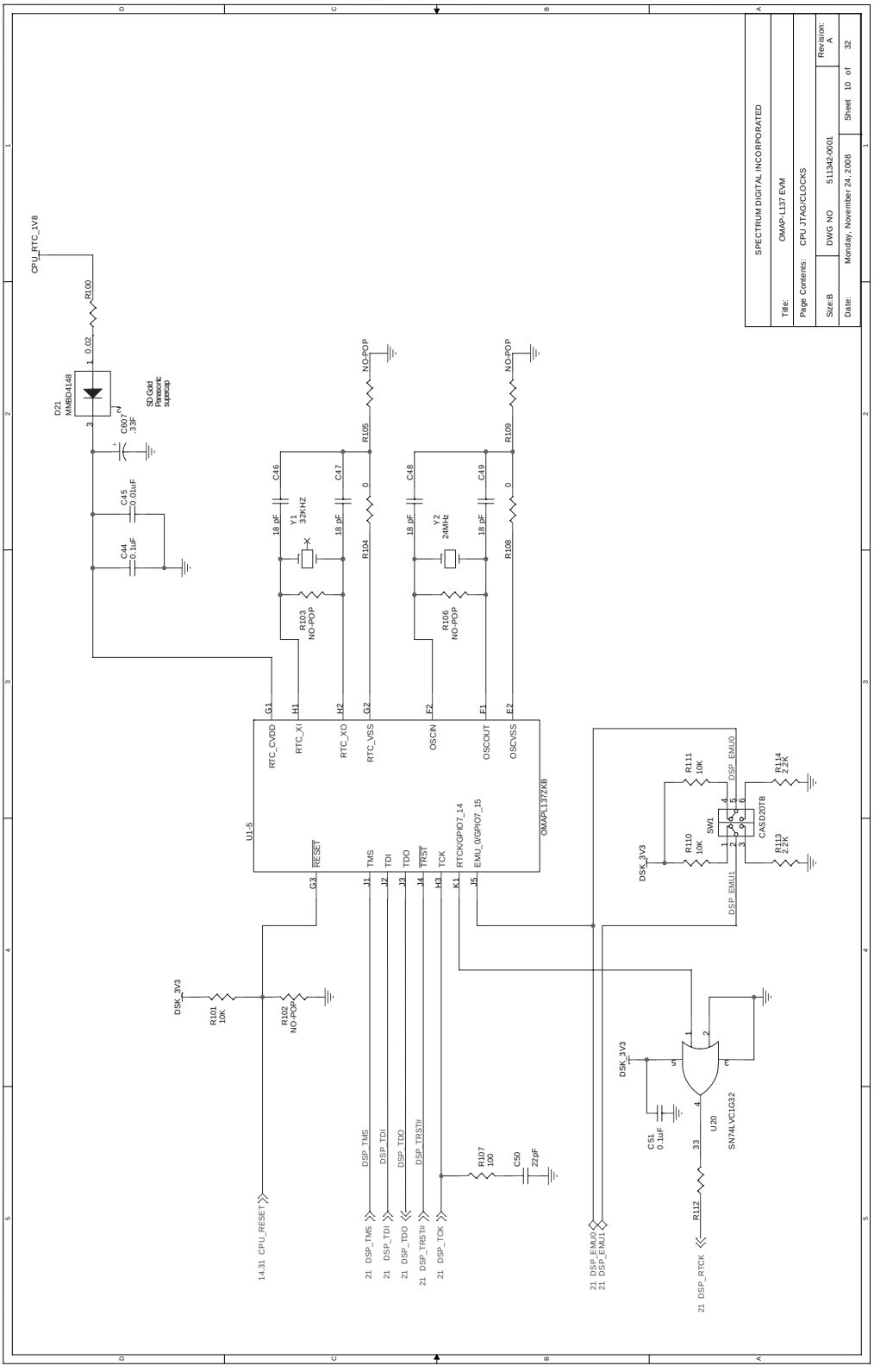

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: SPI MUXING
Size: B
DWG NO 5113-42-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 5 of 32
U11
SN74CBTLV3257PW
U12
74CBTLV3253
VCC_3V3
C11 0.1uF
C12 0.1uF
R48 360
R49 2K
R50 2K
R51 2K
EXP1_SPI1_CLK 27
EXP1_SPI1_SIMO 27
EXP1_SPI1_SOMI 27
EXP2_SPI1_CLK 28
EXP2_SPI1_SIMO 28
EXP2_SPI1_SOMI 28
UART2_TXD 18
UART2_RXD 18
EXP1_SPI1_SCSn 27
EXP2_SPI1_SCSn 28
EXP1_SPI1_ENAn 27
EXP2_SPI1_ENAn 28
BOOT_DISABLEn
SEL_SPI1_EXP1
SEL_SPI1_EXP2
T_SPI1_SCSn
T_SPI1_ENAn
SPI1_CLK
SPI1_SIMO
SPI1_SOMI

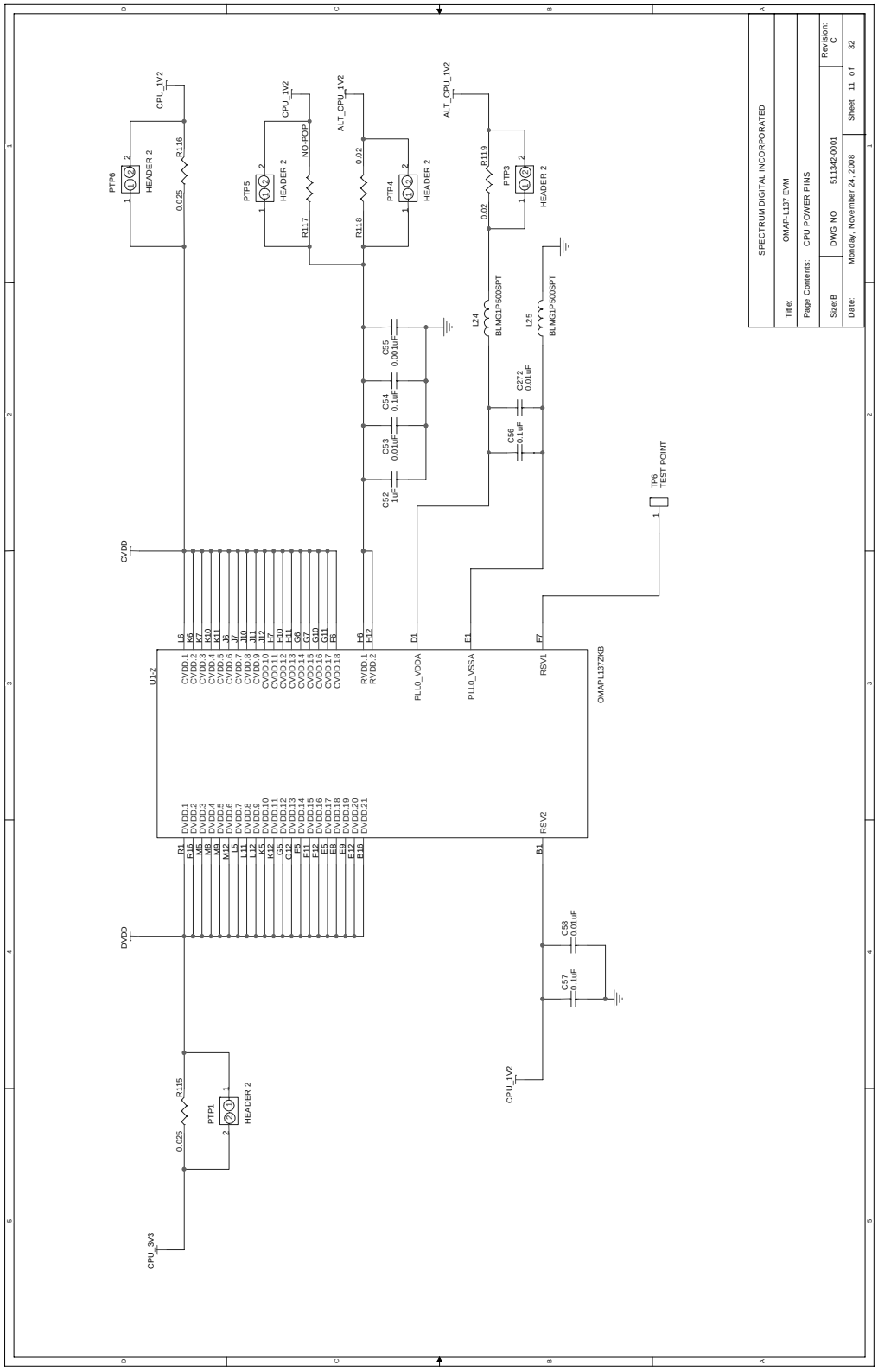

THESE FOOTPRINTS ARE OVERLAYED
ONLY 1 OF 3 IS POPULATED AT 1 TIME
SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: PRIMUS USB 2.0 INTERFACE
Size: B
DWG NO 5113-42-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 6 of 32
J2B
J2A
J2C
USB-micro/AB connector
FULL SIZE B CONNECTOR
MICRO A-B CONNECTOR
FULL SIZE A CONNECTOR
USB_SHIELD
BLM21PG221SN1
TPD2E001DRL
OMAPL137ZKB
TPS2065D
74CBTLV1G125GRG4
NFM21PC474R1C3D
BLM18AG121SN1D
Differential Pair
USB0_DM
USB0_DP
DSK_3V3
CPU_3V3
CPU_1V8
VCC_5V
TP1
VBUS
TP2
VBUS_OCn2
ON_BD_OFF_BD 8,14
2,27 T_ACLKX0

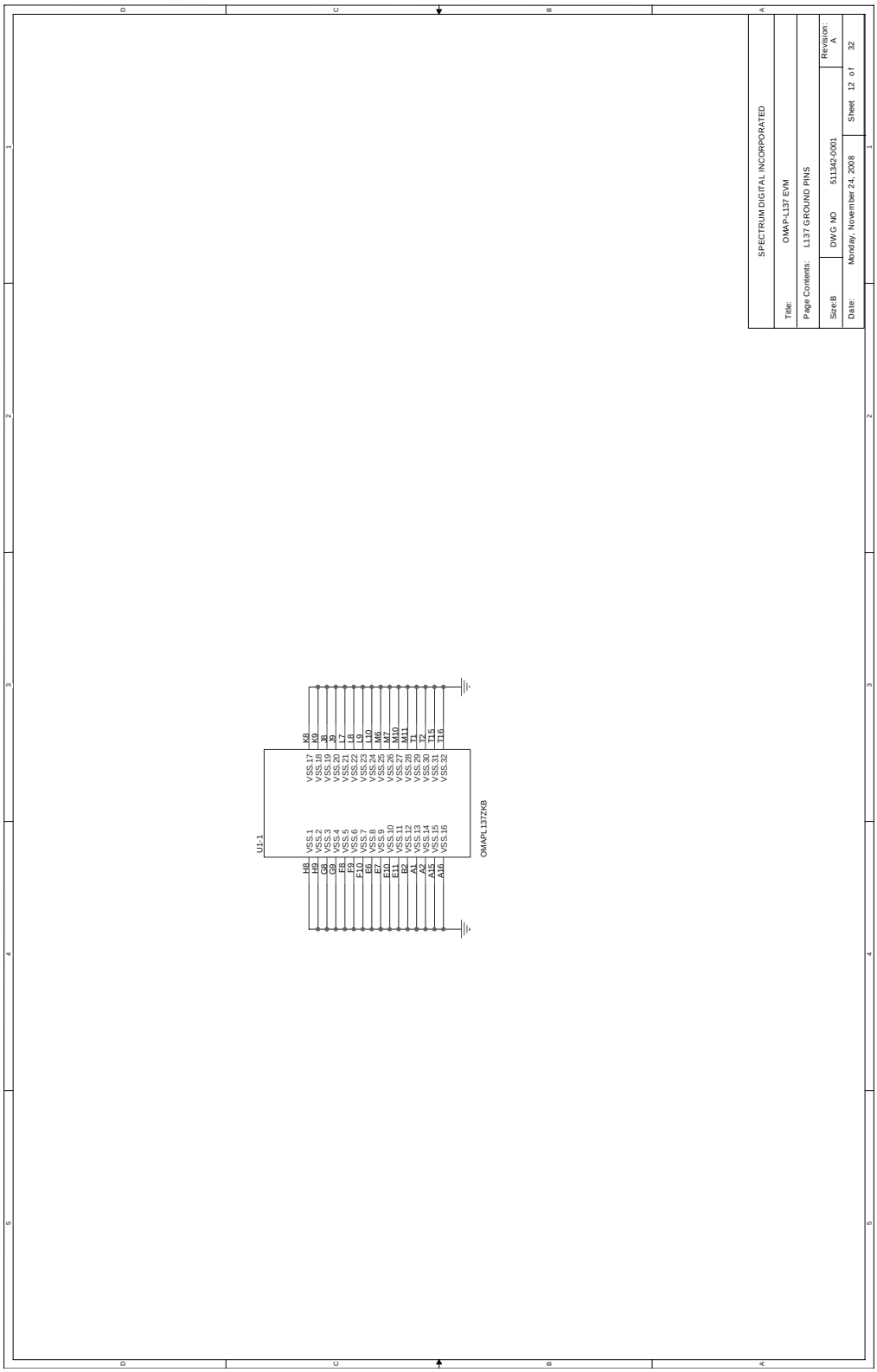

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: USB 1.0 HOST INTERFACE
Size: B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 7 of 32
J3
USB-A connector
U56
TPD2E001DRL
U14
TPS2065D
U1-8
OMAPL137ZKB
Differential Route 90 ohms
USB_DM
USB_DP
USB1_DM
USB1_DP
VBUS_OCn1
8_ON_BD_USB_DRV
8_ON_BD_USB_OVC
CPU_3V3
CPU_1V8
VCC_5V
DSK_3V3

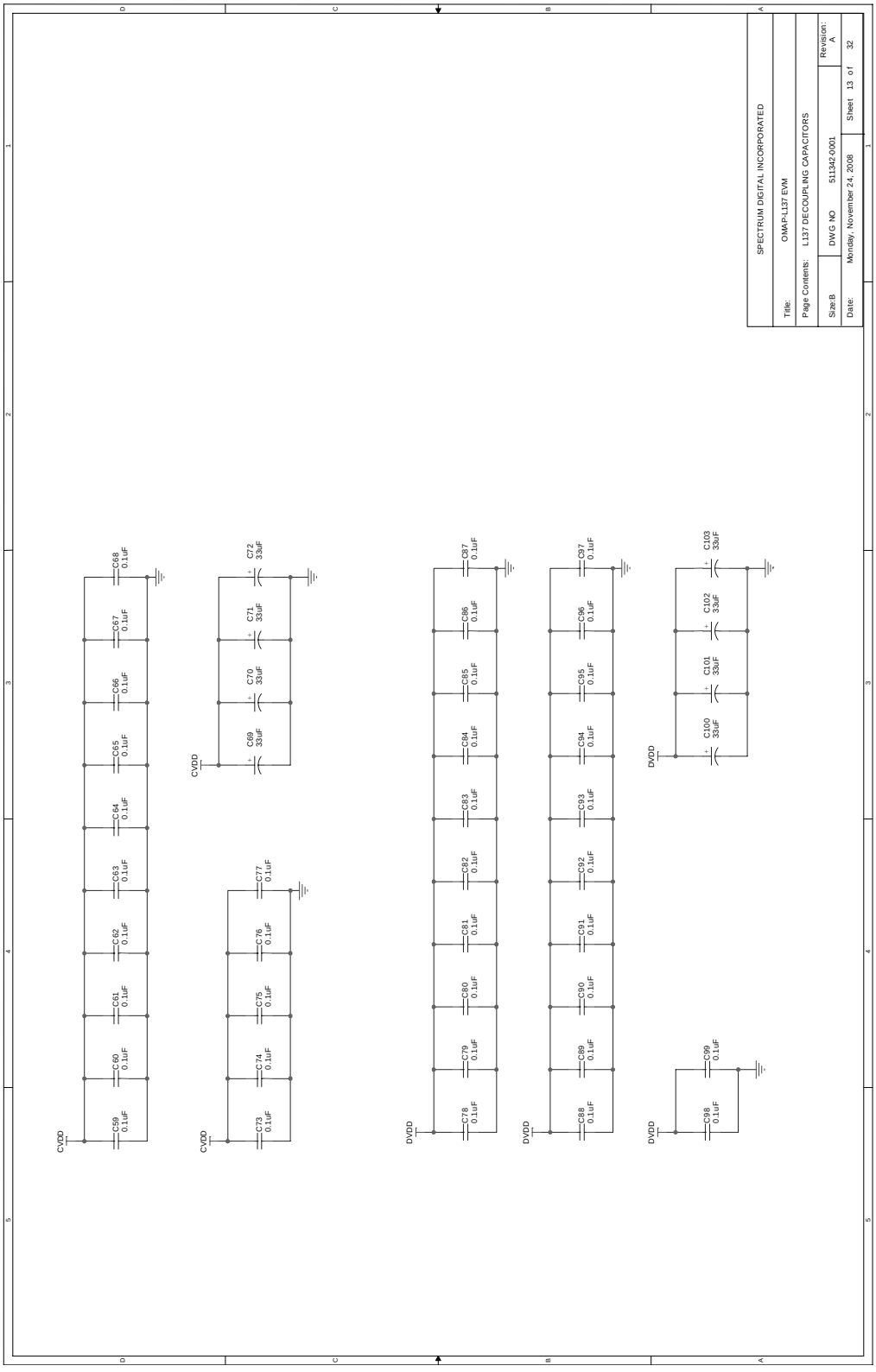

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: CPU EMIF A
Size:B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 8 of 32
OMAPL137ZKB
SN74CBTLV3257PW
74CBTLV3253
SN74CBTLV1G125
RPACK8-22
EMIFA_WAIT0
EMIFA_BA0
EMIFA_BA1
EMIFA_A0
EMIFA_A1
EMIFA_A2
EMIFA_A3
EMIFA_A4
EMIFA_A5
EMIFA_A6
EMIFA_A7
EMIFA_A8
EMIFA_A9
EMIFA_A10
EMIFA_A11
EMIFA_A12
EMIFA_CS2n
EMIFA_CS3n
EMIFA_CS4n
EMIFA_CS5n
EMIFA_CLK
EMIFA_SDCKE
EMIFA_OEn
EMIFA_WEn
EMIFA_WEn_DQM0
EMIFA_WEn_DQM1
EMIFA_D0
EMIFA_D1
EMIFA_D2
EMIFA_D3
EMIFA_D4
EMIFA_D5
EMIFA_D6
EMIFA_D7
EMIFA_D8
EMIFA_D9
EMIFA_D10
EMIFA_D11
EMIFA_D12
EMIFA_D13
EMIFA_D14
EMIFA_D15
DSK_3V3
DC_3V3
VCC_3V3
EXP_EMIFA_CS5n
EXP_EMIFA_WEn
EXP_EMIFA_D8
EXP_EMIFA_D9
EXP_EMIFA_D10
EXP_EMIFA_D11
EXP_EMIFA_D12
EXP_EMIFA_D13
EXP_EMIFA_D14
EXP_EMIFA_D15
EXP3_EMIFA_CLK
EXP3_EMIFA_WEn
EXP3_EMIFA_OEn
EXP3_SEL_MEM
EXP3_SEL_MEM_CTL
EXP3_SEL_MEMD8_D11
EXP3_SEL_MEMD12_D15
EXP1_AMUTE2
EXP3_EMIFA_CS3n
ON_BD_USB_DRV
ON_BD_USB_OVC
ON_BD_OFF_BD
AHCLKR2
USER_SW1
USER_SW2
USER_SW3
USER_SW4
USER_LED1
USER_LED2
USER_LED3
USER_LED4
R65 10K
R66 22
R67 20K
R68 NO-POP
R69 22
R70 20K
R71 NO-POP
R72 22
R73 20K
R74 NO-POP
R75 22
R76 22
R77 22
R78 22
R79 22
R80 22
R81 20K
R82 22
R83 2K
R84 2K
R85 NO-POP
R86 22
R87 22
R88 2K
R89 2K
R384 2K
R152 360
C39 1uF
C40 0.1uF
C41 0.1uF
C42 0.1uF
C43 0.1uF
C265 0.1uF

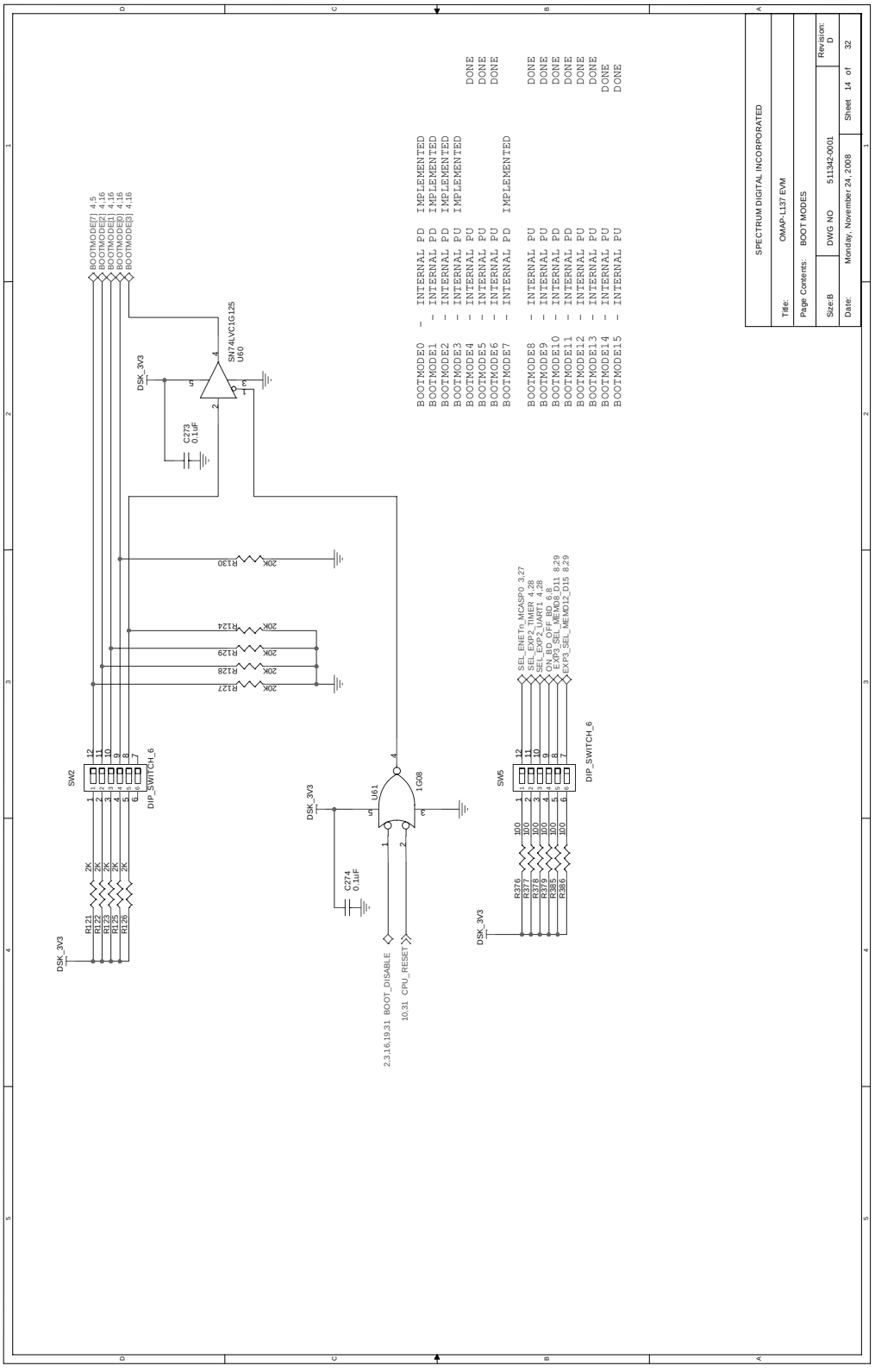

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: CPU EMIF-B
Size:B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 9 of 32
OMAPL137ZKB
RPACK8-22
RPACK8-10
DSK_3V3

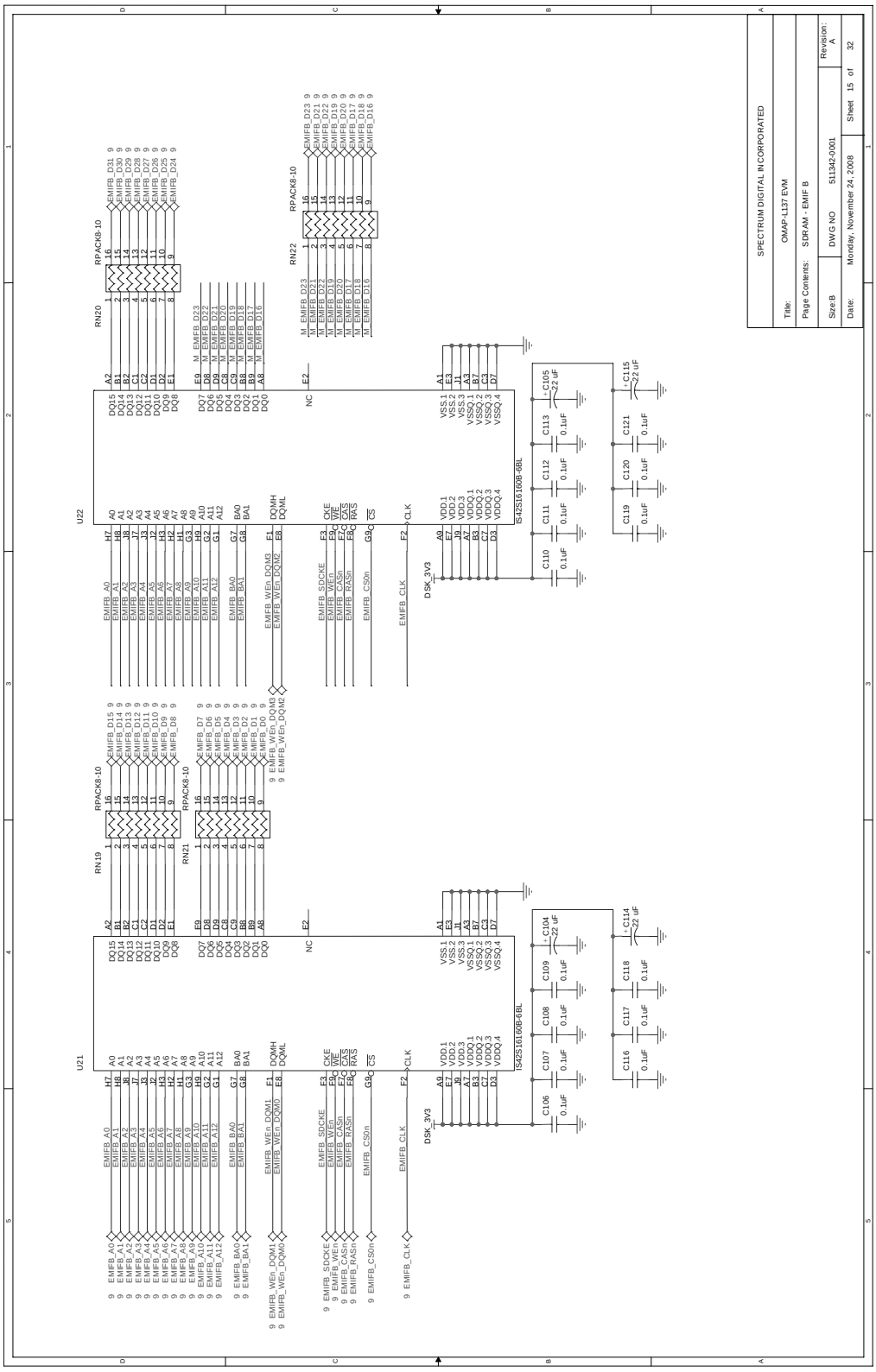

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: CPU JTAG/CLOCKS
Size: B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 10 of 32
CPU_RTC_1V8
R100
0.02
D21
MMBD4148
SD Gold
Panasonic
sptecap
C607
.33F
C45
0.01uF
C44
0.1uF
C46
18 pF
Y1
32KHZ
C47
18 pF
R103
NO-POP
R104
0
R105
NO-POP
C48
18 pF
Y2
24MHz
C49
18 pF
R106
NO-POP
R108
0
R109
NO-POP
U1-5
OMAPL1372KB
RTC_CVDD
RTC_XI
RTC_XO
RTC_VSS
OSCIN
OSCOUT
OSCVSS
RESET
TMS
TDI
TDO
TRST
TCK
RTCK/GPIO7_14
EMU_0/GPIO7_15
DSK_3V3
R101
10K
R102
NO-POP
14,31 CPU_RESET
21 DSP_TMS
21 DSP_TDI
21 DSP_TDO
21 DSP_TRST#
21 DSP_TCK
R107
100
C50
22pF
DSP_EMU0
DSP_EMU1
R111
10K
R110
10K
SW1
CASD20TB
R114
2.2K
R113
2.2K
21 DSP_EMU0
21 DSP_EMU1
C51
0.1uF
U20
SN74LVC1G32
33
R112
21 DSP_RTCK

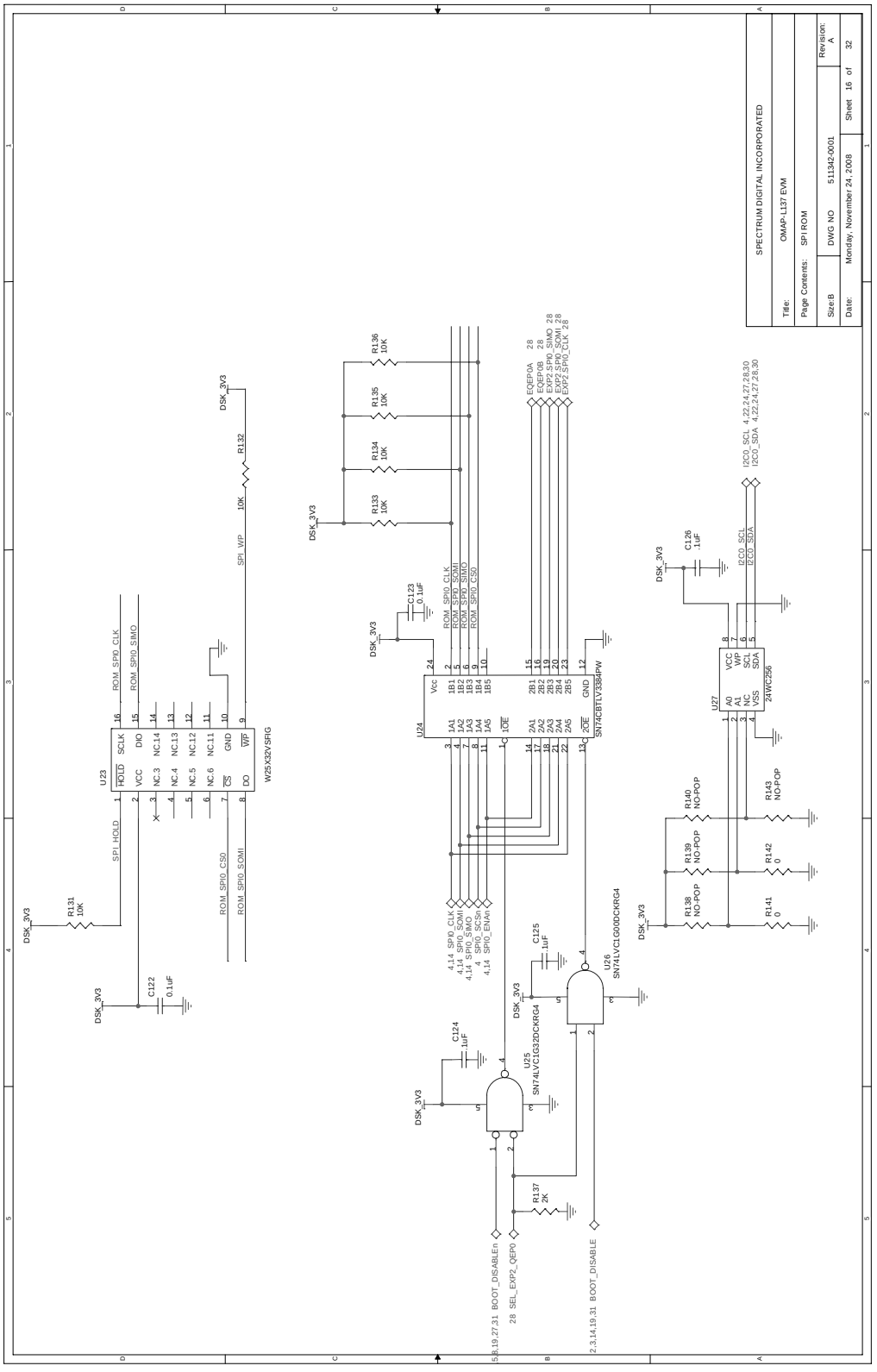

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: CPU POWER PINS
Size: B
DWG NO 511342-0001
Revision: C
Date: Monday, November 24, 2008
Sheet 11 of 32
CPU_1V2
ALT_CPU_1V2
CPU_3V3
CVDD
DVDD
PTP1
PTP3
PTP4
PTP5
PTP6
HEADER 2
NO-POP
R115
R116
R117
R118
R119
0.025
0.02
L24
L25
BLM31P500SPT
C52
C53
C54
C55
C56
C57
C58
C272
0.01uF
0.1uF
1uF
TP6
TEST POINT
U1:2
OMAPL137ZKB
CVDD.1
CVDD.2
CVDD.3
CVDD.4
CVDD.5
CVDD.6
CVDD.7
CVDD.8
CVDD.9
CVDD.10
CVDD.11
CVDD.12
CVDD.13
CVDD.14
CVDD.15
CVDD.16
CVDD.17
CVDD.18
RVDD.1
RVDD.2
PLL0_VDDA
PLL0_VSSA
RSV1
RSV2
DVDD.1
DVDD.2
DVDD.3
DVDD.4
DVDD.5
DVDD.6
DVDD.7
DVDD.8
DVDD.9
DVDD.10
DVDD.11
DVDD.12
DVDD.13
DVDD.14
DVDD.15
DVDD.16
DVDD.17
DVDD.18
DVDD.19
DVDD.20
DVDD.21

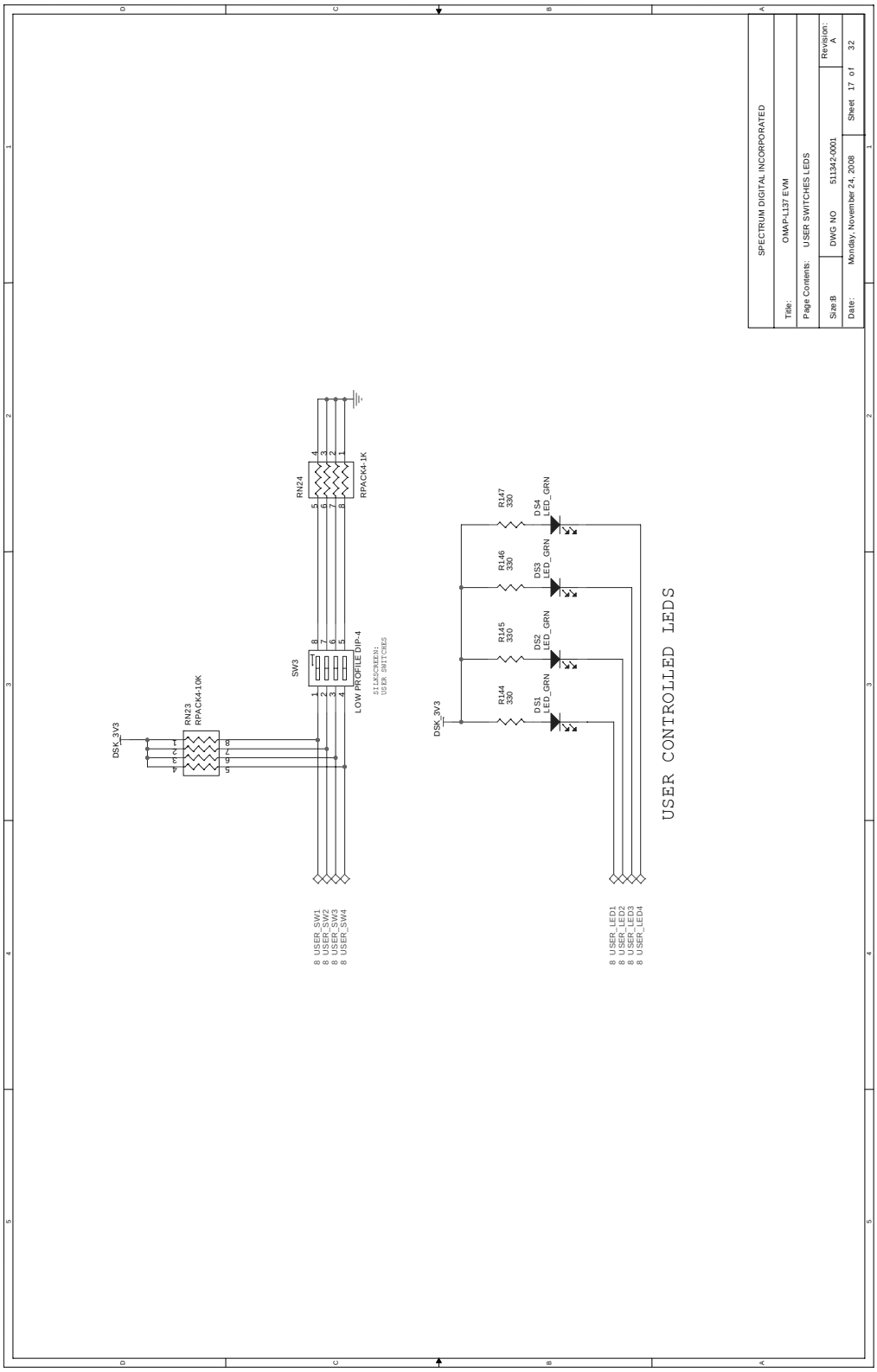

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: L137 GROUND PINS
Size:B DWG NO 511342-0001 Revision: A
Date: Monday, November 24, 2008 Sheet 12 of 32
U1-1
OMAPL137ZKB
VSS.1 VSS.2 VSS.3 VSS.4 VSS.5 VSS.6 VSS.7 VSS.8 VSS.9 VSS.10 VSS.11 VSS.12 VSS.13 VSS.14 VSS.15 VSS.16
VSS.17 VSS.18 VSS.19 VSS.20 VSS.21 VSS.22 VSS.23 VSS.24 VSS.25 VSS.26 VSS.27 VSS.28 VSS.29 VSS.30 VSS.31 VSS.32

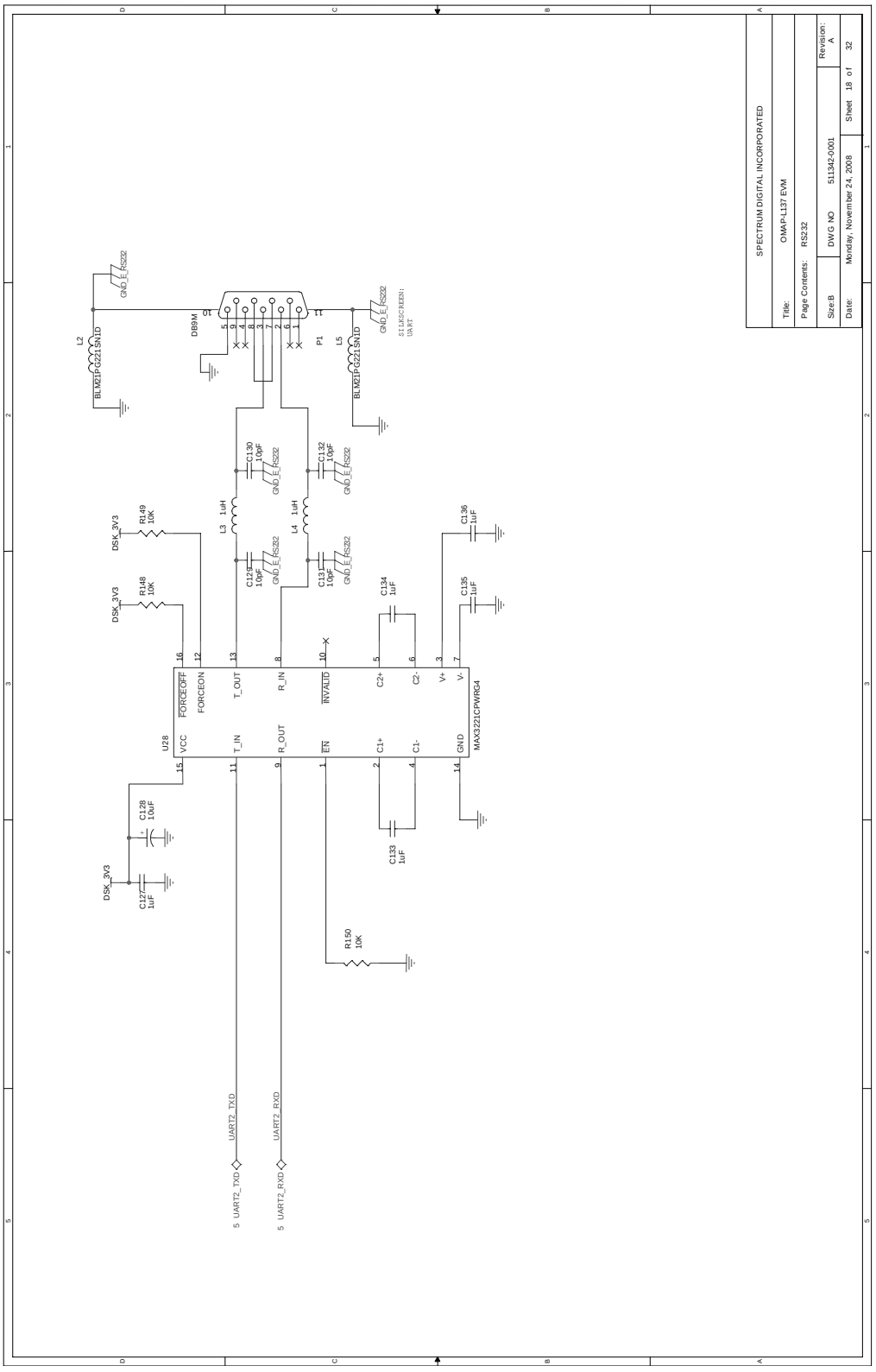

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: L137 DECOUPLING CAPACITORS
Size: B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 13 of 32
CVDD
DVDD
C59 0.1uF
C60 0.1uF
C61 0.1uF
C62 0.1uF
C63 0.1uF
C64 0.1uF
C65 0.1uF
C66 0.1uF
C67 0.1uF
C68 0.1uF
C69 33uF
C70 33uF
C71 33uF
C72 33uF
C73 0.1uF
C74 0.1uF
C75 0.1uF
C76 0.1uF
C77 0.1uF
C78 0.1uF
C79 0.1uF
C80 0.1uF
C81 0.1uF
C82 0.1uF
C83 0.1uF
C84 0.1uF
C85 0.1uF
C86 0.1uF
C87 0.1uF
C88 0.1uF
C89 0.1uF
C90 0.1uF
C91 0.1uF
C92 0.1uF
C93 0.1uF
C94 0.1uF
C95 0.1uF
C96 0.1uF
C97 0.1uF
C98 0.1uF
C99 0.1uF
C100 33uF
C101 33uF
C102 33uF
C103 33uF

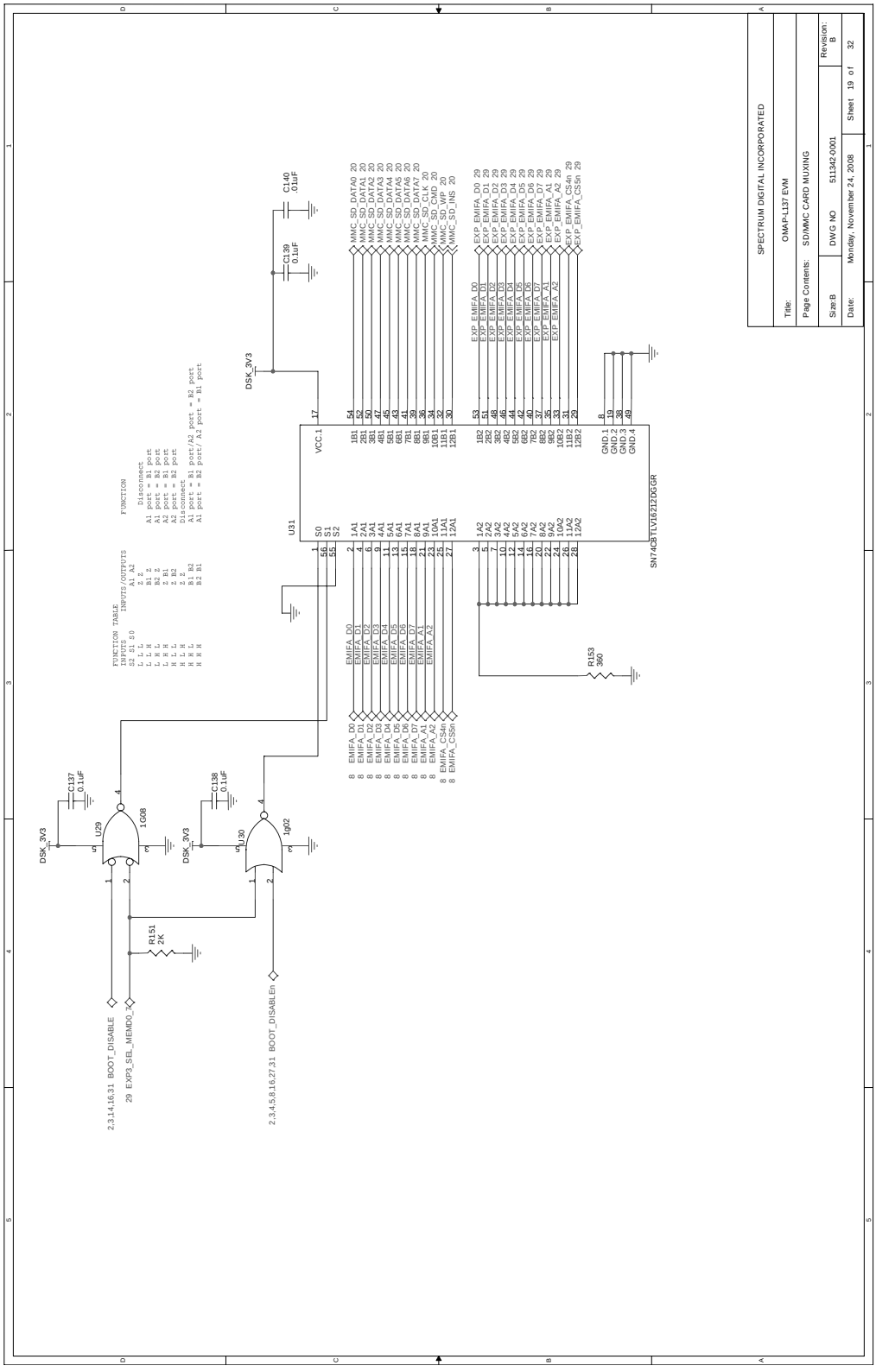

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: BOOT MODES
Size:B DWG NO 511342-0001 Revision: D
Date: Monday, November 24, 2008 Sheet 14 of 32
BOOTMODE0 - INTERNAL PD IMPLEMENTED
BOOTMODE1 - INTERNAL PD IMPLEMENTED
BOOTMODE2 - INTERNAL PD IMPLEMENTED
BOOTMODE3 - INTERNAL PU IMPLEMENTED
BOOTMODE4 - INTERNAL PU DONE
BOOTMODE5 - INTERNAL PU DONE
BOOTMODE6 - INTERNAL PU DONE
BOOTMODE7 - INTERNAL PD IMPLEMENTED
BOOTMODE8 - INTERNAL PU DONE
BOOTMODE9 - INTERNAL PU DONE
BOOTMODE10 - INTERNAL PD DONE
BOOTMODE11 - INTERNAL PD DONE
BOOTMODE12 - INTERNAL PU DONE
BOOTMODE13 - INTERNAL PU DONE
BOOTMODE14 - INTERNAL PU DONE
BOOTMODE15 - INTERNAL PU DONE
BOOTMODE[7] 4.5
BOOTMODE[2] 4.16
BOOTMODE[1] 4.16
BOOTMODE[0] 4.16
BOOTMODE[3] 4.16
SN74LVC1G125 U60
DSK_3V3
C273 0.1uF
R130 20K
R124 20K
R129 20K
R128 20K
R127 20K
SW2
DIP_SWITCH_6
R121 2K
R122 2K
R123 2K
R124 2K
R125 2K
R126 2K
U61
1G08
C274 0.1uF
2,3,16,19,31 BOOT_DISABLE
10,31 CPU_RESET
SW5
DIP_SWITCH_6
R376 100
R377 100
R378 100
R379 100
R385 100
R386 100
SEL_ENETn_MCASP0 3,27
SEL_EXP_TIM64 4,28
SEL_EXP2_UART1 4,28
ON_BD_OFF_BD 6,8
EXP3_SEL_MEM32_D11 8,29
EXP3_SEL_MEM32_D15 8,29

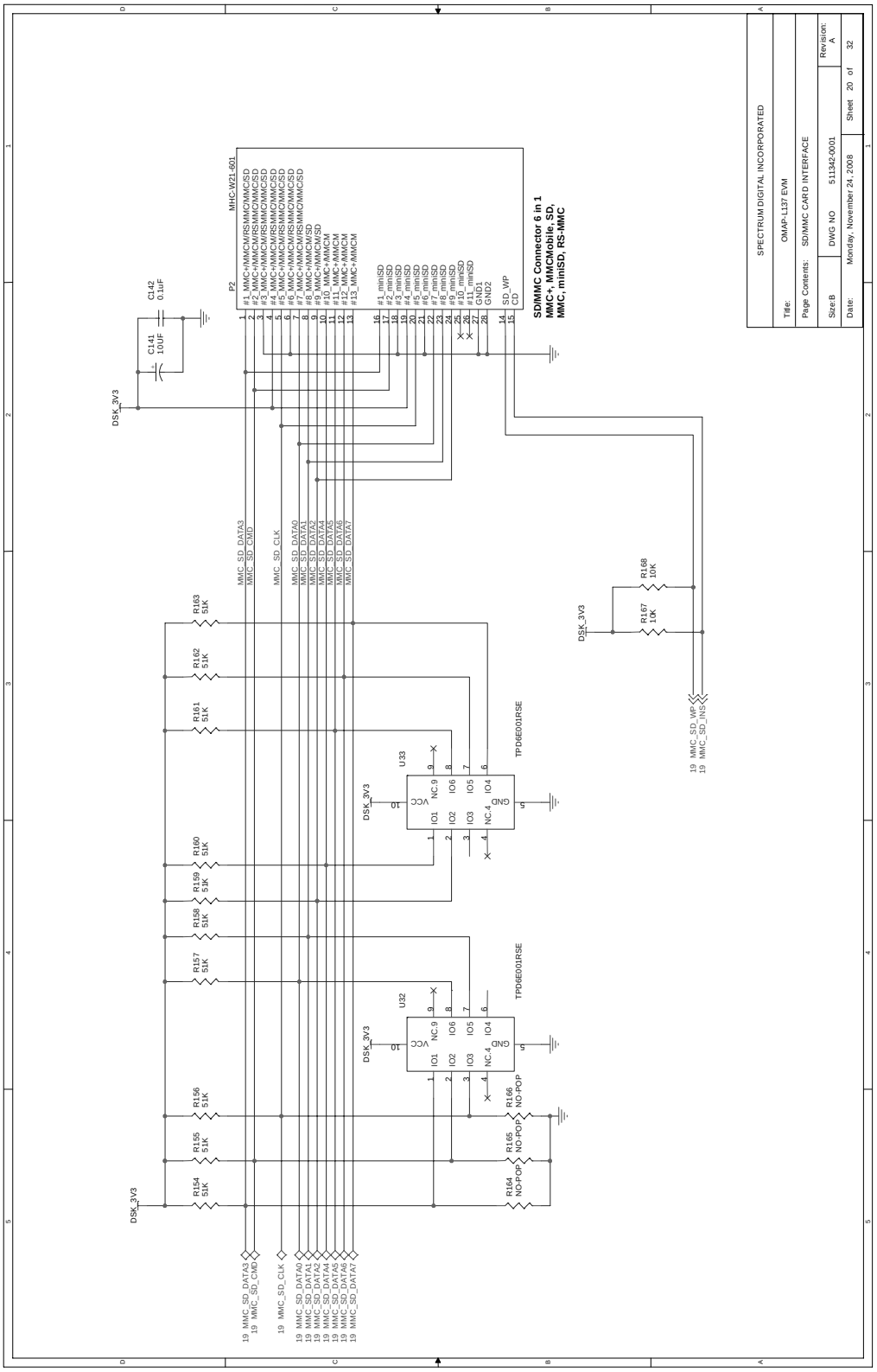

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: SDRAM - EMIF B
Size:B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 15 of 32
U21
U22
RN19
RN20
RN21
RN22
RPACK8-10
IS42S16160B-6BL
DSK_3V3
EMIFB_A0
EMIFB_A1
EMIFB_A2
EMIFB_A3
EMIFB_A4
EMIFB_A5
EMIFB_A6
EMIFB_A7
EMIFB_A8
EMIFB_A9
EMIFB_A10
EMIFB_A11
EMIFB_A12
EMIFB_BA0
EMIFB_BA1
EMIFB_WEn_DQM1
EMIFB_WEn_DQM0
EMIFB_SDCKE
EMIFB_WEn
EMIFB_CASn
EMIFB_RASn
EMIFB_CS0n
EMIFB_CLK
EMIFB_WEn_DQM3
EMIFB_WEn_DQM2
C104 22 uF
C105 22 uF
C106 0.1uF
C107 0.1uF
C108 0.1uF
C109 0.1uF
C110 0.1uF
C111 0.1uF
C112 0.1uF
C113 0.1uF
C114 22 uF
C115 22 uF
C116 0.1uF
C117 0.1uF
C118 0.1uF
C119 0.1uF
C120 0.1uF
C121 0.1uF

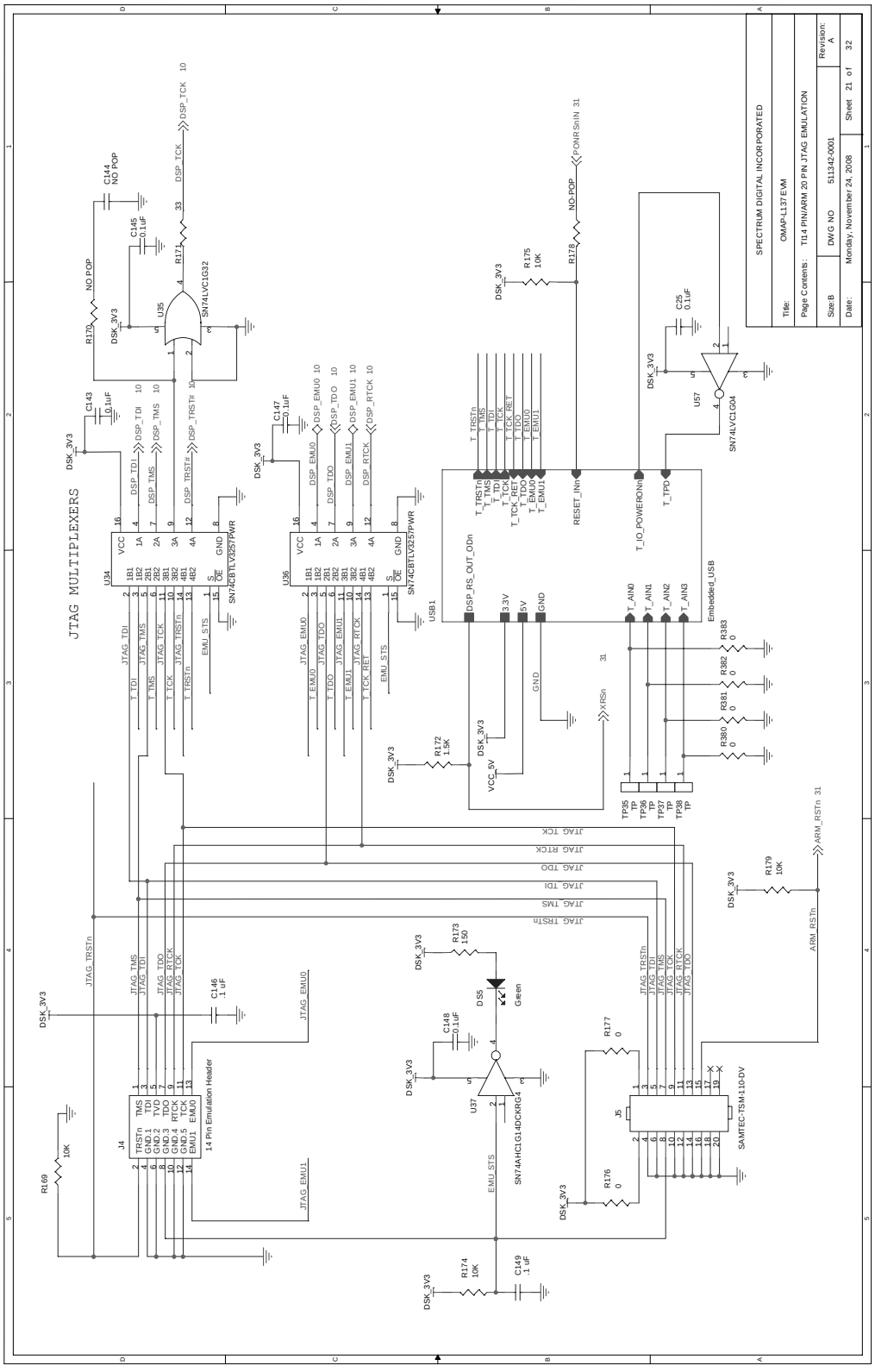

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: SPI ROM
Size B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 16 of 32
U23
W25X32VSFIG
SPI_HOLD
ROM_SPI0_CLK
ROM_SPI0_SIMO
ROM_SPI0_CS0
ROM_SPI0_SOMI
SPI_WP
U24
SN74CBTLV3384PW
U25
SN74LVC1G32DCKRG4
U26
SN74LVC1G00DCKRG4
U27
24WC256
R131 10K
R132 10K
R133 10K
R134 10K
R135 10K
R136 10K
R137 2K
R138 NO-POP
R139 NO-POP
R140 NO-POP
R141 0
R142 0
R143 NO-POP
C122 0.1uF
C123 0.1uF
C124 1uF
C125 1uF
C126 1uF
DSK_3V3
BOOT_DISABLEn
SEL_EXP2_QEP0
BOOT_DISABLE
I2C0_SCL
I2C0_SDA
EQEP0A
EQEP0B
EXP2.SPI0_SIMO
EXP2.SPI0_SOMI
EXP2.SPI0_CLK

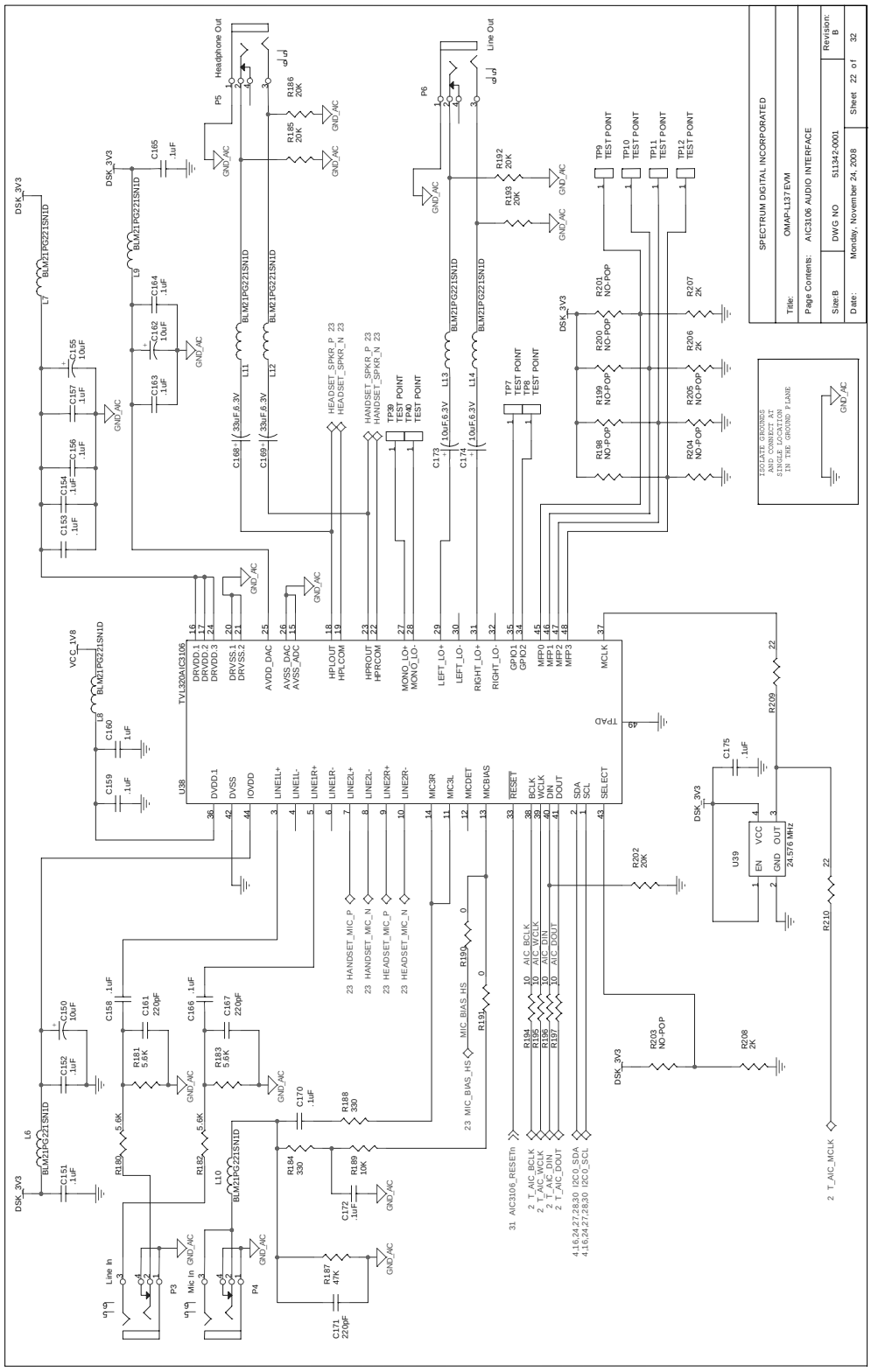

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: USER SWITCHES LEDS
Size:B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 17 of 32
USER CONTROLLED LEDS
DSK_3V3
RN23
RPACK4-10K
SW3
LOW PROFILE DIP-4
SILKSCREEN: USER SWITCHES
RN24
RPACK4-1K
R144 330
R145 330
R146 330
R147 330
DS1 LED_GRN
DS2 LED_GRN
DS3 LED_GRN
DS4 LED_GRN
8 USER_SW1
8 USER_SW2
8 USER_SW3
8 USER_SW4
8 USER_LED1
8 USER_LED2
8 USER_LED3
8 USER_LED4

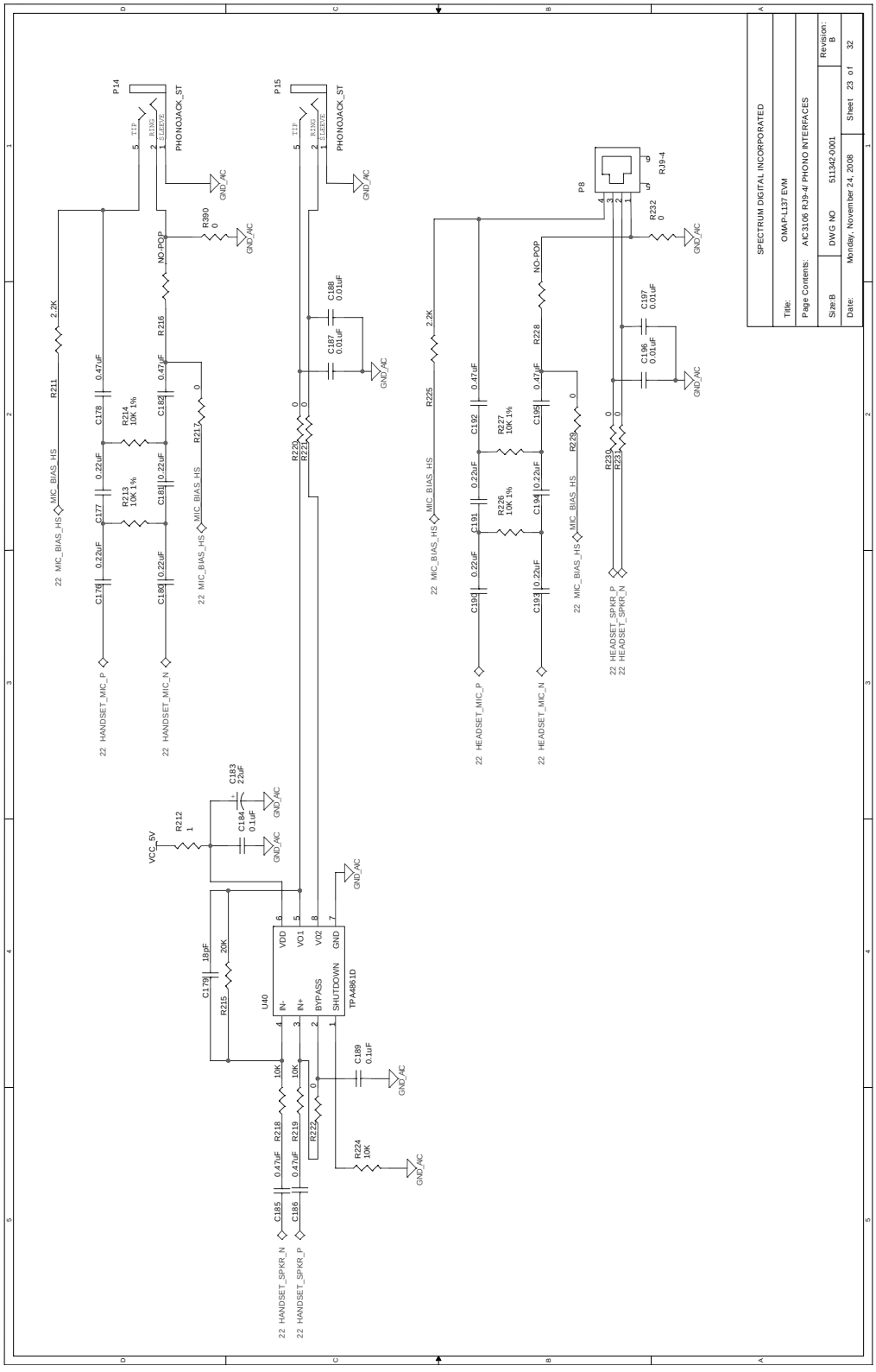

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: RS232
Size:B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 18 of 32
MAX3221CPWR64
UART2_TXD
UART2_RXD

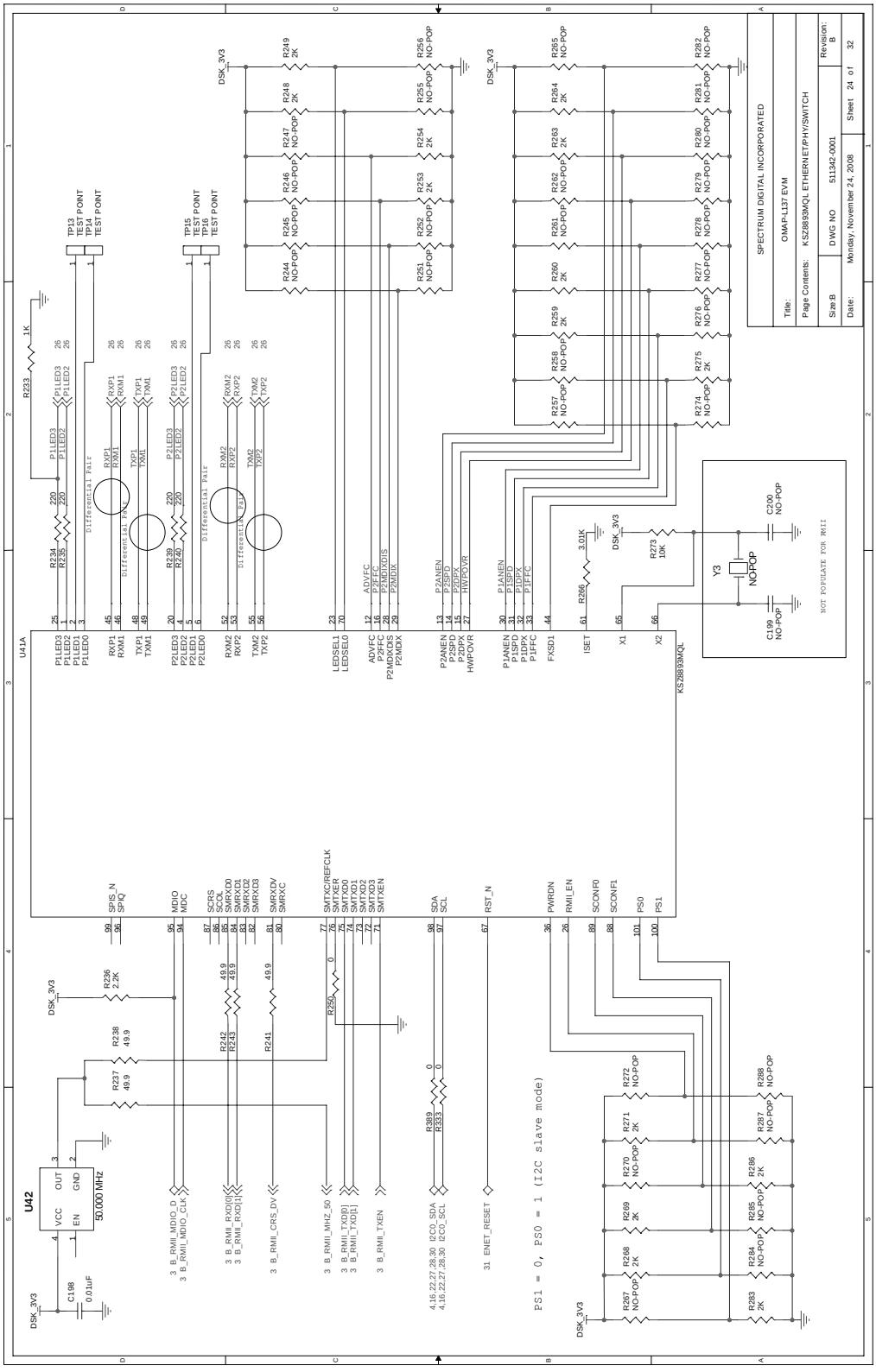

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: SD/MMC CARD MUXING
Size: B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 19 of 32
U31
SN74CBTLV16212DGGR
U29
U30
1G08
1g02
C137 0.1uF
C138 0.1uF
C139 0.1uF
C140 .01uF
R151 2K
R153 360
DSK_3V3
BOOT_DISABLE
EXP3_SEL_MEMD0_N
BOOT_DISABLEn
EMIFA_D0
EMIFA_D1
EMIFA_D2
EMIFA_D3
EMIFA_D4
EMIFA_D5
EMIFA_D6
EMIFA_D7
EMIFA_A1
EMIFA_A2
EMIFA_CS4n
EMIFA_CS5n
MMC_SD_DATA0
MMC_SD_DATA1
MMC_SD_DATA2
MMC_SD_DATA3
MMC_SD_DATA4
MMC_SD_DATA5
MMC_SD_DATA6
MMC_SD_DATA7
MMC_SD_CLK
MMC_SD_CMD
MMC_SD_WP
MMC_SD_INS
EXP_EMIFA_D0
EXP_EMIFA_D1
EXP_EMIFA_D2
EXP_EMIFA_D3
EXP_EMIFA_D4
EXP_EMIFA_D5
EXP_EMIFA_D6
EXP_EMIFA_D7
EXP_EMIFA_A1
EXP_EMIFA_A2
EXP_EMIFA_CS4n
EXP_EMIFA_CS5n

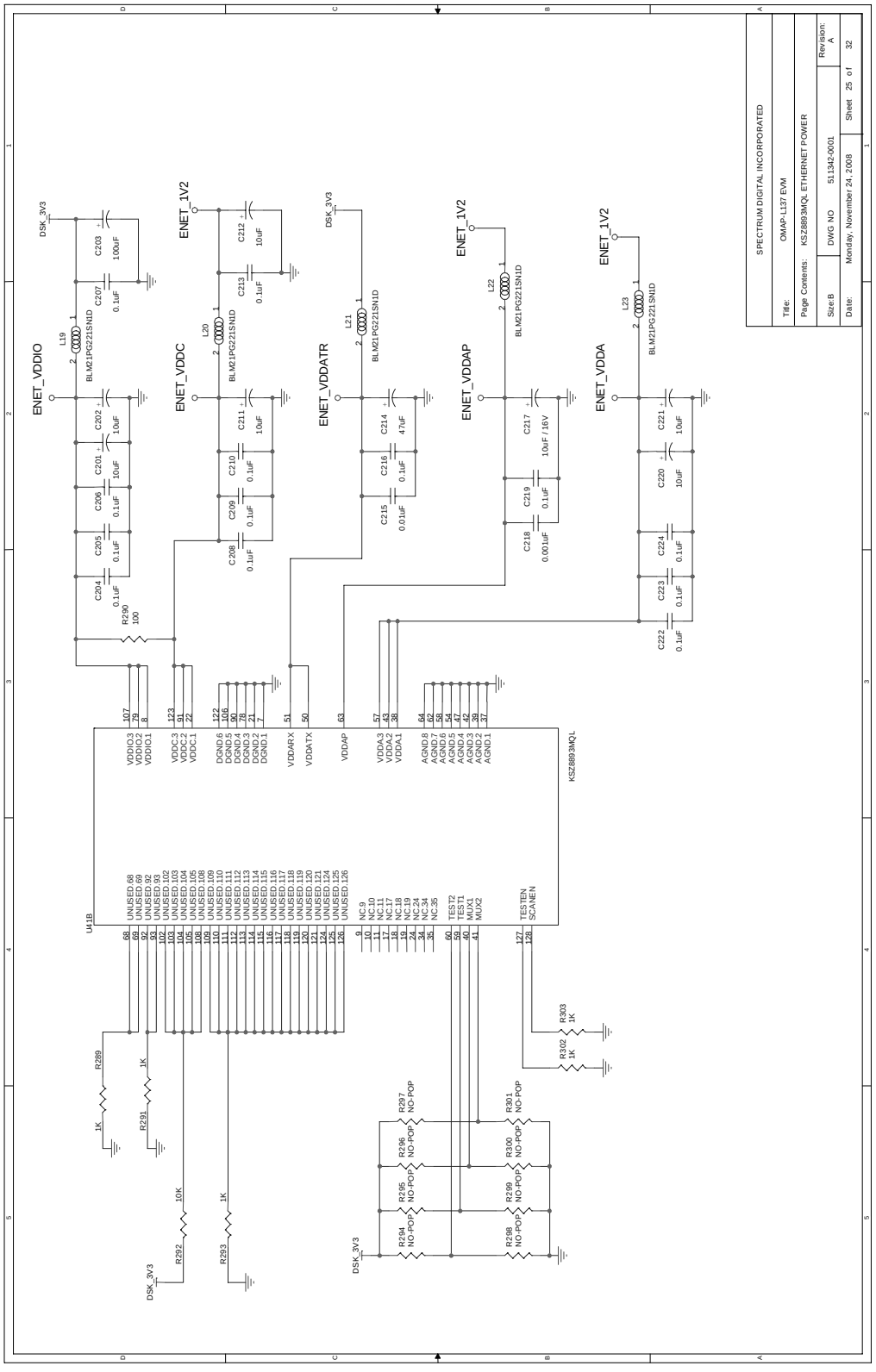

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: SD/MMC CARD INTERFACE
Size:B DWG NO 511342-0001 Revision: A
Date: Monday, November 24, 2008 Sheet 20 of 32
SD/MMC Connector 6 in 1
MMC+, MMCMobile, SD,
MMC, miniSD, RS-MMC
P2
MHC-W21-601
C142 0.1uF
C141 10UF
DSK_3V3
R163 51K
R162 51K
R161 51K
R160 51K
R159 51K
R158 51K
R157 51K
R156 51K
R155 51K
R154 51K
R168 10K
R167 10K
R166 NO-POP
R165 NO-POP
R164 NO-POP
U33
U32
TPD6E001RSE
MMC_SD_DAT3
MMC_SD_CMD
MMC_SD_CLK
MMC_SD_DAT0
MMC_SD_DAT1
MMC_SD_DAT2
MMC_SD_DAT4
MMC_SD_DAT5
MMC_SD_DAT6
MMC_SD_DAT7
MMC_SD_WP
MMC_SD_INS

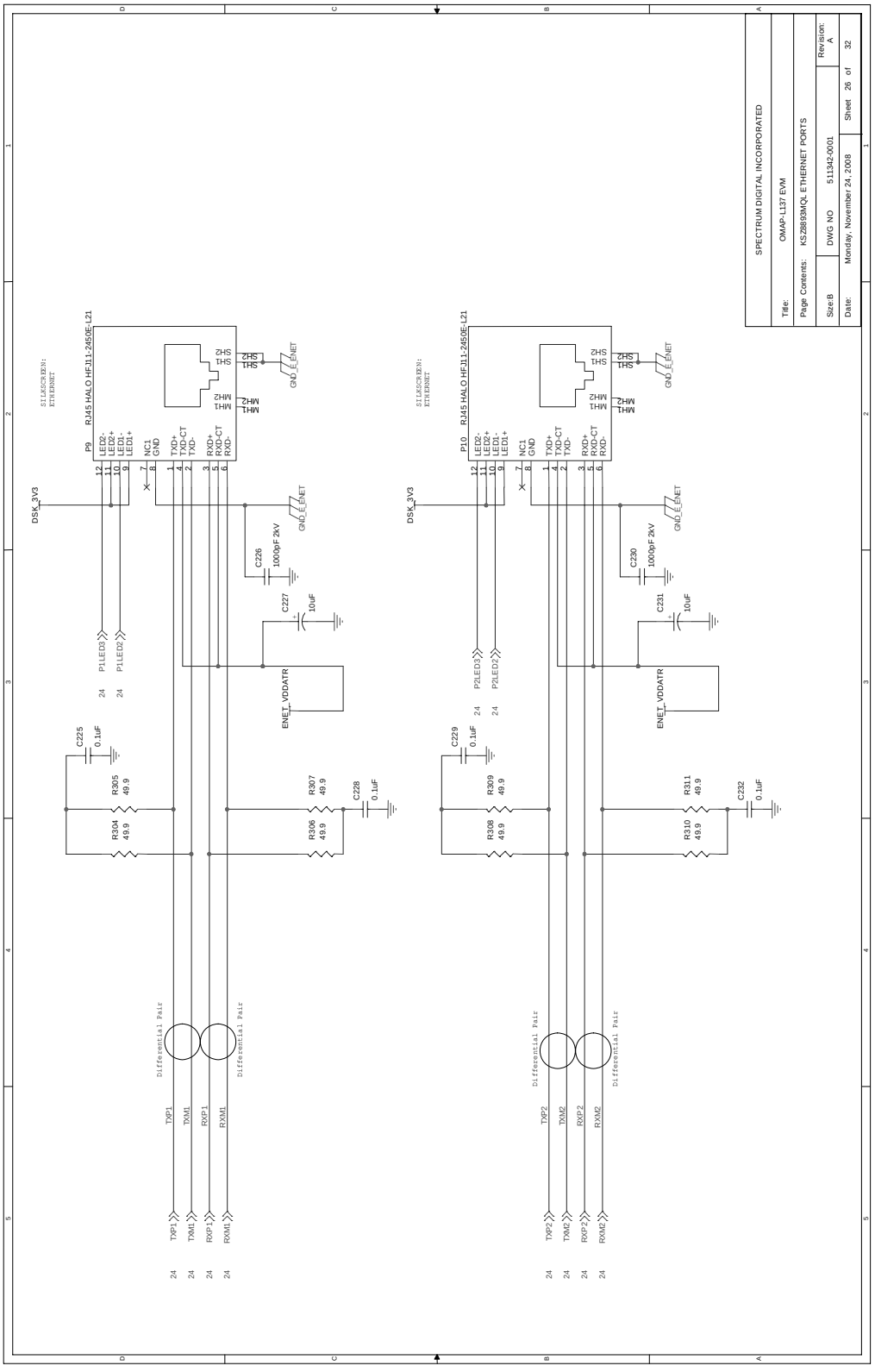

JTAG MULTIPLEXERS
SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: TI14 PIN/ARM 20 PIN JTAG EMULATION
Size: B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 21 of 32
SN74CBTLV3257PWR
SN74LVC1G32
SN74LVC1G04
SN74AHC1G14DCKRG4
14 Pin Emulation Header
SAMTEC-TSM-110-DV
Embedded_USB
JTAG_TRSTn
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_RTCK
JTAG_TCK
JTAG_EMU0
JTAG_EMU1
DSP_TDI
DSP_TMS
DSP_TRST#
DSP_TCK
DSP_EMU0
DSP_TDO
DSP_EMU1
DSP_RTCK
T_TRSTn
T_TMS
T_TDI
T_TCK
T_TCK_RET
T_TDO
T_EMU0
T_EMU1
RESET_IN
T_IO_POWERONn
T_TPD
T_AIN0
T_AIN1
T_AIN2
T_AIN3
DSP_RS_OUT_ODn
3.3V
5V
GND
VCC_5V
EMU_STS
ARM_RSTn
KRSn
PONRSnIN
NO POP
DSK_3V3

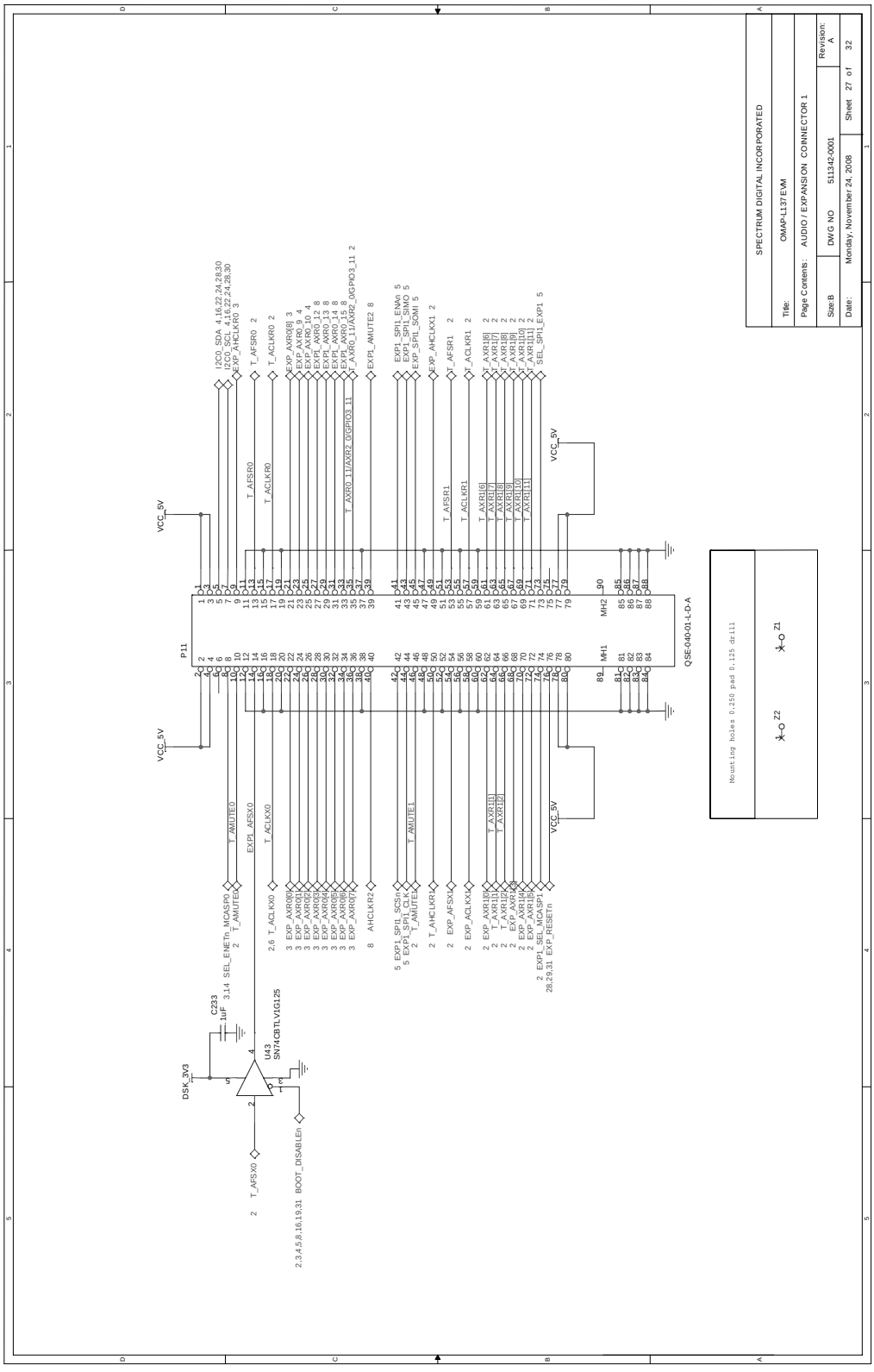

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: AIC3106 AUDIO INTERFACE
Size:B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 22 of 32
TVL320AIC3106
U38
DSK_3V3
VCC_1V8
GND_AIC
Headphone Out
Line Out
Line In
Mic In
P3
P4
P5
P6
U39
24.576 MHz
TP7
TP8
TP9
TP10
TP11
TP12
TP39
TP40
TEST POINT
ISOLATE GROUNDS AND CONNECT AT SINGLE POINT ONLY IN THE GROUND PLANE
HEADSET_SPKR_P 23
HEADSET_SPKR_N 23
HANDSET_SPKR_P 23
HANDSET_SPKR_N 23
HANDSET_MIC_P 23
HANDSET_MIC_N 23
HEADSET_MIC_P 23
HEADSET_MIC_N 23
MIC_BIAS_HS 23
AIC3106_RESETn 31
2 T_AIC_BCLK
2 T_AIC_WCLK
2 T_AIC_DIN
2 T_AIC_DOUT
2 T_AIC_MCLK
4,16,24,27,28,30 I2C0_SDA
4,16,24,27,28,30 I2C0_SCL

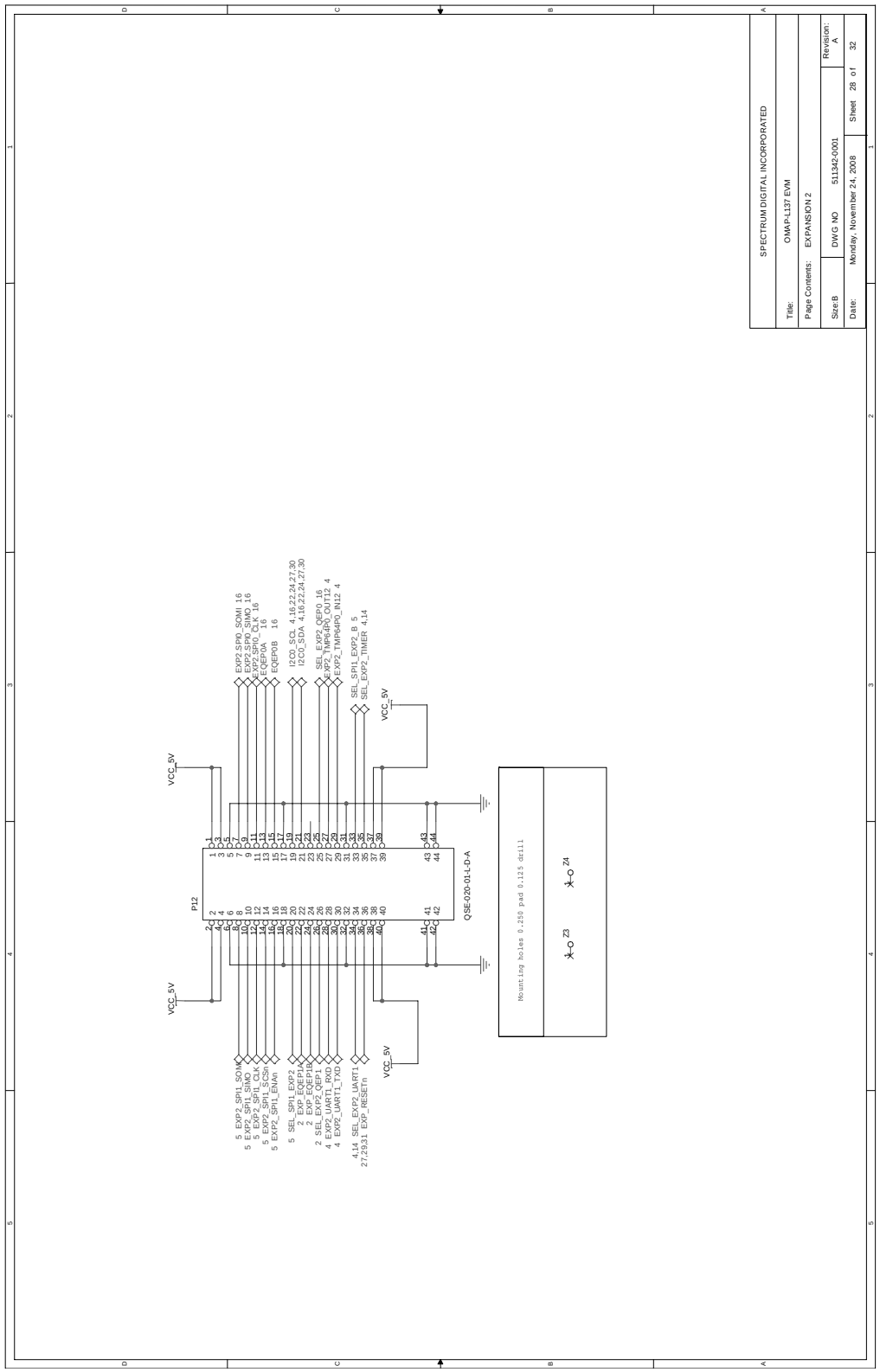

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: AIC3106 RJ9-4/ PHONO INTERFACES
Size: B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 23 of 32
P14
P15
PHONOJACK_ST
P8
RJ9-4
U40
TPA4861D
VDD
VO1
VO2
GND
IN-
IN+
BYPASS
SHUTDOWN
VCC_5V
NO-POP
MIC_BIAS_HS
HANDSET_MIC_P
HANDSET_MIC_N
HANDSET_SPKR_N
HANDSET_SPKR_P
HEADSET_MIC_P
HEADSET_MIC_N
HEADSET_SPKR_P
HEADSET_SPKR_N
GND_AIC

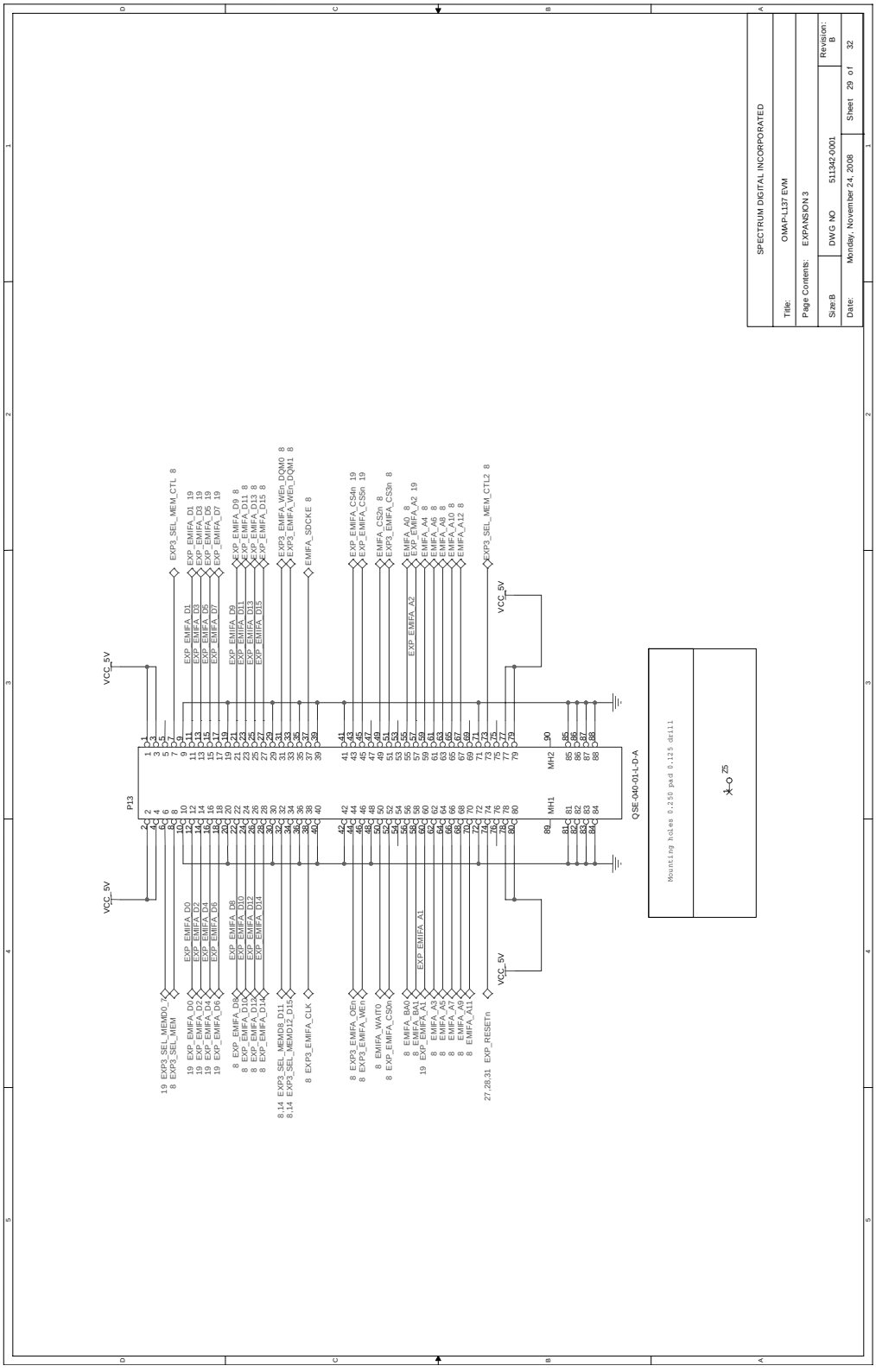

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: KSZ8893MQL ETHERNET/PHYSWITCH
Size: B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 24 of 32
U41A
KSZ8893MQL
U42
50.000 MHz
NOPOP
NOT POPULATE FOR RMII
DSK_3V3
PS1 = 0, PS0 = 1 (I2C slave mode)

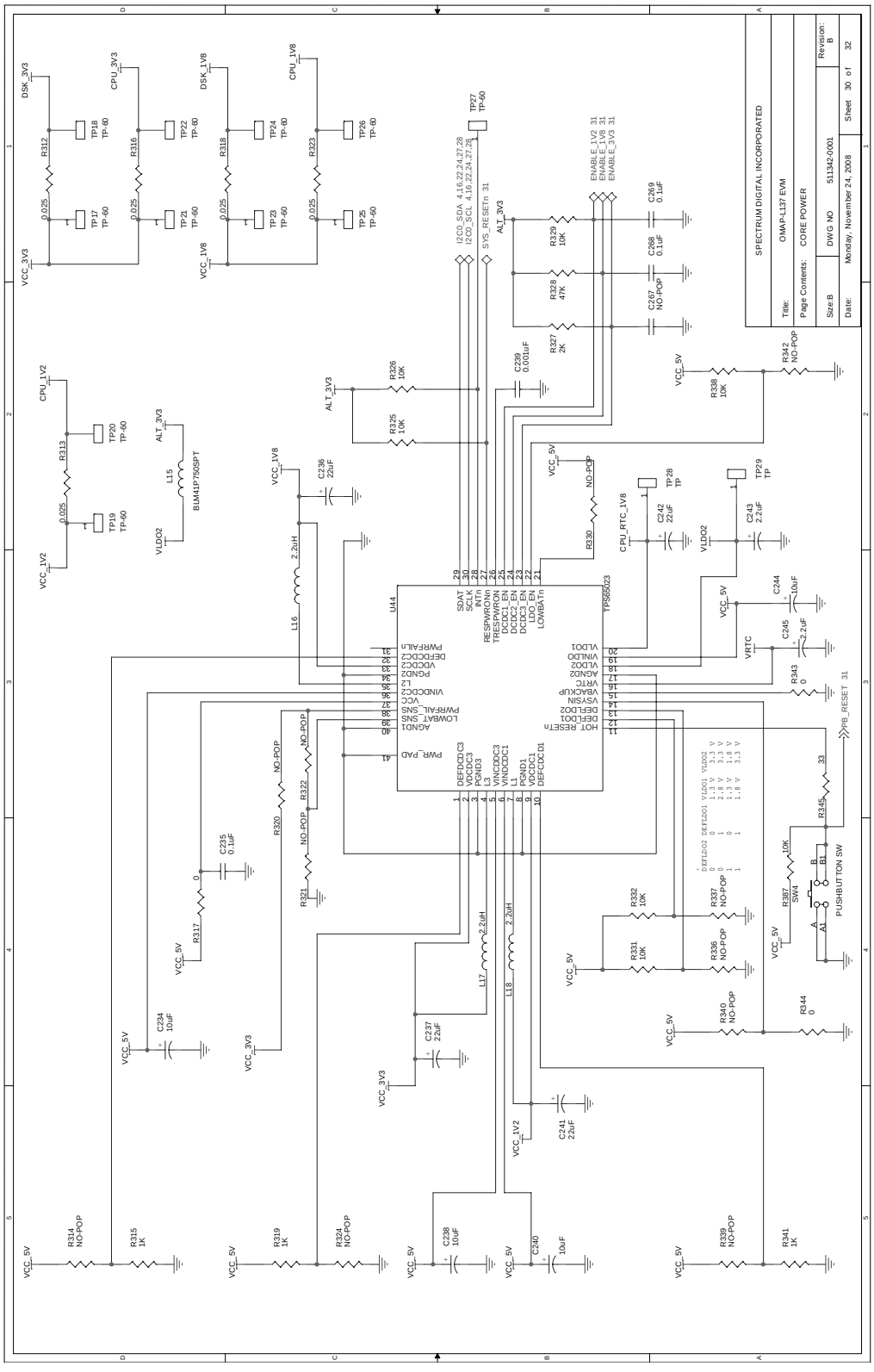

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: KSZ8893MQL ETHERNET POWER
Size: B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 25 of 32
ENET_VDDIO
ENET_VDDC
ENET_VDDATR
ENET_VDDAP
ENET_VDDA
ENET_1V2
DSK_3V3
KSZ8893MQL
U41B
R290 100
R289 1K
R291 1K
R292 10K
R293 1K
R294 NO-POP
R295 NO-POP
R296 NO-POP
R297 NO-POP
R298 NO-POP
R299 NO-POP
R300 NO-POP
R301 NO-POP
R302 1K
R303 1K

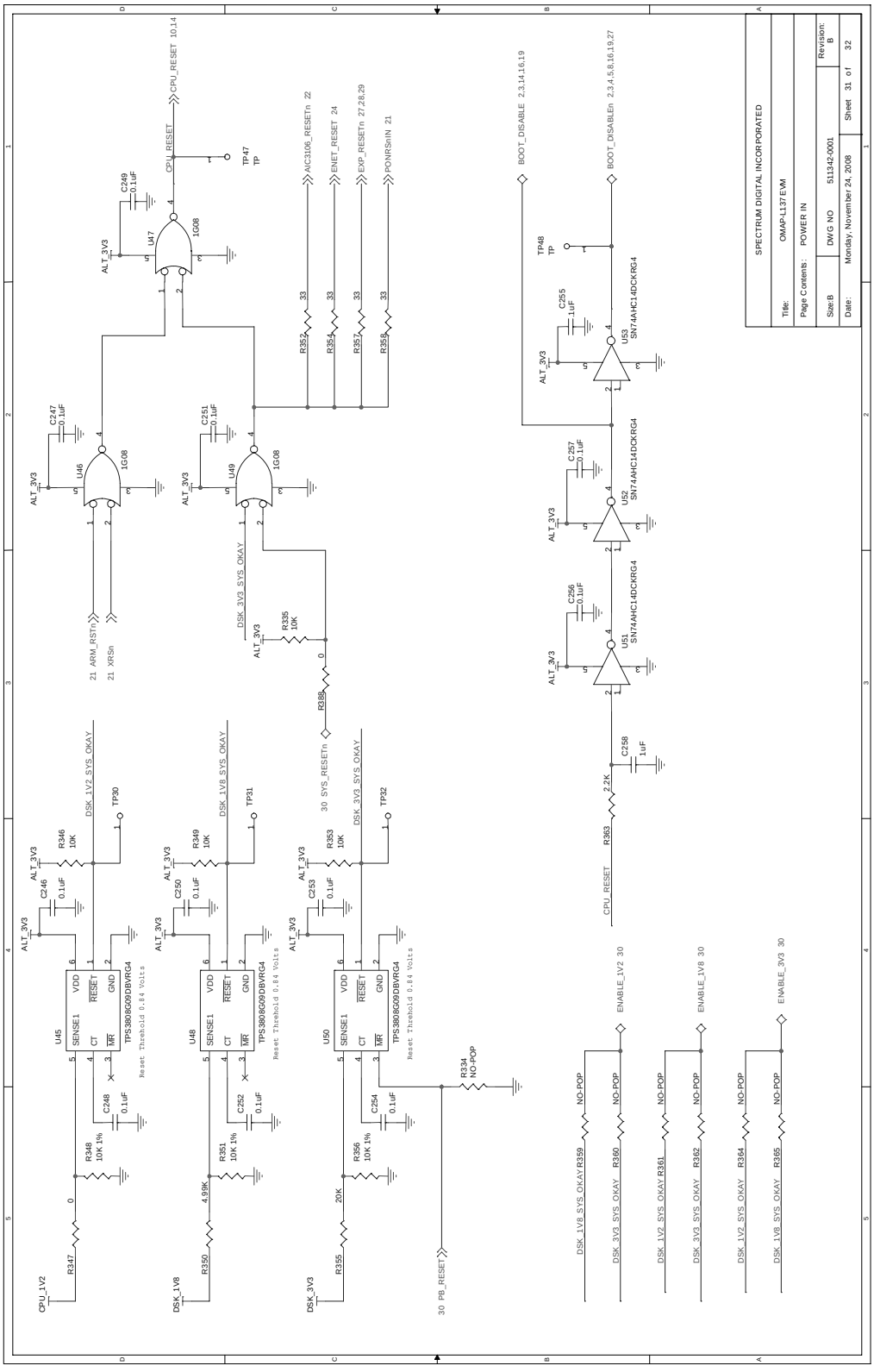

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: KSZ8893MQL ETHERNET PORTS
Size: B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 26 of 32
P9
P10
RJ45 HALO HFJ11-2450E-L21
SILKSCREEN: ETHERNET
LED2-
LED2+
LED1-
LED1+
NC1
GND
TXD+
TXD-CT
TXD-
RXD+
RXD-CT
RXD-
MH1
MH2
SH1
SH2
GND_E_ENET
DSK_3V3
C225
C226
C227
C228
C229
C230
C231
C232
0.1uF
1000pF 2kV
10uF
R304
R305
R306
R307
R308
R309
R310
R311
49.9
ENET_VDDATR
P1LED0
P1LED1
P2LED2
P2LED3
TXP1
TXM1
RXP1
RXM1
TXP2
TXM2
RXP2
RXM2
Differential Pair

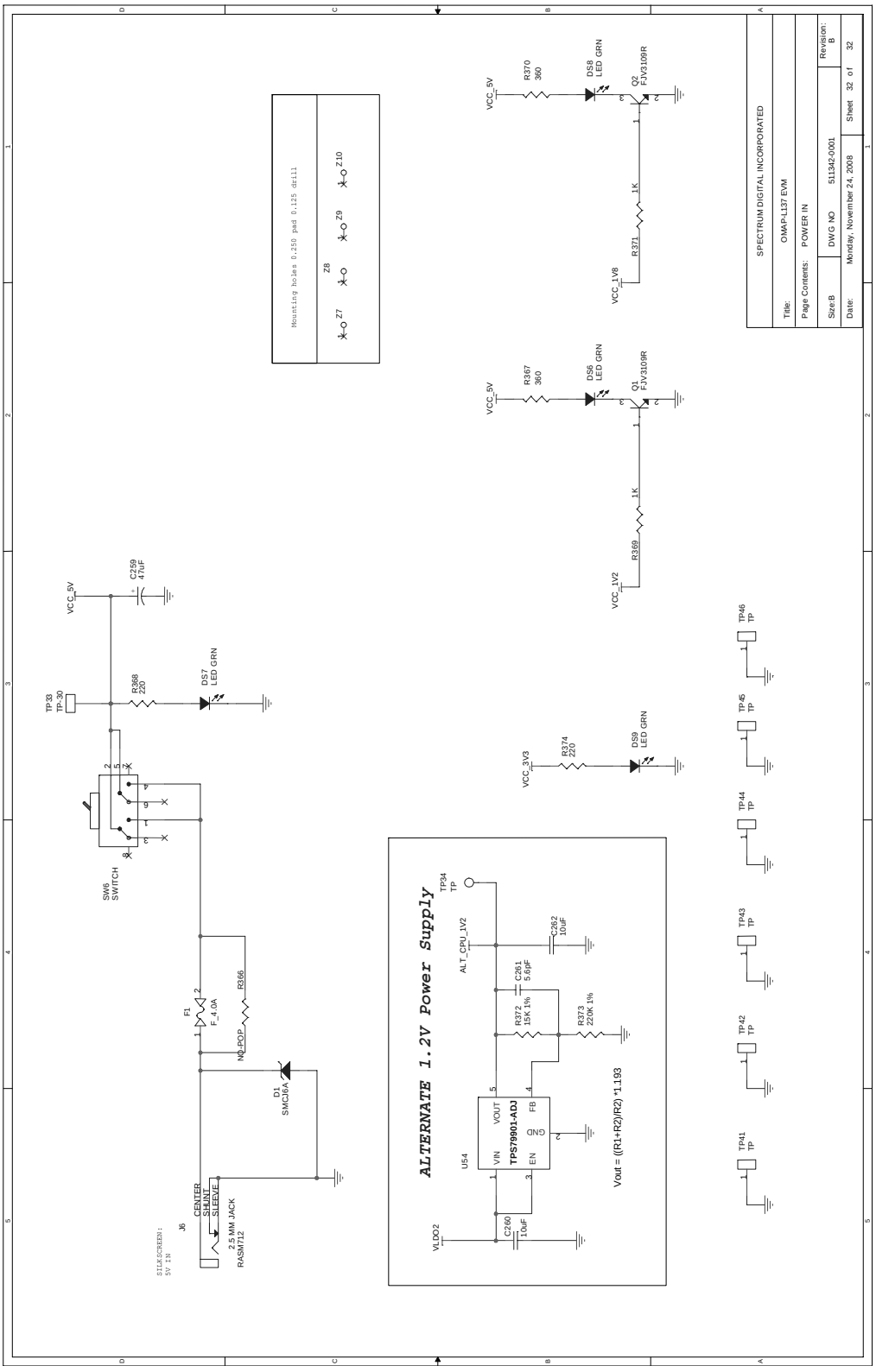

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: AUDIO / EXPANSION CONNECTOR 1
Size: B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 27 of 32
P11
QSE-040-01-L-D-A
U43
SN74CBTLV1G125
C233
1uF
VCC_5V
DSK_3V3
Mounting holes 0.250 pad 0.125 drill


SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: EXPANSION 2
Size:B
DWG NO 511342-0001
Revision: A
Date: Monday, November 24, 2008
Sheet 28 of 32
P12
QSE-020-01-L-D-A
VCC_5V
Mounting holes 0.250 pad 0.125 drill
Z3
Z4


SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: EXPANSION 3
Size: B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 29 of 32
P13
QSE-040-01-L-D-A
MH1
MH2
Z5
Mounting holes 0.250 pad 0.125 drill
VCC_5V
EXP_EMIFA_D0
EXP_EMIFA_D1
EXP_EMIFA_D2
EXP_EMIFA_D3
EXP_EMIFA_D4
EXP_EMIFA_D5
EXP_EMIFA_D6
EXP_EMIFA_D7
EXP_EMIFA_D8
EXP_EMIFA_D9
EXP_EMIFA_D10
EXP_EMIFA_D11
EXP_EMIFA_D12
EXP_EMIFA_D13
EXP_EMIFA_D14
EXP_EMIFA_D15
EXP_EMIFA_A1
EXP_EMIFA_A2
EXP3_SEL_MEM
EXP3_SEL_MEMD0_7
EXP3_SEL_MEMD8_D11
EXP3_SEL_MEMD12_D15
EXP3_EMIFA_CLK
EXP3_EMIFA_OEn
EXP3_EMIFA_WEn
EMIFA_WAIT0
EXP_EMIFA_CS0n
EMIFA_BA0
EMIFA_BA1
EMIFA_A1
EMIFA_A2
EMIFA_A7
EMIFA_A9
EMIFA_A11
EXP_RESETn
EXP3_SEL_MEM_CTL
EXP3_SEL_MEM_CTL2
EXP3_EMIFA_WEL_DQM0
EXP3_EMIFA_WEL_DQM1
EMIFA_SDCKE
EXP_EMIFA_CS4n
EXP_EMIFA_CS5n
EMIFA_CS2n
EXP3_EMIFA_CS3n
EMIFA_A0
EMIFA_A4
EMIFA_A6
EMIFA_A8
EMIFA_A10
EMIFA_A12


SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: CORE POWER
Size B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 30 of 32
TPS65023
U44
L15
B1M41P750SPT
L16
L17
L18
2.2uH
SW4
PUSHBUTTON SW
HOT_RESETn
PWR_PAD
I2C0_SDA 4,16,22,24,27,28
I2C0_SCL 4,16,22,24,27,28
SYS_RESETn 31
ENABLE_1V2 31
ENABLE_1V8 31
ENABLE_3V3 31
VRTC
VLDO1
VLDO2
CPU_RTC_1V8
HB_RESET 31

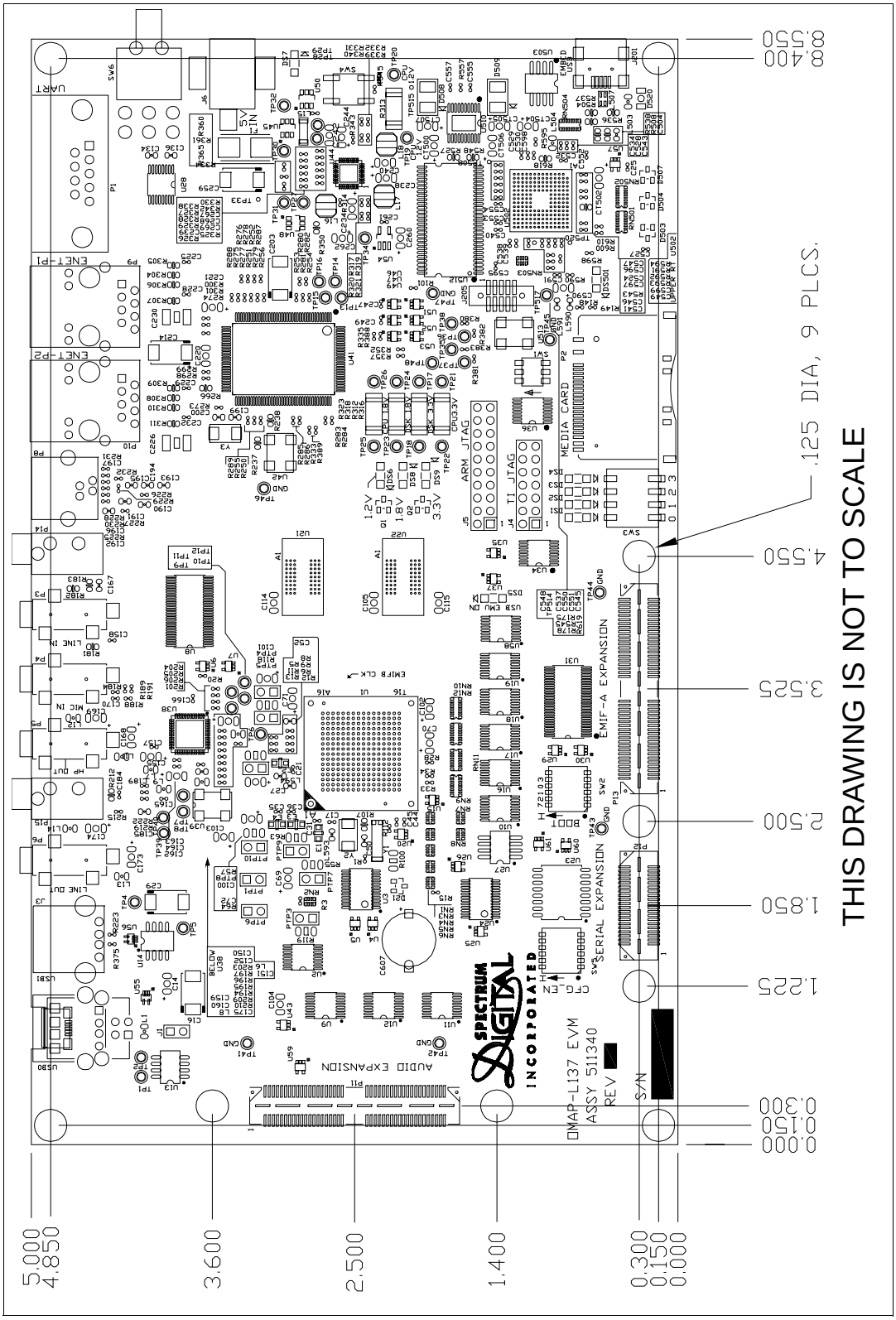

SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: POWER IN
Size: B
DWG NO 511342-0001
Revision: B
Date: Monday, November 24, 2008
Sheet 31 of 32
CPU_RESET 10,14
AIC3106_RESETn 22
ENET_RESET 24
EXP_RESETn 27,28,29
PONRSnIN 21
BOOT_DISABLE 2,3,14,16,19
BOOT_DISABLEn 2,3,4,5,8,16,19,27
21 ARM_RSTn
21 XRSn
30 SYS_RESETn
30 PB_RESET
ENABLE_1V2 30
ENABLE_1V8 30
ENABLE_3V3 30
DSK_1V2_SYS_OKAY
DSK_1V8_SYS_OKAY
DSK_3V3_SYS_OKAY
CPU_RESET
CPU_1V2
DSK_1V8
DSK_3V3
ALT_3V3
U45
U46
U47
U48
U49
U50
U51
U52
U53
TPS3808G09DBVRG4
SN74AHC14DCKRG4
Reset Threshold 0.84 Volts
R347 0
R348 10K 1%
R349 10K
R350 4.99K
R351 10K 1%
R352 33
R353 10K
R354 33
R355 20K
R356 10K 1%
R357 33
R358 33
R359 NO-POP
R360 NO-POP
R361 NO-POP
R362 NO-POP
R363 2.2K
R364 NO-POP
R365 NO-POP
R334 NO-POP
R335 10K
R336 0
C246 0.1uF
C247 0.1uF
C248 0.1uF
C249 0.1uF
C250 0.1uF
C251 0.1uF
C252 0.1uF
C253 0.1uF
C254 0.1uF
C255 .1uF
C256 0.1uF
C257 0.1uF
C258 1uF
TP30
TP31
TP32
TP47 TP
TP48 TP


SPECTRUM DIGITAL INCORPORATED
Title: OMAP-L137 EVM
Page Contents: POWER IN
Size:B DWG NO 511342-0001 Revision: B
Date: Monday, November 24, 2008 Sheet 32 of 32
Mounting holes 0.250 pad 0.125 drill
Z7 Z8 Z9 Z10
VCC_5V R370 360 DS8 LED GRN Q2 FJV3109R
R371 1K VCC_1V8
VCC_5V R367 360 DS6 LED GRN Q1 FJV3109R
R369 1K VCC_1V2
VCC_3V3 R374 220 DS9 LED GRN
VCC_5V C259 47uF
TP33 TP-30 R368 220 DS7 LED GRN
SW6 SWITCH
F1 F_4.0A R366 NO_POP
D1 SMCJ6.5
J6 CENTER SHUNT SLEEVE 2.5 MM JACK RASM712
SILKSCREEN: 5V IN
ALTERNATE 1.2V Power Supply
TP34 TP
ALT_CPU_1V2
C262 10uF
C261 5.6pF
R372 15K 1%
R373 220K 1%
U54 TPS79901-ADJ VIN VOUT FB GND EN
C260 10uF
VLDO2
Vout = ((R1+R2)/R2) *1.193
TP46 TP
TP45 TP
TP44 TP
TP43 TP
TP42 TP
TP41 TP

Appendix B

Mechanical Information

This appendix contains the mechanical information about the OMAP-L137 EVM produced by Spectrum Digital.


THIS DRAWING IS NOT TO SCALE
.125 DIA, 9 PLCS.
0.000
0.150
0.300
1.250
1.850
2.500
3.250
4.050
4.400
4.550
0.000
0.300
1.400
2.500
3.600
4.850
5.000
OMAP-L137 EVM
ASSY 511340
REV
S/N
SPECTRUM DIGITAL INCORPORATED
AUDIO EXPANSION
SERIAL EXPANSION
EMIF-A EXPANSION
MEDIA CARD
ARM JTAG
TI JTAG
ENET-P1
ENET-P2
UART
LINE IN
MIC IN
HP OUT
LINE OUT

[redacted]

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Printed in U.S.A., November 2008
511345-0001 Rev A