LTC2757
18-Bit, Parallel Input, SoftSpan I_{OUT} DAC

DESCRIPTION

Demonstration circuit 1485A features the LTC®2757A single 18-bit SoftSpan™ I_{OUT} DAC with ±1LSB maximum INL. This device features six programmable output ranges: 0V to 5V, 0V to 10V, ± 5V, ±10V, ±2.5V and –2.5V to 7.5V. The demo circuit allows all of the LTC2757's features to be exercised, including system-level gain and offset adjustments.

Design files for this circuit board are available at http://www.linear.com/demo

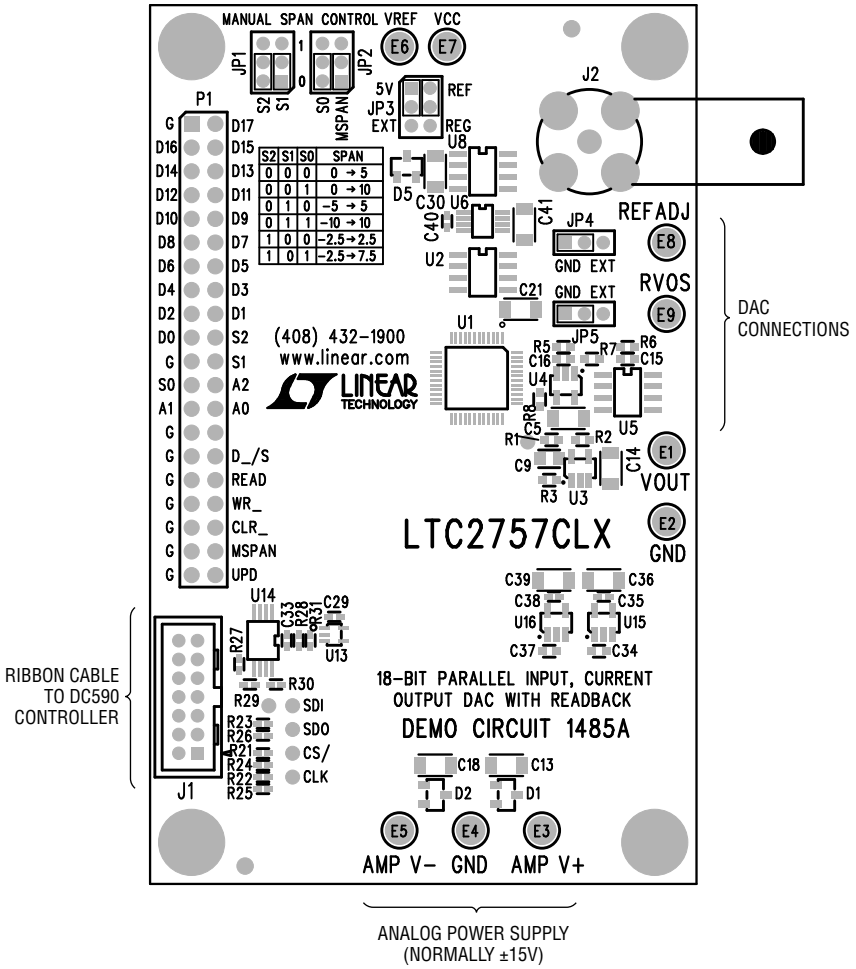
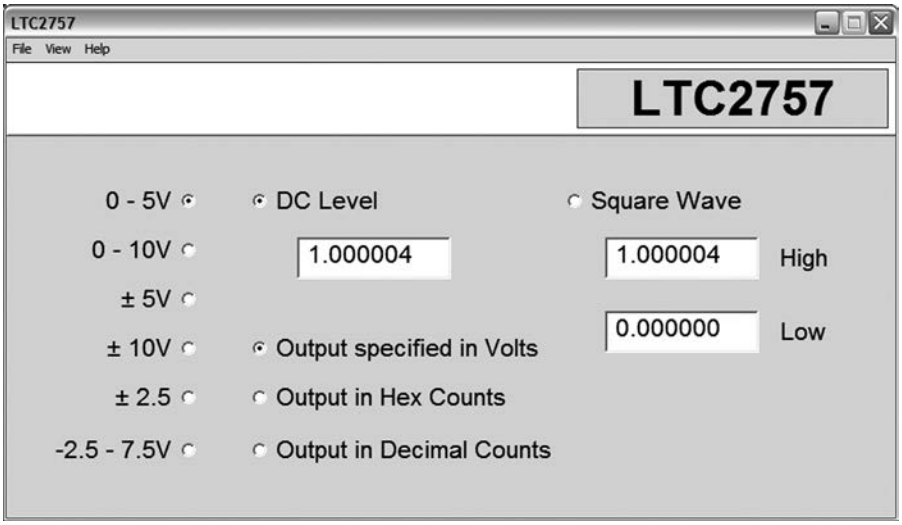


Figure 1. Connection Diagram

QUICK START PROCEDURE

Connect a clean ±15V power supply to the turret posts at the bottom of the DC1485A board. Connect J1 to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Connect DC590 to a host PC with a standard USB A/B cable. Run the QuikEval™ evaluation software which can be downloaded from www.linear.com/software. The correct control panel will be loaded automatically. The software automatically sets the LTC2757 outputs according to the entries in the control panel. A square wave option is available to test settling time. MSPAN jumper should be in the lower position if software span control is desired.

Additional software documentation may be available from the Help menu item, as features may be added periodically.



USING THE PARALLEL CONNECTOR

Protocol

The DC1485A can be used without the DC590 QuikEval system. If a DC590 demo board is not connected the shift registers on the DC1485A are disabled, allowing the user to clock in data through the parallel connector (P1).

The data input register is loaded directly from the 18-bit microprocessor bus (D0-D17 on the parallel connector) by holding the D_/S pin low and then pulsing the WR_ pin low. The second register (DAC register) is loaded by pulsing the UPD pin high, which copies the data held in the input register into the DAC register. Note that updates always include both data and span; but the DAC register values will not change unless the input register values have been changed by writing.

Loading the span input register is accomplished in a similar manner, by holding the D_/S pin high and then bringing the WR_ pin low. The span and data register structures are the same except for the number of parallel bits. The span registers have three bits, while the data registers have 18 bits.

Please see the LTC2757 data sheet for in depth timing diagrams and more information about the communication protocol.

Parallel Pin Descriptions

D0-D17: DAC Input/Output Data Bits. These I/O pins set and read back the DAC code. D17 is the MSB. D0 is the LSB.

S0-S2: Span Input/Output. Pins S0, S1 and S2 are used to program and to read back the output range of the DAC.

D_/S: Data/Span Select: This pin is used to select activation of the data or span I/O pins (D0 to D17 or S0 to S2, respectively), along with their respective dedicated registers, for write or read operations. Update operations ignore D_/S, since all updates affect both data and span registers. For single-span operation, tie D_/S to GND.

READ: Read Pin. When READ is asserted high, the data I/O pins (D0-D17) or span I/O pins (S0-S2) output the contents of the selected register. For single-span operation, readback of the span I/O pins is disabled.

UPD: Update and Buffer Select Pin. When READ is held low and UPD is asserted high, the contents of the input registers (both data and span) are copied into their respective DAC registers. The output of the DAC is updated, reflecting the new DAC register values. When READ is held high, the update function is disabled and the UPD pin functions as a buffer selector—logic low to select the input register, high for the DAC register.

WR_: Active Low Write Pin. A Write operation copies the data present on the data or span I/O pins (D0-D17 or S0-S2, respectively) into the input register. When READ is high, the Write function is disabled.

MSPAN: Manual Span Control Pin. MSPAN is used to configure the LTC2757 for operation in a single, fixed output range.

G: Ground Pin. (Note, if an IDE cable is used, Pin 21 is often keyed on the connector and may be trimmed.)

HARDWARE SETUP

Jumpers

MSPAN: Manual Span Control Pin. MSPAN is used to configure the LTC2757 for operation in a single, fixed output range. If MSPAN is high it will be configured for single-span use. If MSPAN is low it will be set through the QuikEval Software. Default position is 0 (low).

S0, S1, S2: Used to set the fixed output range if MSPAN is high. Default position is 0, 0, 0 (0V to 5V).

S2	S1	S0	SPAN
0	0	0	0V to 5V
0	0	1	0V to 10V
0	1	0	±5V
0	1	1	±10V
1	0	0	±2.5 V
1	0	1	–2.5V to 7.5V

REFADJ: Gain Adjust Pin. If no adjustments are required, select GND. Selecting EXT connects the pin to the turret allowing external adjustment to null gain error or compensate for reference errors.

RVOS: Offset adjustment for DAC. If no offset adjustment is required, select GND. Selecting EXT connects the offset pin to the turret allowing external adjustment of offset.

V_{CC}: Select source for 5V V_{CC} supply. Set to 5V for supply by onboard LT1236 reference (recommended). Set to REG to be supplied by regulated supply from DC590 Controller and remove the jumper to supply externally.

Analog Connections (Turret Posts)

V_{OUT}: DAC Voltage Output.

V_{REF}: DAC Reference Voltage. If the onboard LT1236 references are selected, the voltage may be measured at these points. If a remote reference is selected, then an external reference must be applied to these points.

RVOS: DAC Offset Adjust Input. Use only if RVOS jumper is set to EXT. Nominal input range is ±5V.

REFADJ: Gain Adjust Pin. This voltage-control pin can be used to null gain error or to compensate for reference errors. The gain error change expressed in LSB is the same for any output range.

Power and Ground Connections

Analog Power: The 15V, –15V and GND turret posts are the analog supplies for the internal DAC amplifiers. These should be connected to a well regulated, low noise power supply.

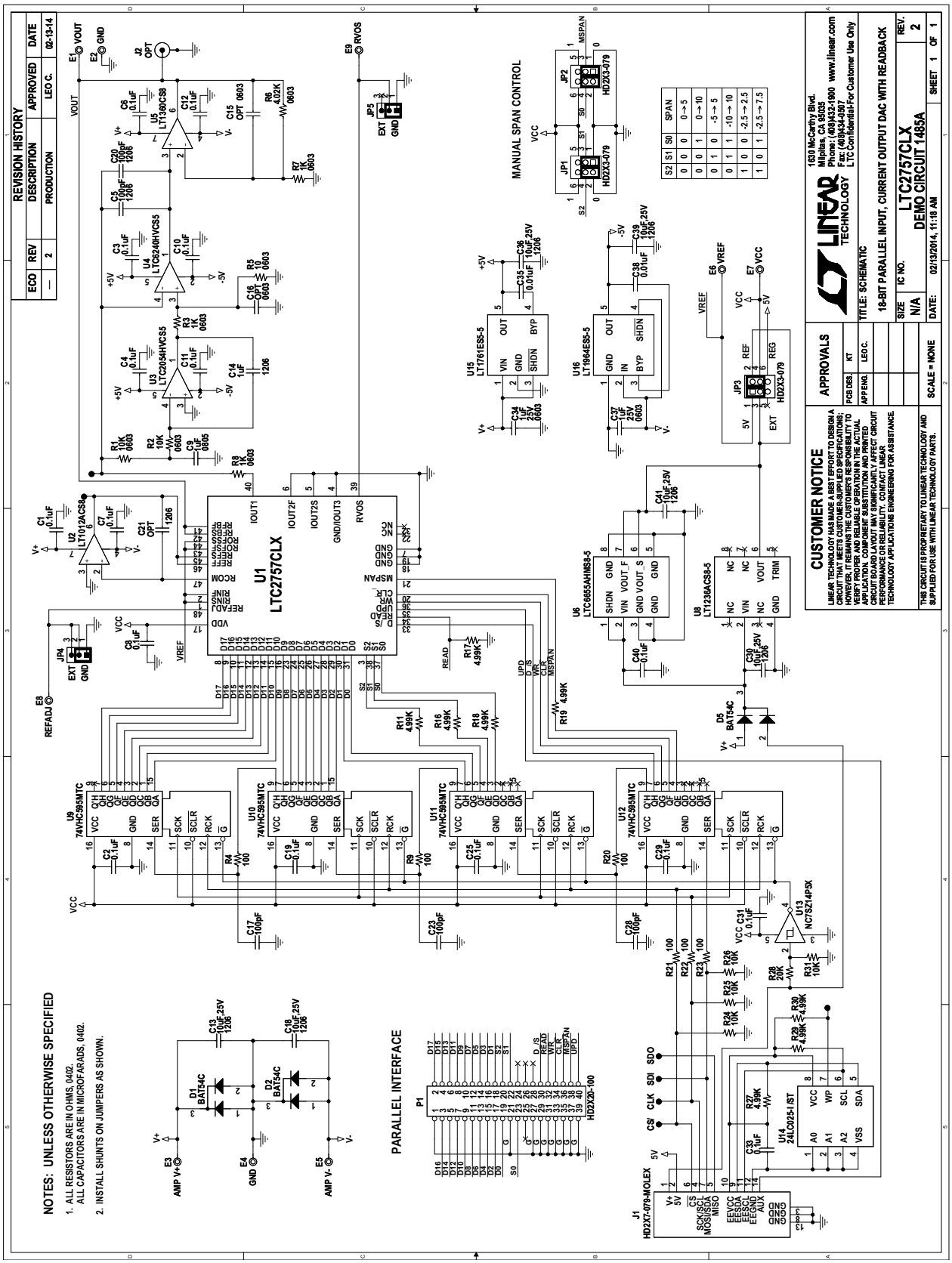
V_{CC}: Connection to V_{CC}. See schematic and description for V_{CC} jumper.

Grounding: Separate power and signal grounds are provided. Signal GND is the turret closest to V_{OUT}, use this for measurement ground and output return. Power GND is between AMP V^+ and AMP V^- turrets.

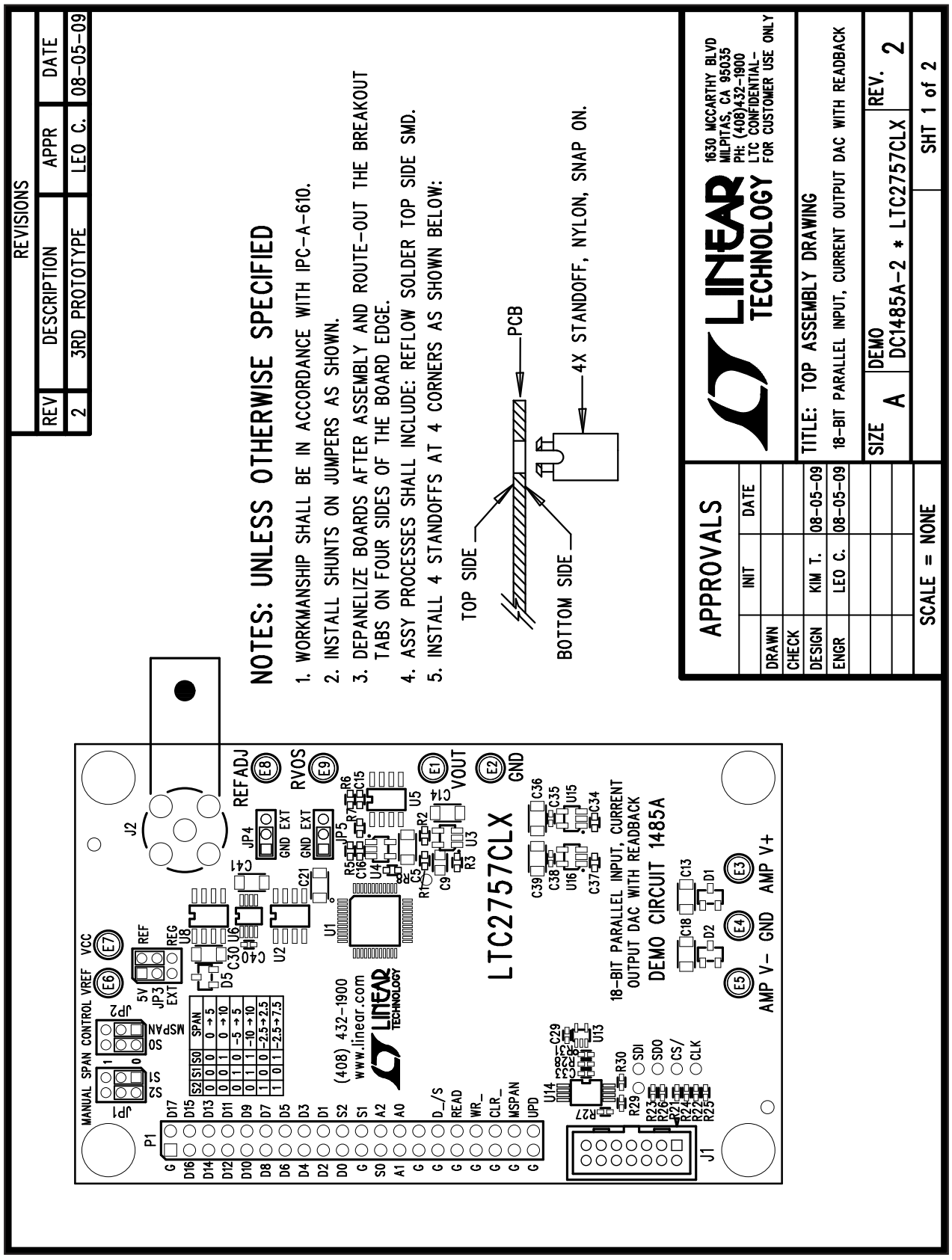
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURE/PART NUMBER	KIT QTY
				NUMBER OF BOARDS =	175
1	16	C1-C4, C6-C8, C10-C12, C19, C25, C29, C31, C33, C40	CAP., X5R, 0.1µF 25V 20%, 0402	TDK, C1005X5R1E104M	2800
2	2	C5, C20	CAP., NP0, 100pF 50V, 5%,1206	AVX, 12065A101JAT2A	350
3	1	C9	CAP., X7R, 1µF 25V 10%, 0805	TDK, C2012X7R1E105K	175
4	2	C34, C37	CAP., X5R, 1µF 25V 20%, 0603	TDK, C1608X5R1E105M	350
5	6	C13, C18, C30, C36, C39, C41	CAP., X5R, 10µF 25V 20%,1206	TDK, C3216X5R1E106M	1050
6	1	C14	CAP., X7R, 1µF 25V 10%,1206	AVX, 12063C105KAT2A	175
7	0	C15, C16	CAP., 0603	OPT	0
8	0	C21	CAP., 1206	OPT	0
9	3	C17, C23, C28	CAP., NP0, 100pF 50V, 5%,0402	AVX, 04025A101JAT2A	525
10	2	C38, C35	CAP., X7R, 0.01µF 25V 20%,0402	TDK, C1005X7R1E103M	350
11	3	D1, D2, D5	DIODE, SCHOTTKY, SOT23	DIODES INC., BAT54C-7-F	525
12	9	E1, E2, E3, E4, E5, E6, E7, E8, E9	TEST POINT, TURRET, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0	1575
13	3	JP1, JP2, JP3	JMP, 2X3, 0.079"	SAMTEC, TMM-103-02-L-D	525
14	2	JP4, JP5	JMP, 1X3, 0.079"	SAMTEC, TMM-103-02-L-S	350
15	1	J1	HEADER, 2X7 PIN, 0.079CC	MOLEX, 87831-1420	175
16	0	J2	CONN, BNC, RTANG 50Ω	OPT (TYCO ELEC. AMP, 413631-1)	0
17	1	P1	JMP, 2X20, 0.100"	SAMTEC, TSW-120-07-L-D	175
18	2	R1, R2	RES., Chip 10k 1/16W 5%, 0603	VISHAY, CRCW060310K0JNEA	350
19	3	R7, R8, R3	RES., Chip 1k 1/16W 5%, 0603	VISHAY, CRCW06031K00JNEA	525
20	6	R4, R9, R20, R21, R22, R23	RES., Chip 100Ω 1/16W 5%, 0402	VISHAY, CRCW0402100RJNED	1050
21	1	R5	RES., Chip 10Ω 1/16W 5%, 0603	VISHAY, CRCW060310R0JNEA	175
22	1	R6	RES., Chip 4.02k 1/16W 1%, 0603	VISHAY, CRCW06024K02FKED	175
23	8	R11, R16, R17, R18, R19, R27, R29, R30	RES., Chip 4.99k 1/16W 1%, 0402	VISHAY, CRCW04024K99FKED	1400
24	4	R24, R25 ,R26, R31	RES., Chip 10k 1/16W 5%,0402	VISHAY, CRCW040210K0JNED	700
25	1	R28	RES., Chip 20k 1/16W 5%,0402	VISHAY, CRCW040220K0JNED	175
26	1	U1	I.C., LTC2757ACLX, LQFP48LX	LINEAR TECH., LTC2757ACLX	175
27	1	U2	I.C., LT1012ACS8, SO8	LINEAR TECH., LT1012ACS8	175
28	1	U3	I.C., LTC2054HVCS5, SOT23-5	LINEAR TECH., LTC2054HVCS5	175
29	1	U4	I.C., LTC6240HVCS5, SOT23-5	LINEAR TECH., LTC6240HVCS5	175
30	1	U5	I.C., LT1360CS8, SO8	LINEAR TECH., LT1360CS8	175
31	0	U6	I.C., LTC6655AHMS8-5, MSOP8	OPT	0
32	1	U8	I.C., LT1236ACS8-5, SO8	LINEAR TECH., LT1236ACS8-5	175
32	4	U9, U10, U11, U12	I.C., 74VHC595MTC, TSSOP16	FAIRCHILD SEMI., 74VHC595MTCX	700
33	1	U13	I.C., NC7SZ14P5X, SC70-5	FAIRCHILD SEMI., NC7SZ14P5X	175
34	1	U14	I.C., Serial EEPROM, TSSOP8	MICROCHIP, 24LC025-I/ST	175
35	1	U15	I.C., LT1761ES5-5, SOT23-5	LINEAR TECH., LT1761ES5-5	175
36	1	U16	I.C., LT1964ES5-5, SOT23-5	LINEAR TECH., LT1964ES5-5	175
37	8	SHUNTS AS SHOWN ON ASSY DWG	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G	1400
38	4	MTG	STAND-OFF, NYLON (SNAP ON), 0.50" TALL	KEYSTONE, 8833 (SNAP ON)	700
39	2		STENCILS BOTH SIDES	DC1485A-1	2

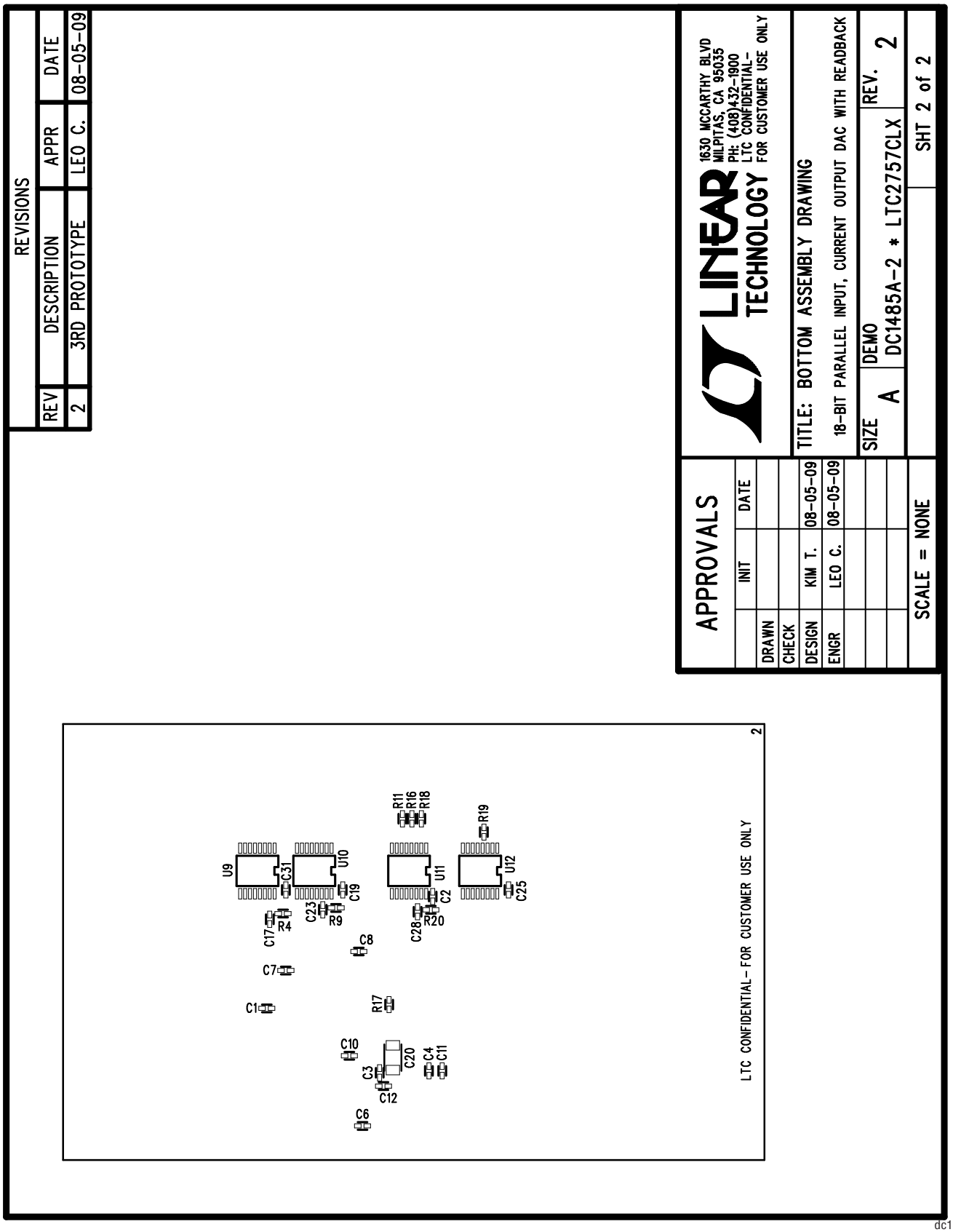
SCHEMATIC DIAGRAM



ASSEMBLY DRAWINGS

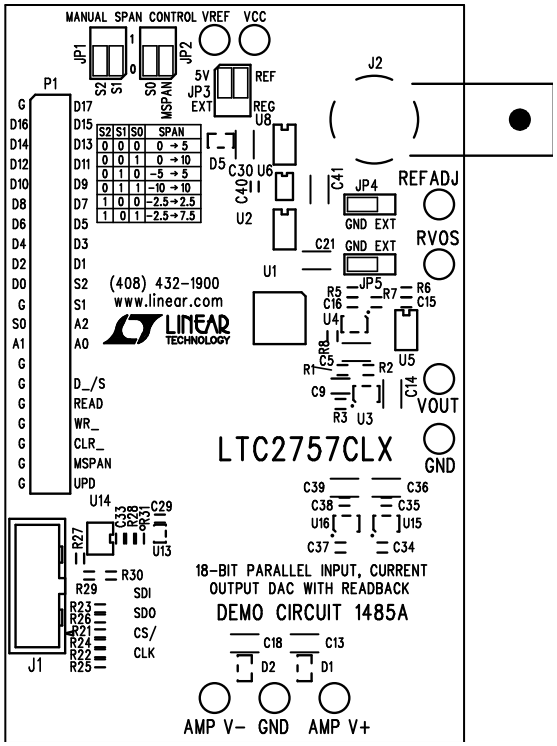


ASSEMBLY DRAWINGS

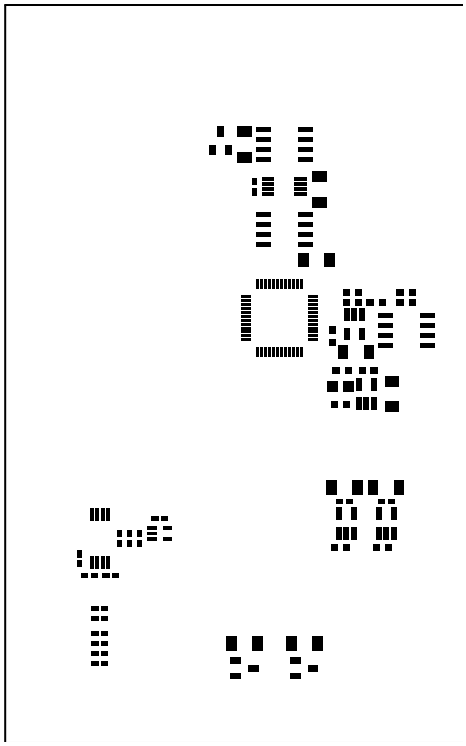


PCB LAYOUT AND FILM

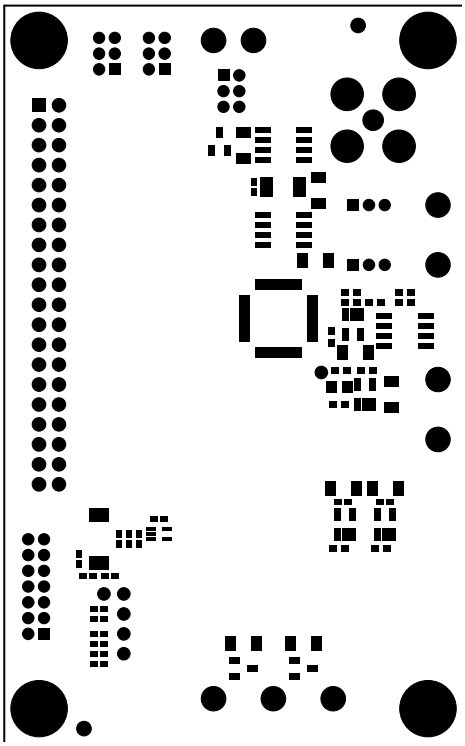
Top Silkscreen



Top Solder Paste

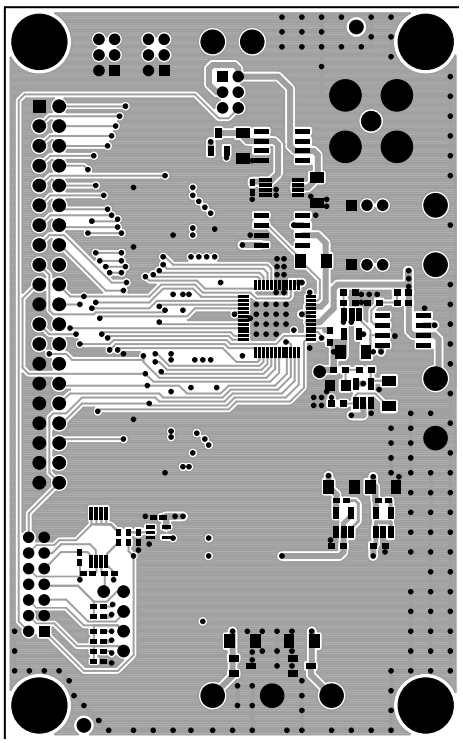


Top Solder Mask

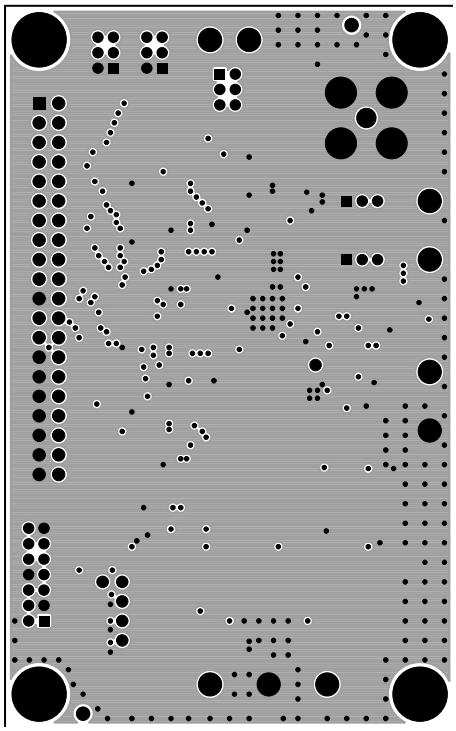


PCB LAYOUT AND FILM

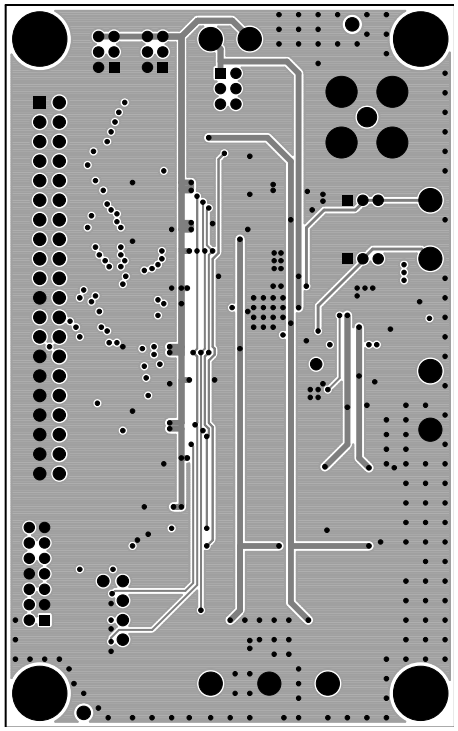
Layer 1-Top Layer



Layer 2-GND Plane 1

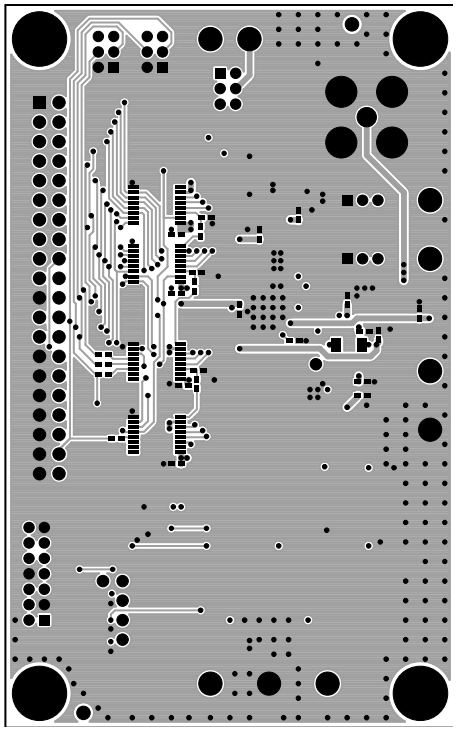


Layer 3- GND Plane 2 + PWR Traces

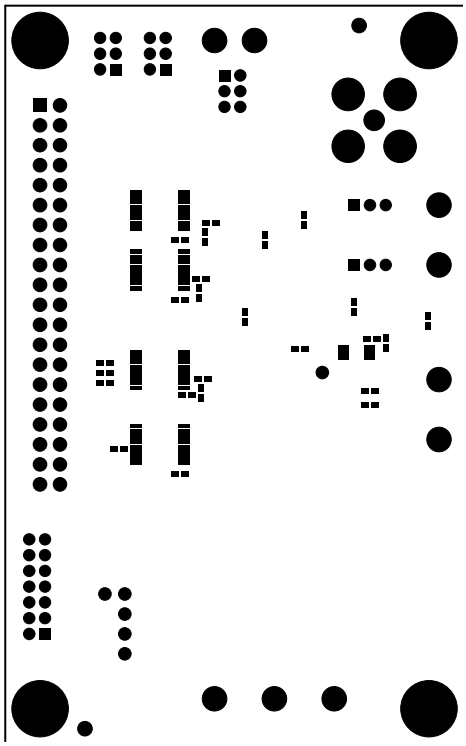


PCB LAYOUT AND FILM

Layer 4-Bottom Layer

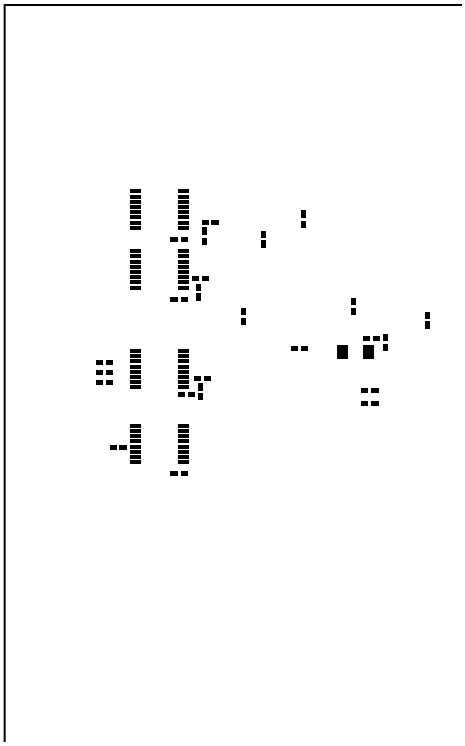


Bottom Solder Mask

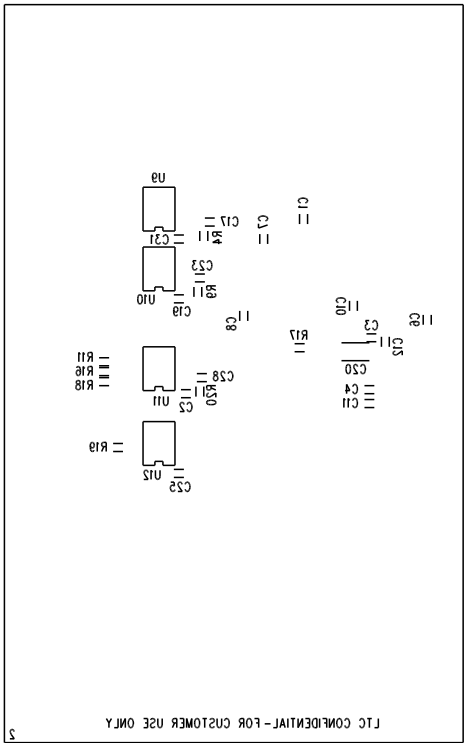


PCB LAYOUT AND FILM

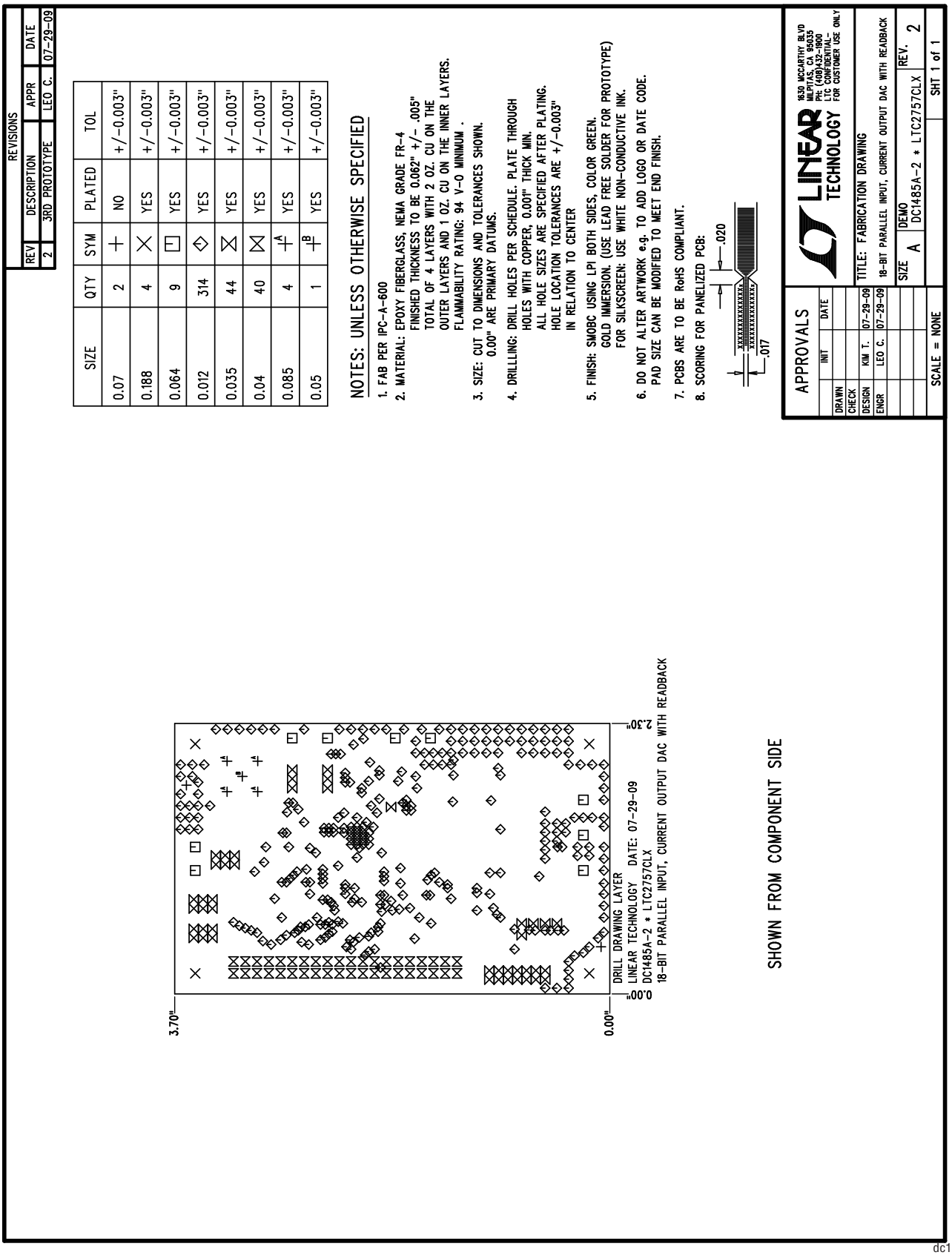
Bottom Solder Paste



Bottom Silkscreen



PC FAB DRAWING



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