FAIRCHILD

SEMICONDUCTOR®

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SG6510X1 — PC Power Supply Supervisors

Features

- Over-Voltage Protection (OVP) for 3.3V, 5V, 12V
- Under-Voltage Sense (UVS) and Under-Voltage Protection (UVP) for 3.3V, 5V
- Open-Drain Output for PGO and FPO Pins
- 300ms Power-Good Delay
- 75ms Turn-on Delay for 3.3V and 5V
- 2.8ms PSON Control to FPO Turn-off Delay
- 38ms /38ms PSON Control Debounce
- 350µs Width Noise Deglitches
- 2ms UVP Debounce Time
- 1ms UVS Debounce Time
- No Lockup During the Fast AC Power On/Off
- Brownout Protection Function for 3.3V and 5V
- Wide Supply Voltage Range from 4V to 15V

Description

SG6510 is designed to provide the voltage supervisor function, remote on/off PSON function, power-good (PGO) indicator function, and fault protection (FPO) function for switching power systems.

For the supervisor function, it provides the over-voltage protection (OVP) monitoring for 3.3V, 5V, and 12V (12V via VDD pin); under-voltage sense (UVS) monitoring for 3.3V and 5V; and under-voltage protection (UVP) monitoring for 3.3V and 5V. When 3.3V or 5V voltage is decreasing to 2.8V and 4.2V, respectively, the under-voltage sense (UVS) function is enabled to reset the PGO signal from high to low. If 3.3V or 5V voltage is further decreasing to 2.5V and 3.6V, respectively, FPO is set high to turn off the PWM controller IC. To achieve better immunity for lighting surge glitch and to prevent accidental power shut down during dynamic loading condition, the debounce time for UVP and UVS is 2ms/1ms, respectively. The deglitch time for OVP is 75µs for better noise immunity. During an AC sag or brownout situation, UVP functions can still be enabled to protect power supply in case of output short circuit.

The power supply is turned on after 38ms debounce time when the PSON signal is set from high to low. To turn off the power supply, the PSON signal is set from low to high and the debounce time is 38ms. The PGI circuitry provides a sufficient power-down warning signal for PGO. When PGI input is lower than the internal 1.2V reference voltage, after 350µs debounce time, the PGO signal is pulled low.

Ordering Information

Part Number	Operating Temperature Range	Package	🍃 Eco Status	Packing Method
SG6510DY1	-40°C to +125°C	DIP-8	Green	Tube
SG6510DZ1	-40°C to +125°C	DIP-8	RoHS	Tube
SG6510SZ1	-40°C to +125°C	SOP-8	RoHS	Tape & Reel
SG6510SY1	-40°C to +125°C	SOP-8	Green	Tape & Reel

🍃 *For Fairchild's definition of "green" please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.*
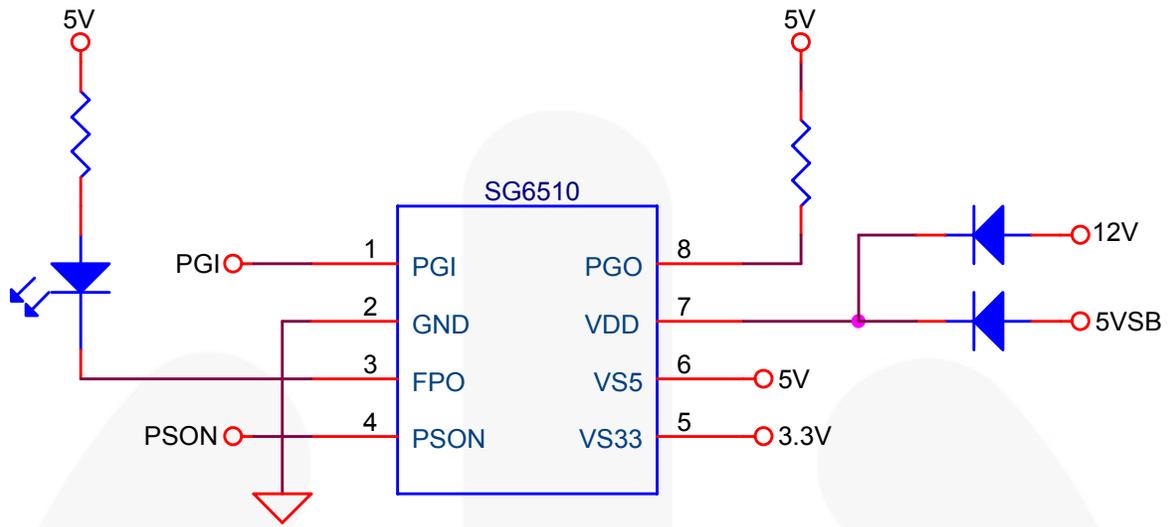
Application Diagram

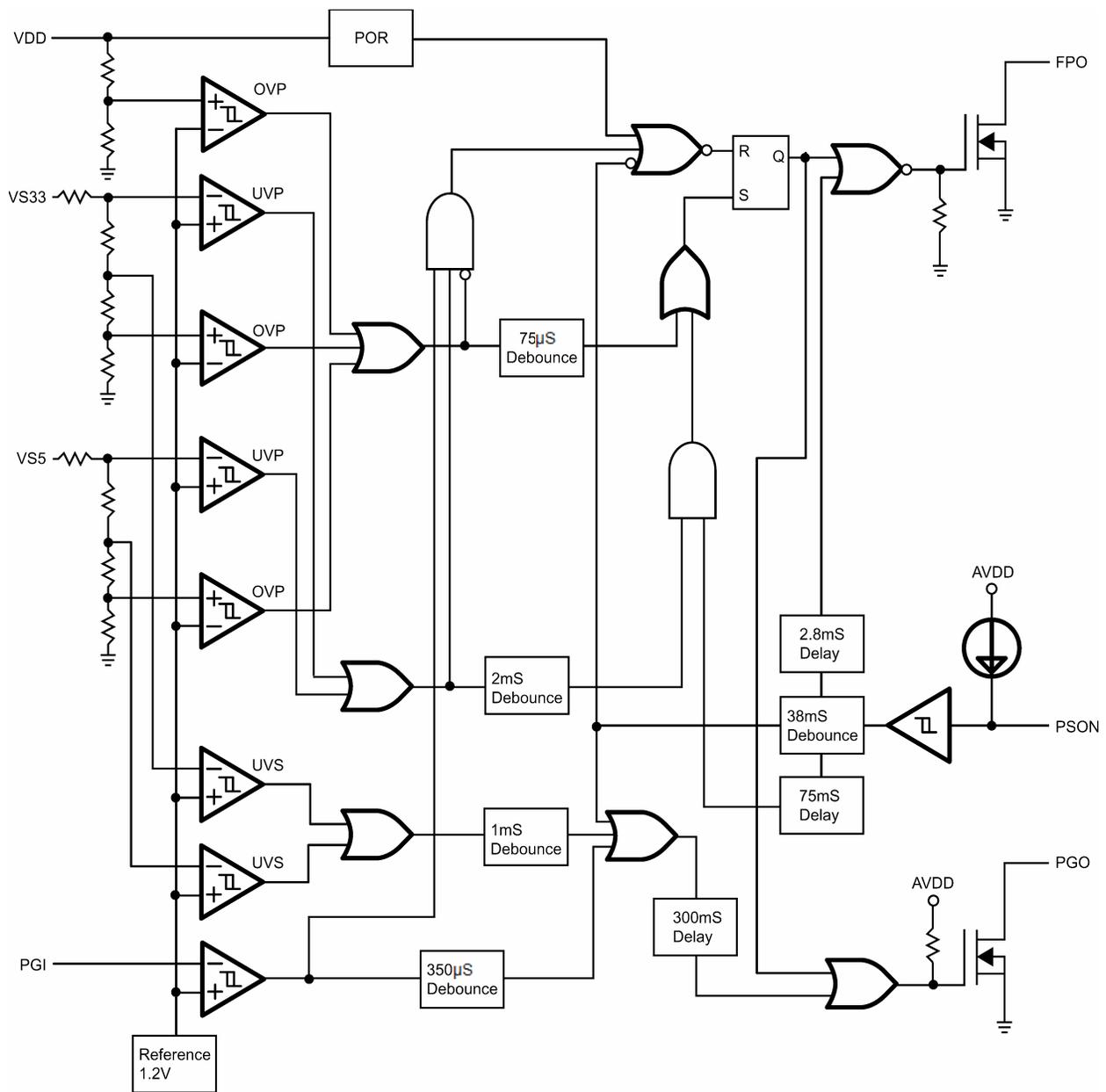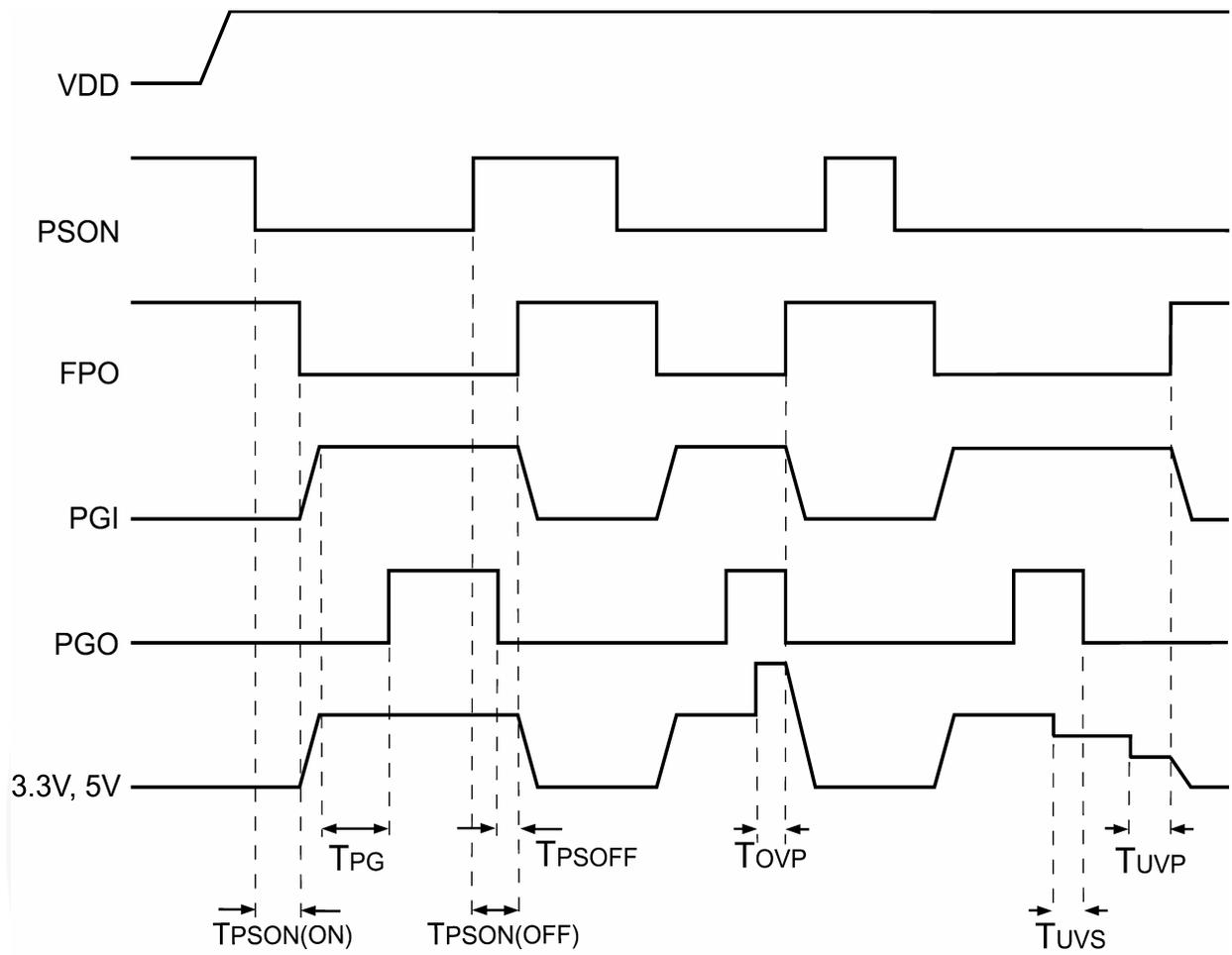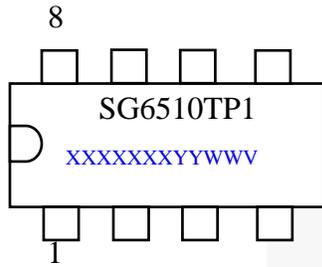**Figure 1.   Typical Application**

Internal Block Diagram

Figure 2.   Functional Block Diagram

Timing Diagram

Marking Information

8

SG6510TP1

XXXXXXXYYWWV

1

T: D = DIP
P: Z = Lead Free
    Null = regular package
XXXXXXX: Wafer Lot
YY: Year; WW: Week
V: Assembly Location

※ Marking for SG6510DZ1 (Pb-free)

   SG6510SZ1 (Pb-free)

𝟋 ZXYTT
6510
TP1M
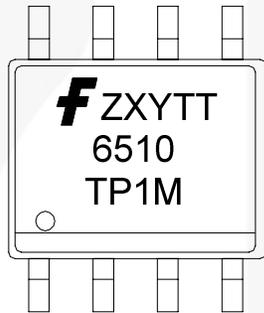
1'st line
Z: Assembly plant code
X: Year code
Y: Week code
TT: Die run code
3'rd line
T: Package type (D = DIP, S=SOP)
P: Y=Green package
M: Manufacture flow code

※ Marking for SG6510DY1 (Green-compound)
    SG6510SY1 (Green-compound)

Figure 3.   **Top Mark**

Pin Configurations

```
        ┌───────┐
  PGI ──┤1     8├── PGO
  GND ──┤2     7├── VDD
  FPO ──┤3     6├── VS5
 PSON ──┤4     5├── VS33
        └───────┘
```
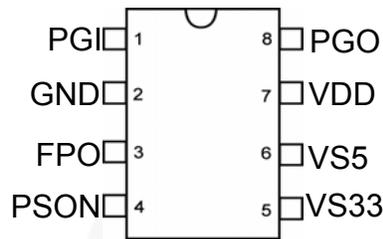
Figure 4.   Pin Configuration

Pin Definitions

Pin #	Name	Type	Description
1	PGI	Analog Input	Power-good input. For ATX SMPS, it detects main AC voltage under-voltage and/or failure.
2	GND	Supply	Ground.
3	FPO	Logic Output	Fault protection output (invert). Output signal to control the PWM IC. For example, it controls the PWM IC of primary side through an opto-coupler. When FPO is low, the main SMPS is operational.
4	PSON	Logic Input	Remote on/off logic input from CPU or main-board. Turn on/off the PWM output after a 38ms delay.
5	VS33	Analog Input	3.3 V over/under-voltage control sense input.
6	VS5	Analog Input	5 V over/under-voltage control sense input.
7	VDD	Supply	Supply voltage; 4V ~ 15V. For ATX SMPS, it is connected to 5V-standby and 12V through diodes, respectively.
8	PGO	Logic Output	Power-good logic output, 0 or 1(open-drain). Power good = 1 means that the power is good for operation. The power-good delay is 300ms.

Function Table

PGI	PSON	UV Sense (3.3V or 5V)	UV Protection (3.3V or 5V)	OV Protection	FPO	PGO
PGI<1.2V	L	No	No	No	L	L
PGI<1.2V	L	Yes	No	No	L	L
PGI<1.2V	L	No	Yes	No	L	L
PGI<1.2V	L	No	No	Yes	H	L
PGI<1.2V	L	Yes	Yes	No	L	L
PGI<1.2V	L	Yes	No	Yes	H	L
PGI<1.2V	L	No	Yes	Yes	H	L
PGI<1.2V	L	Yes	Yes	Yes	H	L
PGI>1.2V	L	No	No	No	L	H
PGI>1.2V	L	Yes	No	No	L	L
PGI>1.2V	L	No	Yes	No	H	L
PGI>1.2V	L	No	No	Yes	H	L
PGI>1.2V	L	Yes	Yes	No	H	L
PGI>1.2V	L	Yes	No	Yes	H	L
PGI>1.2V	L	No	Yes	Yes	H	L
PGI>1.2V	L	Yes	Yes	Yes	H	L
X	H	X	X	X	H	L

X = Don't care

FPO = L means: fault IS NOT latched

FPO = H means: fault IS latched

PGO = L means: fault

PGO = H means: No fault

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage		-0.3	16	V
V_i	Input Voltage	PSON, VS33, VS5, PGI	-0.3	8.0	V
V_{OUT}	Output Voltage	FPO	-0.3	16	V
		PGO	-0.3	8.0	V
TA	Operating Free Air Temperature Range		-40	+85	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
T_L	Soldering Temperature			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model		2	KV

Note:
1. Stresses above those listed may cause permanent damage to the device.

Recommended Operating Conditions

| Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage		4	15	V
V_{IL}	Input Voltage	PSON, VS33, VS5, PGI		7	V
V_{OUT}	Output Voltage	FPO		15	V
		PGO		7	
I_{oSINK}	Output Sink Current	FPO		20	mA
		PGO		10	
T_R	Supply Voltage Rising Time[2]		1		ms
T_A	Operating Free Air Temperature Range		-30	85	°C

Note:
2. V_{DD} rising and falling slew rate must be less than 14V/ms.

Electrical Characteristics

Unless otherwise noted, V_{DD}=12V and T_A=25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Over-Voltage Protection						
V_{OVP}	Over-Voltage Protection VS33		3.7	3.9	4.1	V
	Over-Voltage Protection VS5		5.7	6.1	6.5	
	Over-Voltage Protection V_{DD}		13.2	13.8	14.4	
I_{LKG}	Leakage Current (FPO)	V_{FPO} = 5V			5	µA
V_{OL}	Low-Level Output Voltage (FPO)	I_{sink} 20mA			0.7	V
$t_{D-VDDOVP}$	Timing, OVP to Protection		33	75	110	ms
Under-Voltage and PGI, PGO						
V_{PGI}	Input Threshold Voltage PGI		1.15	1.20	1.25	V
V_{UVS}	Under-Voltage Sense VS33		2.6	2.8	3.0	V
	Under-Voltage Sense VS5		4.0	4.2	4.4	
V_{UVP}	Under-Voltage Protection VS33		2.3	2.5	2.7	V
	Under-Voltage Protection VS5		3.4	3.6	3.8	
t_{UVS}	Timing UVS to Sense (PG)		0.6	1.0	1.5	ms
t_{UVP}	Timing UVP to Protection (FPO)		1.3	2.0	3.0	ms
I_{LKG}	Leakage Current (PGO)	PGO = 5V			5	µA
V_{OL}	Low-Level Output Voltage (PGO)	V_{DD} = 12V, I_{SINK} 10mA			0.7	V
t_{UVE}	Under-Voltage Enable Delay Time		49	75	114	ms
t_{PG}	Timing PG Delay	PGI to PGO	200	300	450	ms
	Noise Deglitch Time	PGI to PGO	200	350	450	µs
PSON Control						
I_{PSON}	Input Pull-up Current	PSON = 0V	100	160	220	µA
V_{IH}	High-Level Input Voltage		2.40	1.85		V
V_{IL}	Low-Level Input Voltage			1.35	1.2	V
t_{PSON}	Timing, PSON to On/Off	On	24	38	57	ms
		Off	24	38	57	
t_{PSOFF}	Timing PG Low to Power Off		1.6	2.8	4.5	ms
Total Device						
I_{DD}	Supply Current	PSON = 5V/V_{DD} = 5V		0.7	1.5	mA

Physical Dimensions
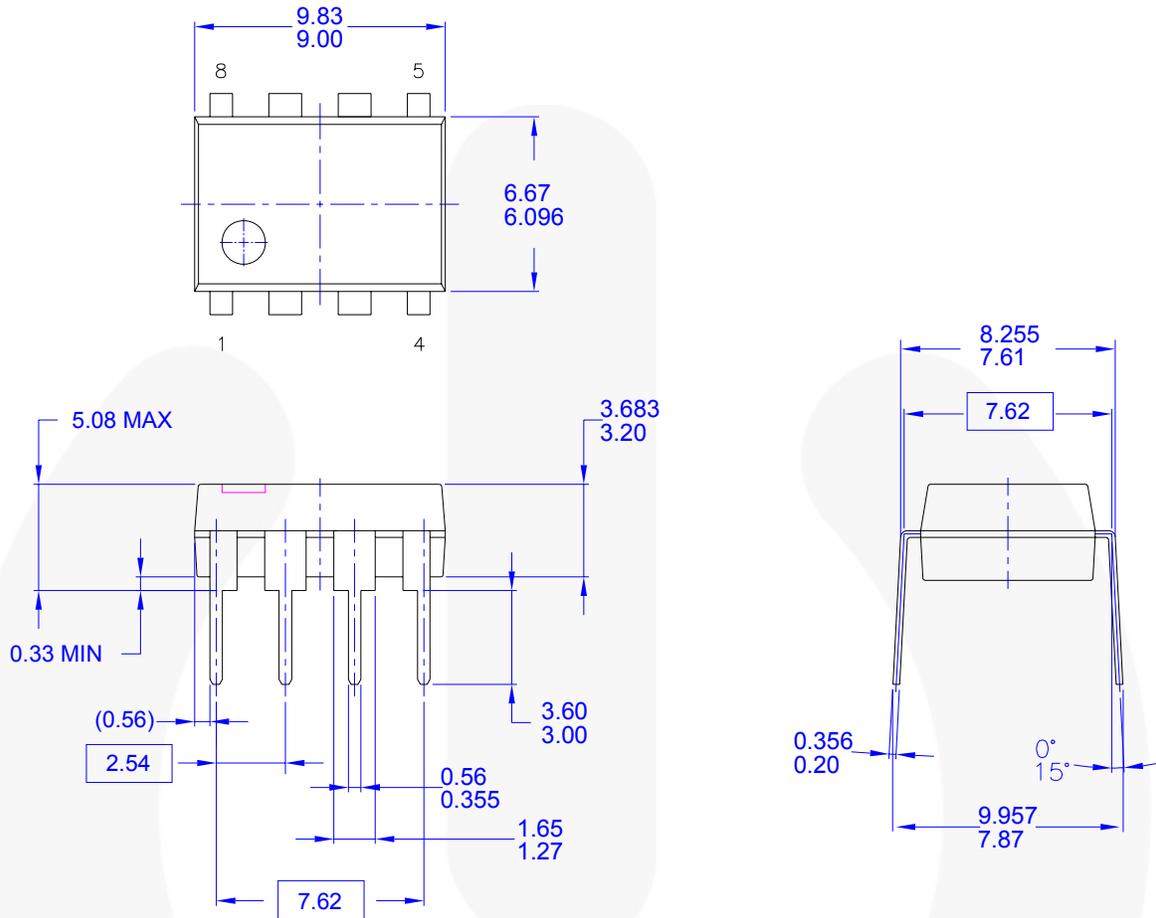
NOTES: UNLESS OTHERWISE SPECIFIED
   A) THIS PACKAGE CONFORMS TO
      JEDEC MS-001 VARIATION BA
   B) ALL DIMENSIONS ARE IN MILLIMETERS.
   C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
      MOLD FLASH, AND TIE BAR EXTRUSIONS.
   D) DIMENSIONS AND TOLERANCES PER
      ASME Y14.5M-1994
   E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 5.   8-Pin, DIP-8 Package

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Physical Dimensions (Continued)

5.00
4.80

A

3.81

8   5

B

6.20
5.80

4.00
3.80

PIN ONE
INDICATOR

1   4

(0.33)

1.27

⊕ | 0.25 Ⓜ | C | B | A

0.25
0.10

1.75 MAX

C

0.51
0.33

▱ | 0.10 | C

R0.10

R0.10

0.50
0.25 x 45°

GAGE PLANE

0.36

8°
0°

0.90
0.406

SEATING PLANE

(1.04)

DETAIL A
SCALE: 2:1

0.65

1.75

5.60

1.27

LAND PATTERN RECOMMENDATION

SEE DETAIL A

0.25
0.19

OPTION A - BEVEL EDGE

OPTION B - NO BEVEL EDGE

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC
   MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
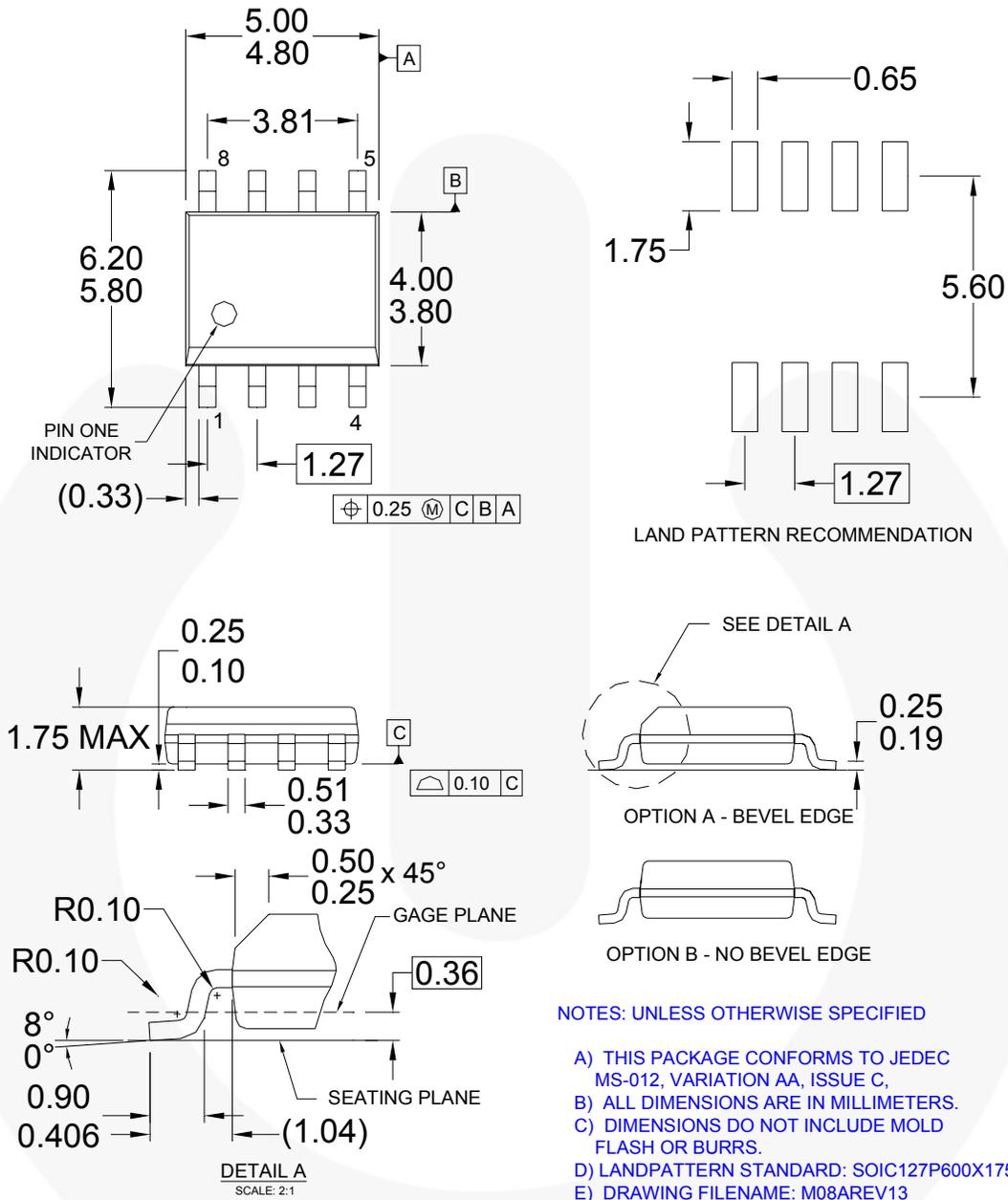E) DRAWING FILENAME: M08AREV13

Figure 6.   8-Pin SOP Package

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