



# MX574BBA805M664

Ultra-Low Jitter 805.664062MHz LVPECL XO

ClockWorks® FUSION

## General Description

The MX574BBA805M664 is an ultra-low phase jitter XO with LVPECL output optimized for high line rate applications.

## Applications

- Optical communications
- Forward error correction (FEC) rates
- FPGA SERDES reference clock

## Absolute Maximum Ratings

Supply Voltage (VIN).....+4.6V  
Lead Temperature (soldering, 10s).....260°C  
Storage Temperature (T<sub>s</sub>).....125°C  
ESD Rating (HBM).....2kV

## Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2V.<sup>1</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				120	mA
F0	Center Frequency			805.664062		MHz
	Frequency Stability	Note 2			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		142 103		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		85		350	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage	LVPECL output levels	VDD - 1.35	VDD - 1.01	VDD - 0.8	V
VOL	Output Low Voltage	LVPECL output levels	VDD - 2.0	VDD - 1.78	VDD - 1.6	V
Vswing	Peak to Peak Output Voltage Swing		0.65	0.77	0.95	V

### Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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June 06, 2017  
MX574BB1-5329

Revision 1.0  
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## Features

- 805.664062MHz LVPECL
- Supports FEC line rate
- Typical phase noise:
  - 103fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

## Operating Ratings

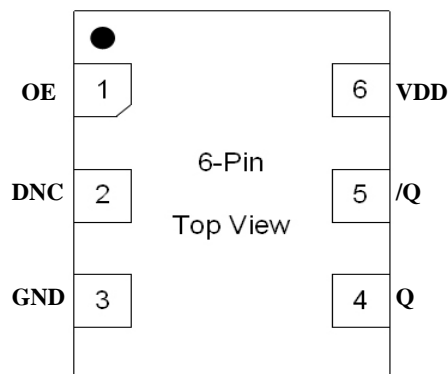
Supply Voltage (VIN).....+2.375V to +3.63V  
Ambient Temperature (TA).....-40°C to +85°C

## Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX574BBA805M664	MX574BB	A805M664	Tube	6-Pin 7mm x 5mm LGA
MX574BBA805M664-TR	MX574BB	A805M664	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

## Pin Configuration



## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVPECL	Clock Output Frequency = 805.664062MHz
6	VDD	PWR		Power Supply

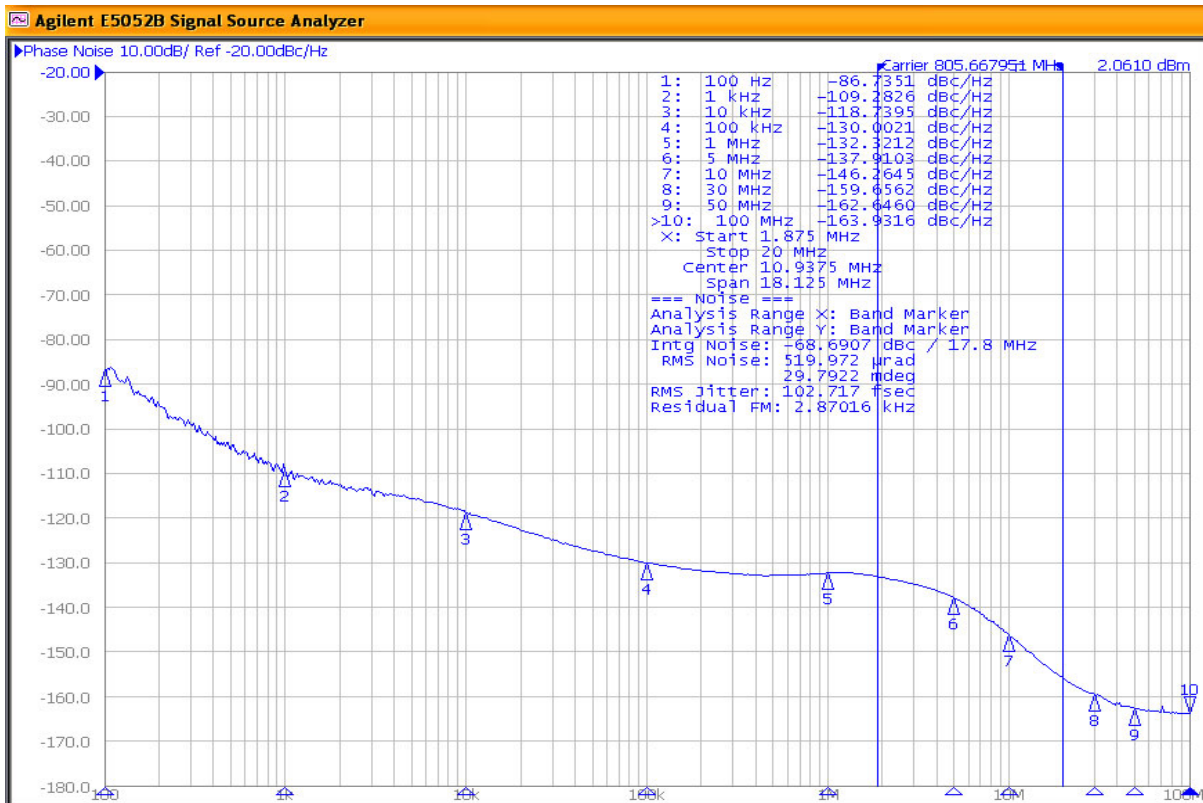


Figure 1. LVPECL Output 805.664062MHz 1.875MHz-20MHz 103fs

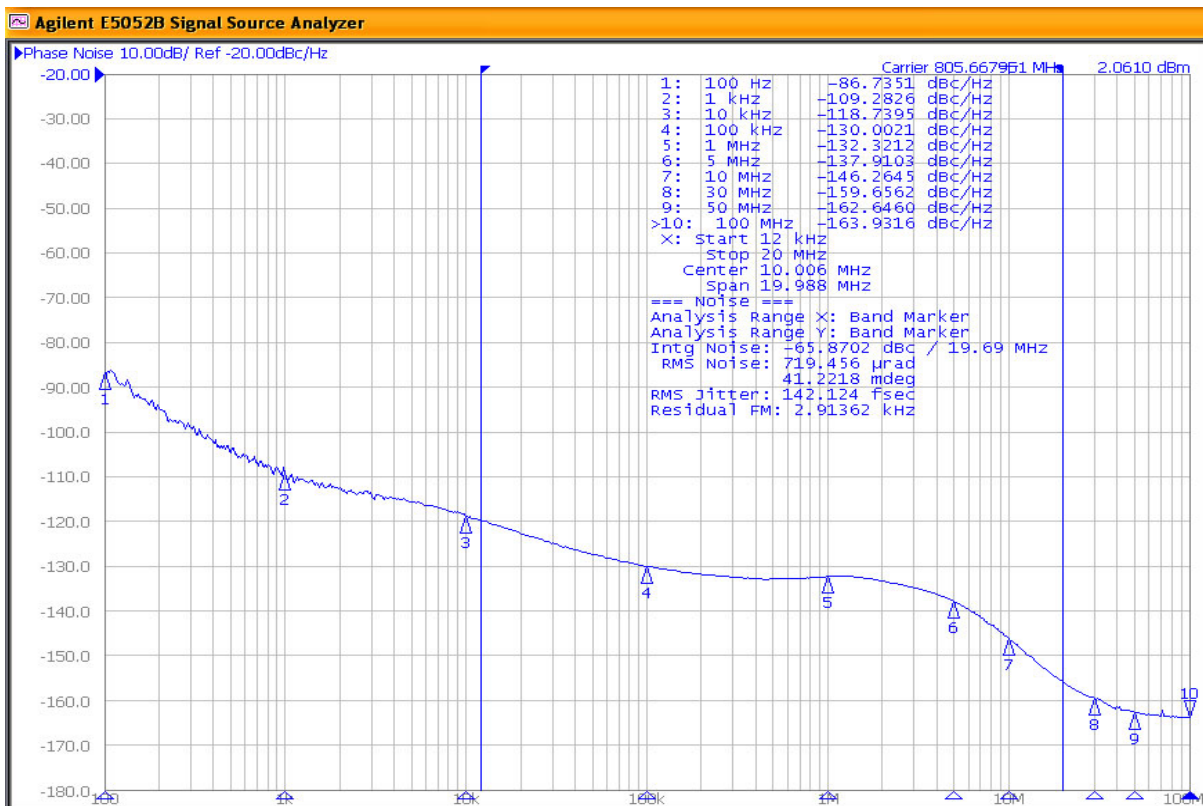


Figure 2. LVPECL Output 805.664062MHz 12kHz-20MHz 142fs

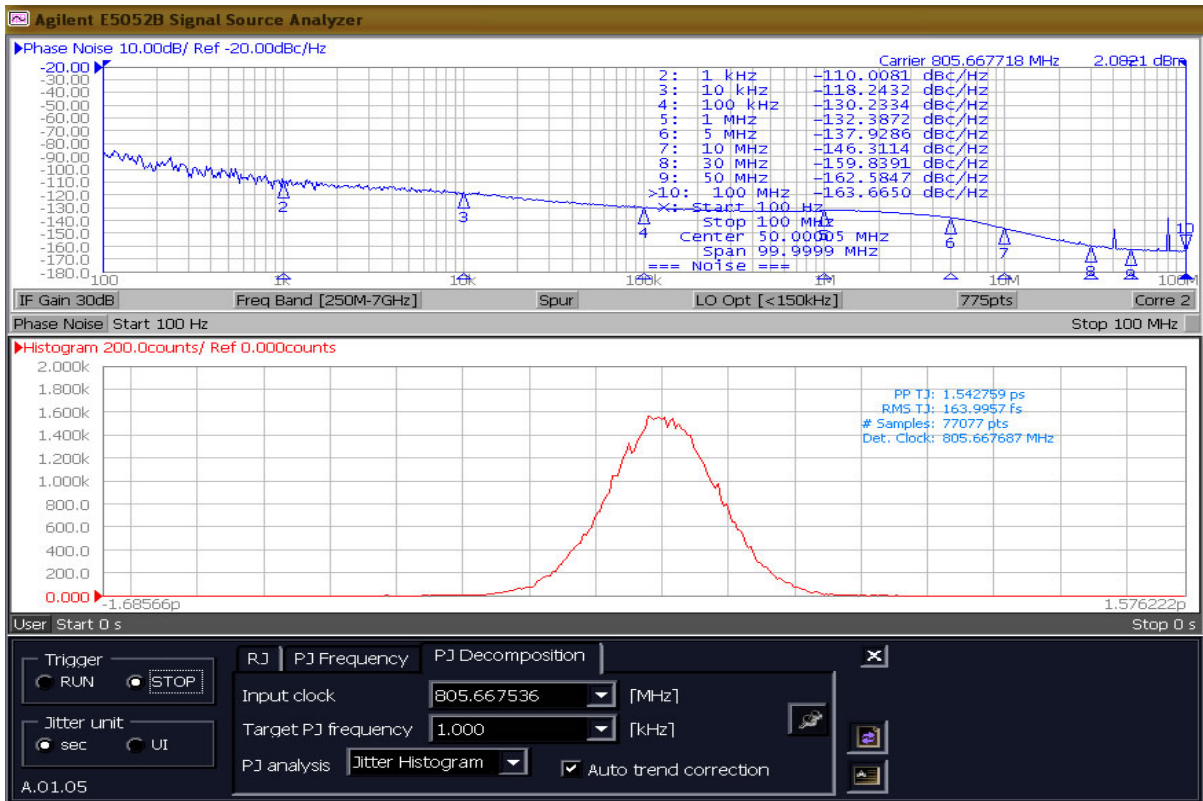
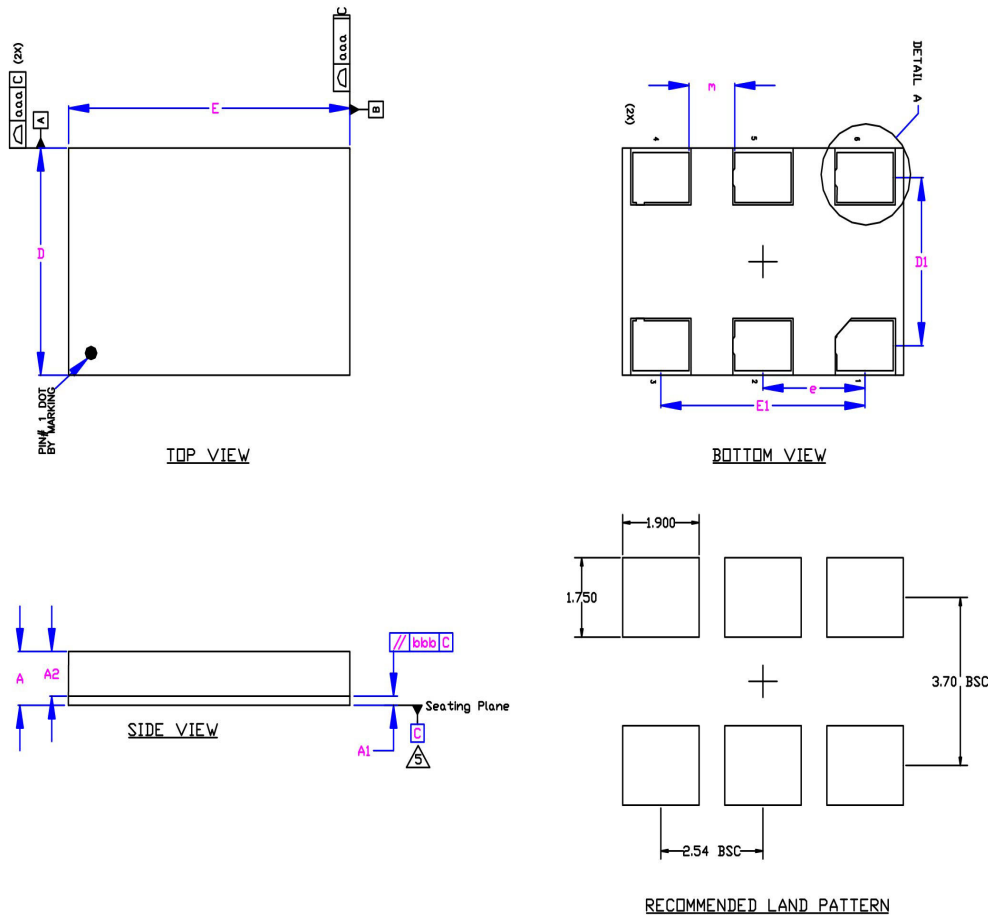
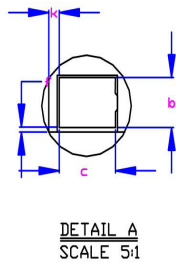


Figure 3. E5001A Period Jitter @ 805.664062MHz LVPECL, RMS TJ: 164fs, Pk-Pk TJ: 1.54ps

### Package Information and Recommended Land Pattern for 6-Pin LGA<sup>3</sup>



Dimensional Tol.			
aaa	0.100		
bbb	0.170		
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	1.260	1.330	1.400
A1	0.190	0.230	0.270
A2	1.070	1.100	1.130
D	4.900	5.000	5.100
D1	3.700 BSC		
E	6.900	7.000	7.100
E1	5.000 BSC		
b	1.050	1.100	1.150
c	1.350	1.400	1.450
e	2.540 BSC		
f	0.150	0.180	0.150
k	0.210	0.260	0.310
m	1.190	1.140	1.190
n	36		



- Notes
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
  2. Dimensions are in millimeters.
  3. 'e' represents the basic LGA pitch
  4. 'n' is the maximum no. of Land for a specified Package.
  5. Package warp shall be 0.150 max.
  6. Substrate base is BT Resin
  7. The Pin#1 corner must be identified on top side only.
  8. Reference Jeduc Spec M1-221
  9. Land pattern tolerance is 0.15mm unless otherwise specified

#### 6-Pin LGA (7x5mm)

**Note:**

3. Package information is correct as of the publication date. For updates and most current information, go to [www.microchip.com](http://www.microchip.com).

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