NB3N511

3.3V / 5.0V 14 MHz to 200 MHz PLL Clock Multiplier

ON Semiconductor®

http://onsemi.com

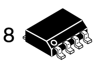
Description

The NB3N511 is a clock multiplier that will generate one of nine selectable output multiples of an input frequency via two 3−level select inputs (S0, S1). It accepts a standard fundamental mode crystal or an external reference clock signal. Phase−Locked−Loop (PLL) design techniques are used to produce a low jitter, TTL level clock output up to 200 MHz with a 50% duty cycle. An Output Enable (OE) pin is provided, and when asserted low, the clock output goes into tri−state (high impedance). The NB3N511 is commonly used in electronic systems as a cost efficient replacement for crystal oscillators

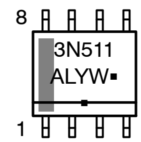
Features

- Clock Output Frequencies up to 200 MHz
- Nine Selectable Multipliers of the Input Frequency
- Operating Range: V_{DD} = 3.3 V ±10% or 5.0 V ±5%
- Low Jitter Output of 25 ps One Sigma (rms)
- Zero ppm Clock Multiplication Error
- 45% − 55% Output Duty Cycle
- TTL/CMOS Output with 25 mA TTL Level Drive
- Crystal Reference Input Range of 5 − 32 MHz
- Input Clock Frequency Range of 1 − 50 MHz
- OE, Output Enable with Tri−State Output
- 8−Pin SOIC
- Industrial Temperature Range −40°C to +85°C
- These are Pb−Free Devices

MARKING DIAGRAM



SOIC−8
D SUFFIX
CASE 751



3N511	=	Specific Device Code
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

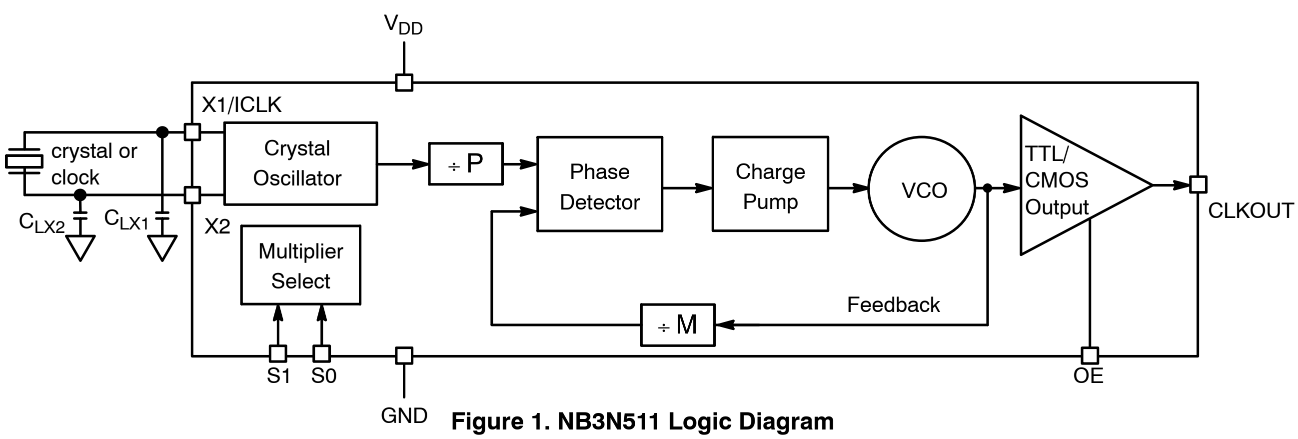


Figure 1. NB3N511 Logic Diagram

Table 1. CLOCK MULTIPLIER SELECT TABLE

S1*	S0*	CLKOUT Multiplier
L	L	4X Input
L	M	5.333X Input
L	H	5X Input
M	L	2.5X Input
M	M	2X Input
M	H	3.333X Input
H	L	6X Input
H	M	3X Input
H	H	8X Input

*Pins S1 and S0 default to M when open
L = GND
H = VDD
M = OPEN (unconnected; will default to VDD/2)

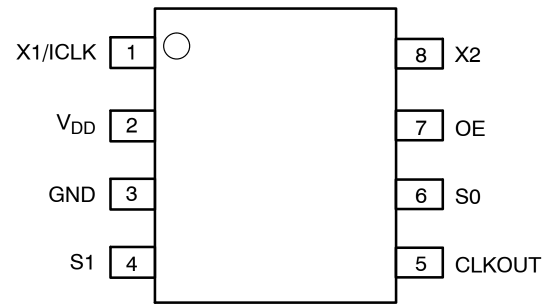


Figure 2. NB3N511 Package Pinout, 8−Pin (150 mil) SOIC (Top View)

Table 2. PIN DESCRIPTION

Pin #	Name	I/O	Description
1	X1/ICLK	Crystal or LVCMOS/LVTTL Input	Crystal or external reference clock input
2	VDD	Power supply	Positive supply voltage
3	GND	Power supply	0 V. Ground.
4	S1	Three level Input	Multiplier select pin − connect to V_{DD}, GND or float
5	CLKOUT	LVCMOS/LVTTL Output	Clock output
6	S0	Three level Input	Multiplier select pin − connect to V_{DD}, GND or float
7	OE	LVCMOS/LVTTL Input	Output Enable. CLKOUT is high impedance when OE is low. Internal pullup
8	X2	Crystal	Crystal input – Leave open when providing an external clock reference

Table 3. COMMON OUTPUT FREQUENCY EXAMPLES

Output Frequency (MHz)	Input Frequency (MHz)	S1, S0
20	10	M, M
24	12	M, M
30	10	H, M
32	16	M, M
33.33	16.66	M, M
37.5	15	M, L
40	10	L, L
48	12	L, L
50	20	M, L
60	10	H, L
64	16	L, L

Table 4. COMMON OUTPUT FREQUENCY EXAMPLES

Output Frequency (MHz)	Input Frequency (MHz)	S1, S0
66.66	20	M, H
72	12	H, L
75	25	H, M
80	10	H, H
83.33	25	M, H
90	15	H, L
100	20	L, H
120	15	H, H
125	25	L, H
133.3	25	L, M
150	25	H, L

Table 4. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1 kV > 150 V > 1 kV
RPU − OE Input Pull−up Resistor		270 kΩ
Moisture Sensitivity (Note 1)	SOIC−8	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V 0 @ 0.125 in
Transistor Count		9555
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{DD}	Positive Power Supply	GND = 0 V		7	V
V_{IO}	Input and Output Voltages			$-0.5\ V \le V_{IO} \le V_{DD} + 0.5$	V
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−8 SOIC−8	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 2)	SOIC−8	41 to 44	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 6. DC CHARACTERISTICS V_{DD} = 3.3 V ±10% or 5.0 V ± 5% unless otherwise noted, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Operating Voltage V_{DD} = 5 V V_{DD} = 3.3 V	4.75 3.0		5.25 3.6	V
I_{DD}	Power Supply Current – Inputs and outputs open, CLKOUT operating at 100 MHz (with 20 MHz crystal) V_{DD} = 5 V V_{DD} = 3.3 V		9 8		mA
V_{OH}	Output HIGH Voltage I_{OH} = −4 mA CMOS High	V_{DD} − 0.4			V
V_{OH}	Output HIGH Voltage I_{OH} = −25 mA TTL High	2.4			V
V_{OL}	Output LOW Voltage I_{OL} = 25 mA			0.4	V
V_{IH}	Input HIGH Voltage, ICLK only (pin 1) V_{DD} = 5 V V_{DD} = 3.3 V	(V_{DD} / 2) + 1 (V_{DD} / 2) + 0.7			V
V_{IL}	Input LOW Voltage, ICLK only (pin 1) V_{DD} = 5 V V_{DD} = 3.3 V			(V_{DD} / 2) − 1 (V_{DD} / 2) − 0.7	V
V_{IH}	Input HIGH Voltage, S0, S1	V_{DD} − 0.5			V
V_{IL}	Input LOW Voltage, S0, S1			0.5	V
V_{IH}	Input HIGH Voltage, OE (pin 7)	2.0			V
V_{IL}	Input LOW Voltage, OE (pin 7)			0.8	V
C_{in}	Input Capacitance, S0, S1 and OE		4		pF
I_{SC}	Output Short Circuit Current, CLKOUT		±70		mA
	Nominal Output Impedance		20		Ω

Table 7. AC CHARACTERISTICS V_{DD} = 3.3 V ±10% or 5.0 V ± 5% unless otherwise noted, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
f_{Xtal}	Crystal Input Frequency (Note 3)	5		32	MHz
f_{CLKIN}	Clock Input Frequency	1		50	MHz
f_{OUT}	Output Frequency Range $f_{OUTMIN} \le f_{IN}$ x Multiplier $\le f_{OUTMAX}$ V_{DD} = 4.25 to 5.25 V (5.0 V ± 5%) V_{DD} = 3.0 to 3.6 V (3.3 V ± 10%)	 14 14		 200 200	MHz
DC	Output Clock Duty Cycle at 1.5 V	45	50	55	%
OE_H	Output enable time, OE high to output on		50		ns
OE_L	Output disable time, OE low to tri−state		50		ns
$t_{jitter\ (rms)}$	Period Jitter (rms, 1 σ)		25		ps
$t_{jitter\ (pk-to-pk)}$	Total Period Jitter, (peak−to−peak)		±70		ps
t_r/t_f	Output rise/fall time (0.8 V to 2.0 V) (measured with 15 pF load)		1	1.5	ns

3. The crystal should be fundamental mode, parallel resonant. Do not use third overtone. For exact tuning when using a crystal, capacitors should be connected from pins X1/CLK to GND and X2 to GND. The value of these capacitors is given by the following equation, where C_L is the specified crystal load capacitance: Crystal capacitance (pF) = (C_L − 12) X 2. So, for a crystal with 16 pF load capacitance, use two 8 pF capacitors.

APPLICATIONS INFORMATION

High Frequency CMOS/TTL Oscillators

The NB3N511, along with a low frequency fundamental mode crystal, can build a high frequency TTL output oscillator. For example, a 20 MHz crystal connected to the NB3N511 with the 5X output selected (S1 = L, S0 = H) produces an 100 MHz CMOS/TTL output clock.

Decoupling and External Components

The NB3N511 requires a 0.01 μF decoupling capacitor to be connected between V_{DD} and GND on pins 2 and 3. It must be connected close to the NB3N511 to minimize lead inductance. Control input pins can be connected to device pins V_{DD} or GND, or to the V_{DD} and GND planes on the board.

Series Termination Resistor

A 33 Ω terminating resistor can be used next to the CLK pin for trace lengths over one inch.

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal load capacitors should be connected from pins X1 to ground and X2 to ground to optimize the frequency accuracy, See Figure 1.

The total on chip capacitance is approximately 12 pF. A parallel resonant, fundamental mode crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should equal (C_L − 12 pF) * 2. In this equation, C_L = crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 8 pF [(16 − 12) x 2 = 8].

Table 8. RECOMMENDED CRYSTAL PARAMETERS

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance
Load Capacitance	18 pF
Operating Range	−40 to +85°C
Shunt Capacitance	5 pF Max
Equivalent Series Resistance (ESR)	50 Ω Max
Correlation Drive Level	1.0 mW Max

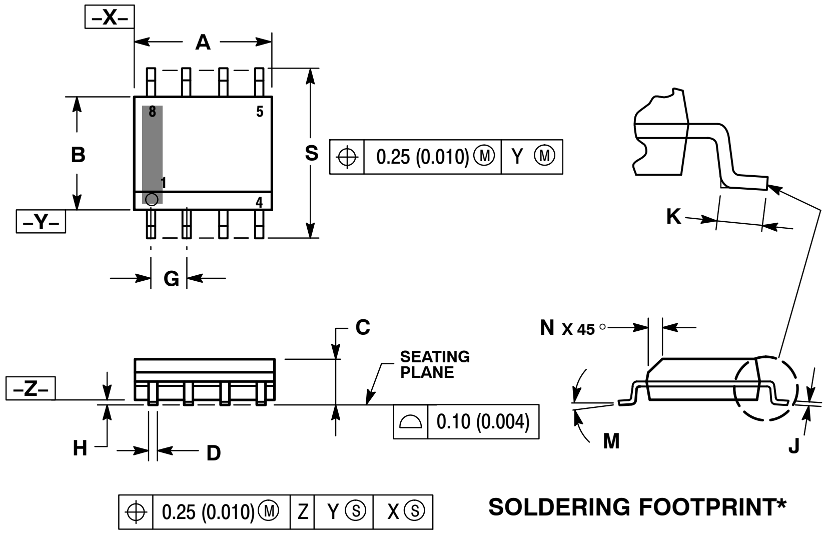
ORDERING INFORMATION

Device	Package	Shipping†
NB3N511DG	SOIC−8 (Pb−Free)	98 Units / Rail
NB3N511DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

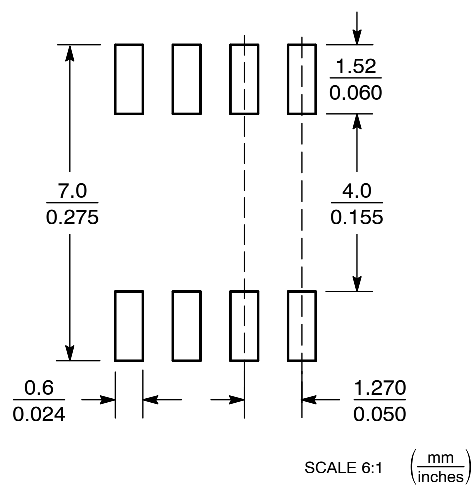
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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