

LTM2882: Dual Isolated RS232 µModule Transceiver + Power

DESCRIPTION

Demonstration circuit 1747A is a dual isolated RS232 µModule® transceiver with integrated power featuring the LTM®2882. The demo circuit provides a 2-channel, 2500V_{RMS}, galvanically isolated RS232 transceiver interface. The demo circuit features an EMI optimized circuit configuration and printed circuit board layout. All components are integrated into the µModule transceiver. The demo circuit operates from a single external supply

on V_{CC}. The part generates the output voltage V_{CC2} and communicates all necessary signaling across the isolation barrier using Linear Technology's isolator µModule technology.

Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V _{CC}	Input Supply Range	LTM2882-5	4.5	5	5.5	V
		LTM2882-3	3.0	3	3.6	V
V _{CC2}	Output Voltage	LTM2882-5 I _{LOAD} = 150mA	4.7	5		V
		LTM2882-3 I _{LOAD} = 100mA	4.7	5		V
f _{MAX}	Maximum Data Rate	R _L = 3k, C _L = 2.5nF	100			kbps
		R _L = 3k, C _L = 1nF	250			kbps
		R _L = 3k, C _L = 250pF	1000			kbps
V _{IO RM}	Maximum Working Insulation Voltage	GND to GND2	560			V _{DC}
			400			V _{RMS}
	Common Mode Transient Immunity		30			kV/µs

OPERATING PRINCIPLES

The LTM2882 contains an isolated DC/DC converter delivering power to V_{CC2} at 5V from the input supply V_{CC}. Isolation is maintained by the separation of GND and GND2 where significant operating voltages and transients can exist without affecting the operation of the LTM2882. The logic side ON pin enables or shuts down the LTM2882. RS232 signaling is controlled by the logic inputs T1IN, T2IN and DE. Connection to the transceiver pins, R1IN-T1OUT or R2IN-T2OUT, permits RS232 communication on the isolated side of the demo circuit. The circuit features two channels, supporting multiple RS232 channels or the addition of flow control on a single RS232 interface.

The spare logic channel, DIN to DOUT, is configured to control the state of the driver outputs, T1OUT and T2OUT, by connecting DOUT to DE.

Data is transmitted out the driver pins T1OUT and T2OUT from the inputs T1IN and T2IN with the input DE set to ON. Data is received through the receiver pins R1IN and R2IN to the outputs R1OUT and R2OUT; receivers are always active.

The demo circuit has been designed and optimized for low RF emissions. To this end, some features of the LTM2882 are not available for evaluation on the demo circuit.

OPERATING PRINCIPLES

The logic supply voltage V_L is tied to V_{CC} on the demo circuit. The ON pin and the spare logic channel DIN to DOUT, connected to DE, are selectable by jumper programming only.

EMI mitigation techniques used include the following:

1. Four layer PCB, allowing for isolated side to logic side “bridge” capacitor. The bridge capacitor is formed between an inner layer of floating copper which overlaps the logic side and isolated side ground planes. This structure creates two series capacitors, each with approximately 0.008" of insulation, supporting the full dielectric withstand rating of $2500V_{RMS}$. The bridge capacitor provides a low impedance return path for injected currents due to parasitic capacitances of the LTM2882's signal and power isolating elements.
2. Discrete bridge capacitors (C3, C4) mounted between GND2 and GND. The discrete capacitors provide additional attenuation at frequencies below 400MHz. Capacitors are safety rated type Y2, manufactured by Murata, part #GA342QR7GF471KW01L.

3. Minimized board/ground plane size. This reduces the dipole antenna formed between the logic side and isolated side ground planes.
4. Optimized top signal routing and ground floods to reduce signal loops, minimizing differential mode radiation.
5. Common mode filtering integrated into the input pin header and output DB9 connector. Filtering helps to reduce emissions caused by conducted noise and minimizes the effects of cabling to common mode emissions.
6. A combination of low ESL and high ESR decoupling. A low ESL ceramic capacitor is located close to the module minimizing high frequency noise conduction. High ESR tantalum capacitors are included to minimize board resonances and prevent voltage spikes due to hot plugging of the input supply voltage.

EMI performance is shown in Figure 1, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, “Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides.”

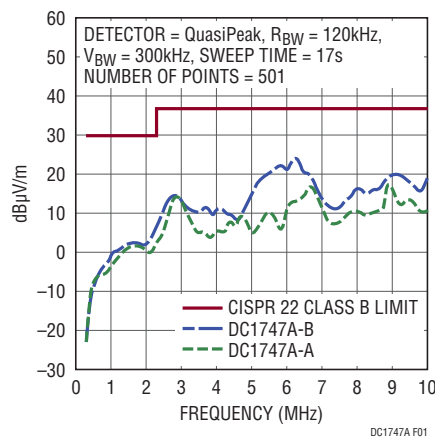


Figure 1. DC1747A Radiated Emissions

QUICK START PROCEDURE

Demonstration Circuit 1747A is easy to set up and evaluate the performance of the LTM2882. Refer to Figure 2 for proper measurement equipment setup and follow the procedure below.

NOTE: Use a short ground lead on the oscilloscope probe when measuring input or output voltage ripple and high speed signals.

1. Install JP1 and JP2 in the ON position.
2. Connect jumper T1I to R1O and T2I to R2O on pin header J1.
3. With power off, connect the input power supply to V_{CC} and GND on pin header J1.
4. Turn on the power at the input.

NOTE: Make sure that the input voltage does not exceed 6V.

5. Check for the proper output voltage. V_{CC2} = 5V. This can be measured between probe point V2 to G2.
6. Once the proper output voltages are established, connect a standard 9-Pin RS232 cable between J2 on the demo board and a computer.
7. Launch any program with the ability to send, receive, and monitor RS232 characters or data, including the ability to control the communication handshaking. Realterm is a free, powerful, terminal program which can easily be used for the above purposes. Signals may be verified with the use of an oscilloscope connected to any of the appropriate signals on pin header J1 or isolated side probe points located next to the DB9 connector.

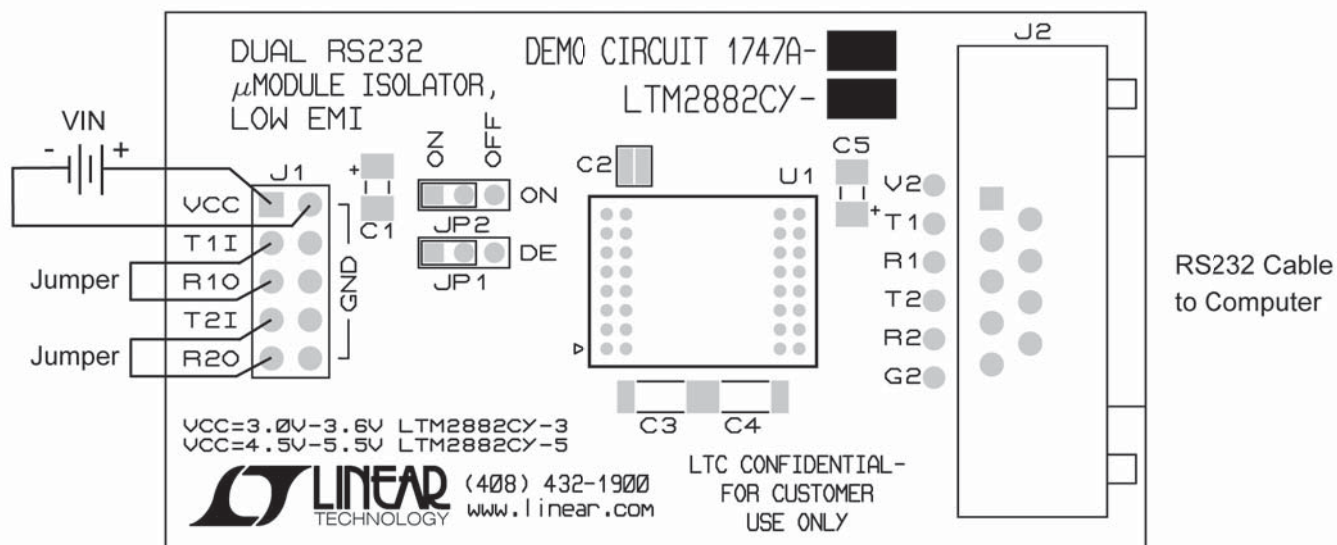
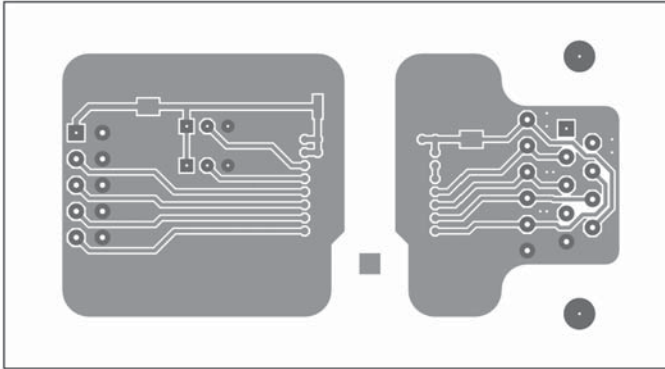


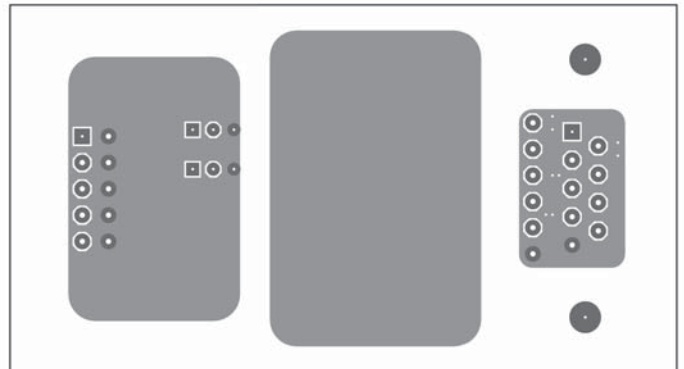
Figure 2. Demo Board Setup

DEMO MANUAL DC1747A

PCB LAYOUT



Layer 1. Top Layer



Layer 2. Ground Plane



Layer 3. Signal Layer



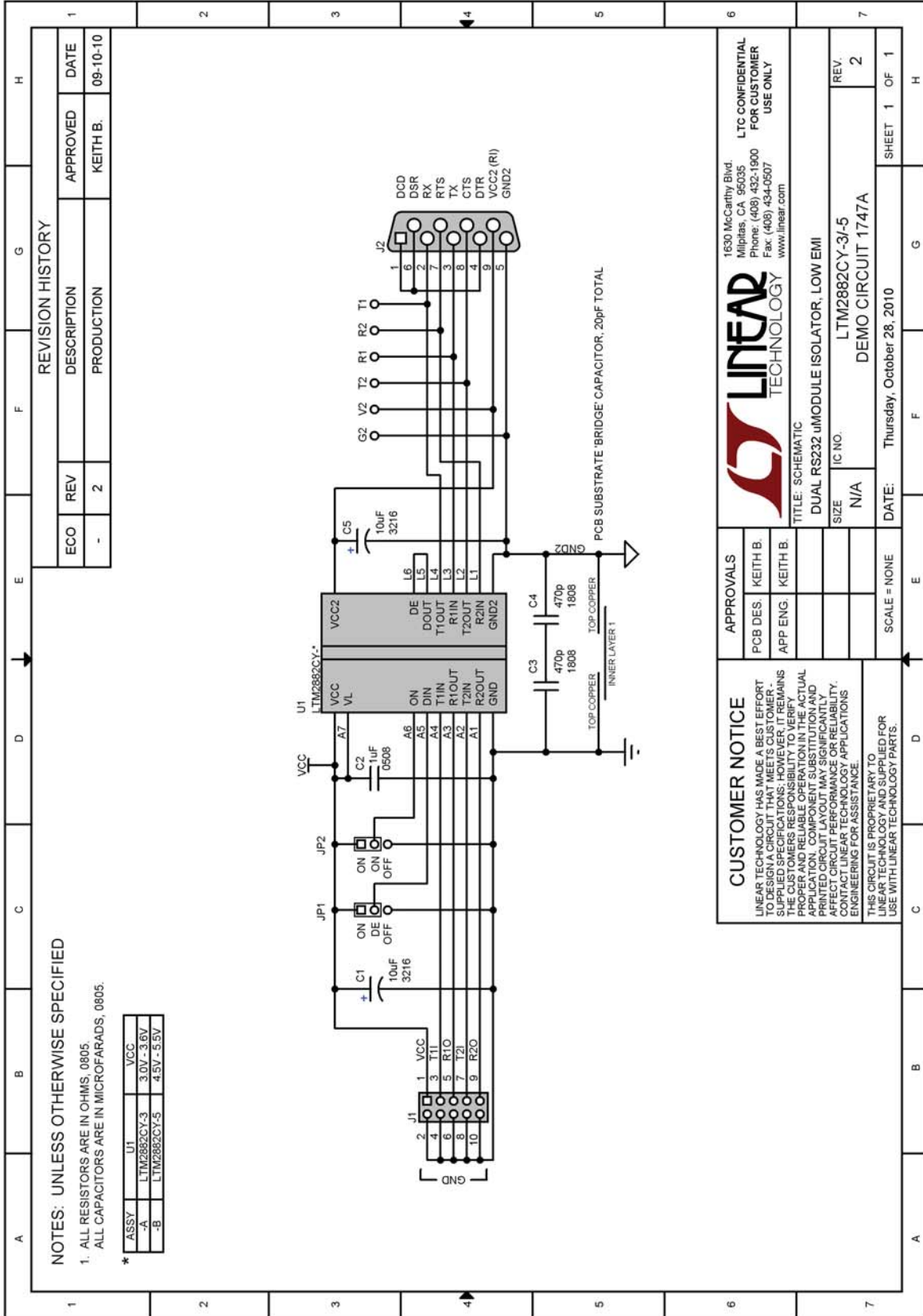
Layer 4. Bottom Layer

PARTS LIST

ITEM	QTY	REFERENCE	DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	1	U1	I.C., LTM2882CY-3	LINEAR TECHNOLOGY LTM2882CY-3#PBF
			I.C., LTM2882CY-5	LINEAR TECHNOLOGY LTM2882CY-5#PBF
Hardware/Components (For Demo Board Only)				
2	2	C1, C5	CAP, TANT 10F 10V 20% TAJA	AVX TAJA106M010RNJ
3	1	C2	CAP, CER 1F 10V 20% 0508	MURATA LLL219R71A105MA01L
4	2	C3, C4	CAP, CER 470pF 250V _{AC} 10% 1808	MURATA GA342QR7GF471KW01L
5	1	J1	0.1" DOUBLE ROW HEADER, 5 × 2 PIN	SAMTEC TSW-105-22-G-D
6	1	J1	0.1" FERRITE PLATE, 5 × 2 HOLE	FAIR RITE 2644247101
7	1	J2	CON, FILTERED, DSUB 9-PIN	KOBICONN 152-3609
8	2	JP1, JP2	2mm SINGLE ROW HEADER, 3-PIN	SAMTEC TMM-103-02-L-S
9	2	JP1, JP2	SHUNT	SAMTEC 2SN-BK-G

dc1747af

SCHEMATIC DIAGRAM



DEMO MANUAL DC1747A

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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