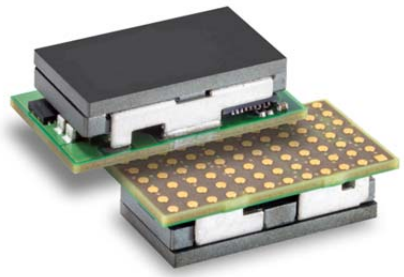
Murata Power Solutions

Okami OKDL-T/60-W12-xxx-C

60A Digital PoL DC-DC Converter Series



Typical units

FEATURES

- Input voltage range of 4.5 to 14Vdc
- 0.6 V - 1.8 V output voltage range
- High efficiency, typ. 94.9% at 5Vin, 1.8Vout half-load
- LGA Package: 25.1 x 14.1 x 7.0 mm (0.99 x 0.556 x 0.276 in)
- Configuration & Monitoring via PMBus™
- Synchronization & phase spreading
- Current sharing, Voltage Tracking & Voltage margining
- MTBF 50 Mhrs
- Non-Linear Response for reduction of decoupling capacitor
- Remote On/Off control & Power Good
- Output short-circuit, output over voltage, & over temperature protection
- Certified to UL/IEC 60950-1

PRODUCT OVERVIEW

The OKDL-T/60-W12 series are high efficiency, digital Point-of-Load (PoL) DC-DC power converters capable of delivering 60A/108W. Available in a Land Grid Array Package, these converters have a typical efficiency of 94.9%. PMBus™ compatibility allows monitoring and configuration of critical system-level performance requirements.

Apart from standard PoL performance and safety features like OVP, OCP, OTP, and UVLO, these digital converters have advanced features: digital current sharing (full power, no derating), non-linear transient response, optimized dead time control, synchronization, and phase spreading. These converters are ideal for use in telecommunications, networking, and distributed power applications.

Power Management via PMBus™

- Configurable soft-start/stop
- Configurable output voltage (Vout) and voltage margins (Margin low and Margin high)
- Configurable protection limits for OVP, input over voltage, input under voltage, over current, on/off, and temperature
- Status monitor Vout, Iout, Vin, Temp, Power Good, and On/Off

Applications

- Distributed power architectures
- Intermediate bus voltage applications
- Servers and storage applications
- Network equipment

PART NUMBER STRUCTURE

OKD L - T / 60 – W12 - xxx - C

Digital Non-isolated PoL

L = Land Grid Array (LGA)

Trimmable Output
Voltage Range
0.6 - 1.8Vdc

Maximum Rated Output
Current in Amps

Input Voltage Range
4.5-14Vdc

Software Configuration Digits
(001 is positive turn-on logic)
(002 is negative turn-on logic)*

RoHS Hazardous Substance Compliance
C = RoHS-6 (does not claim EU RoHS exemption 7b – lead in solder)

***Special quantity order is required; contact Murata Power Solutions for MOQ and lead times.**

RoHS COMPLIANT · cULus · PMBus · AMP Architects of Modern Power

Ordering Guide				
Model Number	Package Type	Output	Input Range	On/Off Logic
OKDL-T/60-W12-001-C	Land Grid Array	0.6-1.8V, 60A/108W	4.5V to 14V	Positive

Absolute Maximum Ratings

Characteristics			Min	Typ	Max	Unit
T_{P1}		Operating temperature (see Thermal Consideration section)	-40		150	°C
T_S		Storage temperature (Ambient)	-40		125	°C
V_I		Input voltage (See Operating Information Section for input	-0.3		16	V
Signal I/O voltage	CTRL, SA0, SA1, SALERT, SCL, SDA, VSET, SYNC, PG, VTRK		-0.3		6.5	V
Ground voltage differential	-S, PREF, GND		-0.3		0.3	V
Analog pin voltage	V_O, +S		-0.3		6.5	V

General and Safety	Conditions	Min	Typ	Max	Unit
Safety	Designed for UL/IEC/EN 60950 1				
Calculated MTBF	Telcordia SR-332, Issue 2 Method 1		50.15		Mhrs

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the Electrical Specification section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Configuration File

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the Standard configuration, unless otherwise specified. The Standard configuration is designed to fit most application needs. Changes in Standard configuration might be required to optimize performance in specific application. Note that current sharing operation requires changed configuration.

Product Electrical Specifications
OKDL-T/60-W12-xxx-C

T_{P1} = -30 to +95 °C, V_I = 4.5 to 14 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
V_O defined by pin strap. Standard configuration.
Tested with external C_{IN} = 470 µF/10 mΩ + 8 x 47 µF, C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF. See Operating Information section for design of input and output filters for a specific application.
In the test set-up sense lines are connected directly to output pins on a converter and all the output voltage measurements are made on output pins.

Characteristics			Conditions	Min	Typ	Max	Unit
V_I	Input voltage			4.5		14	V
	Input voltage slew rate		Monotonic			2.4	V/ms
V_O	Output voltage without pin-strap				1.2		V
	Output voltage adjustment range			0.60		1.8	V
	Output voltage adjustment including PMBus margining			0.54		1.98	V
	Output voltage set-point resolution				±1.2		mV
	Output voltage accuracy		Including line, load, temp	-1		1	% V_O
			Current sharing. Note 2	-2		2	% V_O
	Internal resistance +S/-S to VOUT/GND				47		Ω
	+S bias current				110		µA
	-S bias current				-110		µA
	Line regulation	I_O = max I_O	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		1 1 1		mV
	Load regulation	I_O = 0 - 100%	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		1 1 1		mV
V_{Oac}	Output ripple & noise (up to 20 MHz)		V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		6 7 9		mVp-p
I_O	Output current			0		60	A
I_{lim}	Current limit threshold			62	72	80	A
I_{sc}	Short circuit current		RMS, hiccup mode, V_O = 1.0 V, 6 mΩ short		9		A
η	Efficiency	50% of max I_O	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		87.6 90.8 93.6		%
		I_O = max I_O	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		83.9 88.3 92.0		%
P_d	Power dissipation at max I_O		V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		6.9 7.9 9.4		W
P_{li}	Input idling power	I_O = 0	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V		0.86 1.0 1.6		W
P_{CTRL}	Input standby power		Turned off with CTRL-pin		180		mW
			Low power mode		90		mW
C_I	Internal input capacitance		V_I = 0 V		132		µF
C_O	Internal output capacitance		V_O = 0 V		500		µF
C_{OUT}	Total external output capacitance		Note 3	1000		35000	uF
	ESR range of external capacitors		Per single capacitor. Note 3	3		30	mΩ

Note 1. For Vout < 1.0V accuracy is ±10 mV. For further deviations see section Output Voltage Adjust using PMBus.
Note 2. Accuracy here means deviation from ideal output voltage level given by configured droop and actual load. Includes line, load and temp variations.
Note 3. This range applies to the "Universal PID" setting described in Operating Information.

Common Electrical Specifications

This section includes parameter specifications common to all product versions within the product series. Typically these are parameters defined by the digital controller of the products. In the table below PMBus commands for configurable parameters are written in capital letters.

T_{P1} = -30 to +95 °C, V_I = 4.5 to 14 V, VI > V_O + 1.0 V unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
V_O defined by pin-strap. Standard configuration.

Characteristics		Conditions	Min	Typ	Max	Unit
$f_{SW} = 1/T_{SW}$	Switching Frequency			320		kHz
	Switching Frequency Range, Note 1	PMBus configurable FREQUENCY_SWITCH	200		640	kHz
	Switching Frequency Set-point Accuracy		-5		5	%
	External Sync Duty Cycle		95		-	%
	External Sync Pulse Width		150			ns
	Input Clock Frequency Drift Tolerance	External sync	-13		13	%

T_{INIT}	Initialization Time	From V_I > ~3 V to ready to be enabled		50		ms
T_{ONdel_tot}	Output voltage Total On Delay Time	Enable by input voltage	T_{INIT} + T_{ONdel}			
		Enable by CTRL pin	T_{ONdel}			
T_{ONdel}	Output voltage On Delay Time	Turn on delay duration		5		ms
		Turn off delay duration		5		ms
		Accuracy (actual delay vs set value)		-0.25/+4		ms
		Range PMBus configurable TOFF_DELAY	0		200	ms
		Delay accuracy (actual delay vs set value)		-0/+2		ms
T_{ONrise} / $T_{OFFfall}$	Output voltage On/Off Ramp Time (0-100%-0 of V_O)	Turn on ramp duration		5		ms
		Turn off ramp duration	Disabled in standard configuration. Turn off immediately upon expiration of Turn off delay.			
		Ramp duration range PMBus configurable TON_RISE/TOFF_FALL	0		200	ms
		Ramp time accuracy for standalone operation (actual ramp time vs set value)	100			µs
			Current sharing 20% of set value			

Characteristics		Conditions	Min	Typ	Max	Unit
Power Good, PG	PG threshold	Rising		90		% V_O
		Falling		85		% V_O
	PG thresholds range	PMBus configurable POWER_GOOD_ON VOUT_UV_FAULT_LIMIT	0		100	% V_O
	PG delay	From V_O reaching target to PG assertion		50-200		ms
	PG delay range	PMBus configurable POWER_GOOD_DELAY	0		5000	ms

Input Under Voltage Protection, IUVP	IUVP threshold			3.85		V
	IUVP threshold range	PMBus configurable VIN_UV_FAULT_LIMIT	3.85		14	V
	IUVP hysteresis			0.35		V
	IUVP hysteresis range	PMBus configurable VIN_UV_WARN_LIMIT	0		10.15	V
	Set point accuracy		-150		+150	mV
	IUVP response delay			2.5		µs
	Fault response	VIN_UV_FAULT_RESPONSE	Automatic restart, 70 ms. Note 2			

Characteristics		Conditions	Min	Typ	Max	Unit
Input Over Voltage Protection, IOVP	IOVP threshold			16		V
	IOVP threshold range	PMBus configurable VIN_OV_FAULT_LIMIT	4.2		16	V
	IOVP hysteresis			1		V
	IOVP hysteresis range	PMBus configurable VIN_OV_WARN_LIMIT	0		11.8	V
	Set point accuracy		-150		+150	mV
	IOVP response delay			2.5		µs
	Fault response	VIN_OV_FAULT_RESPONSE	Automatic restart, 70 ms. Note 2			
Output Voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold			85		% V_O
	UVP threshold range	PMBus configurable VOUT_UV_FAULT_LIMIT	0		100	% V_O
	OVP threshold			115		% V_O
	OVP threshold range	PMBus configurable VOUT_OV_FAULT_LIMIT	100		115	% V_O
	UVP/OVP response time			25		µs
	Fault response	VOUT_UV_FAULT_RESPONSE VOUT_OV_FAULT_RESPONSE	Automatic restart, 70 ms. Note 2			
Over Current Protection, OCP	OCP threshold	Set value	76			A
	OCP threshold range	PMBus configurable IOUT_AVG_OC_FAULT_LIMIT	0-76			A
	Protection delay	PMBus configurable	1-32			T_{SW}
	Fault response	MFR_IOUT_OC_FAULT_RESPONSE	Automatic restart, 70 ms. Note 2			
Over Temperature Protection, OTP Position P4	OTP threshold			125		°C
	OTP threshold range	PMBus configurable OT_FAULT_LIMIT	-40		+125	°C
	OTP hysteresis	PMBus configurable		15		°C
	Fault response	OT_FAULT_RESPONSE	Automatic restart, 240 ms. Note 2			

Characteristics		Conditions	Min	Typ	Max	Unit
Monitoring Accuracy	Input voltage READ_VIN			±3		% V_I
	Output voltage READ_VOUT			±1		% V_O
	Output current READ_IOUT	T_{P1} = 25 °C, V_O = 1.0 V		±3		A
		T_{P1} = 0 - 95 °C, V_O = 1.0 V		±5		A
	Duty cycle READ_DUTY_CYCLE	Duty cycle < 10%	-3		3	%
		Duty cycle > 10%	-1	±0.5	1	%
	Temperature READ_TEMPERATURE_1	Position P4	-5		5	°C

Tracking Input Bias Current	VTRK pin		110	200	µA
Tracking Input Voltage Range	VTRK pin	0		5	V
Tracking Accuracy	Regulation 100% tracking	-1		1	%
	Ramp accuracy, V_O = 1.0 V, 10 ms ramp	-100		100	mV

Current difference between products in a current sharing group	Steady state operation	Max 2 x READ_IOUT monitoring accuracy			
Number of products in a current sharing group				8	

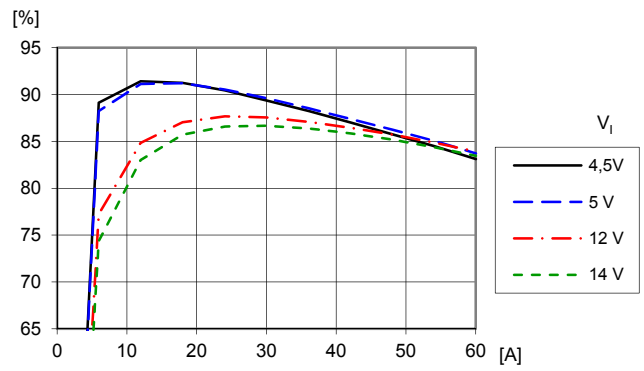
V_{OL}	Logic output low signal level	SCL, SDA, SYNC, GCB, SALERT, PG Sink/source current = 4 mA			0.8	V
V_{OH}	Logic output high signal level		2.25			V
I_{OL}	Logic output low sink current				4	mA
I_{OH}	Logic output high source current				2	mA
V_{IL}	Logic input low threshold	SCL, SDA, CTRL, SYNC, GCB			0.8	V
V_{IH}	Logic input high threshold		2			V
I_{I_LEAK}	Logic leakage current	SCL, SDA, SYNC, SALERT, PG			10	µA
C_{I_PIN}	Logic pin input capacitance	SCL, SDA, CTRL, SYNC, GCB		10		pF
R_{I_PU}	Logic pin internal pull-up resistance	SCL, SDA, SALERT		No internal pull-up		
		CTRL to +5V		1		kΩ
f_{SMB}	SMBus Operating frequency			100		kHz
T_{BUF}	SMBus Bus free time	STOP bit to START bit See section SMBus – Timing	2			ms
t_{set}	SMBus SDA setup time from SCL	See section SMBus – Timing	300			ns
t_{hold}	SMBus SDA hold time from SCL	See section SMBus – Timing	250			ns

Note 1.There are configuration changes to consider when changing the switching frequency, see section Switching Frequency. Changing switching frequency below 320 kHz is not recommended for Vout > 1.2V.
Note 2.Automatic restart ~70 ms or 240 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart. See Operating Information for other fault response options.
Note 3.The typical initialization time varies in the range ~40-50 ms, depending on the On Delay Time (TON_DELAY) and On Ramp Time (TON_RISE) settings.

Typical Output Characteristics, V_O = 0.6 V

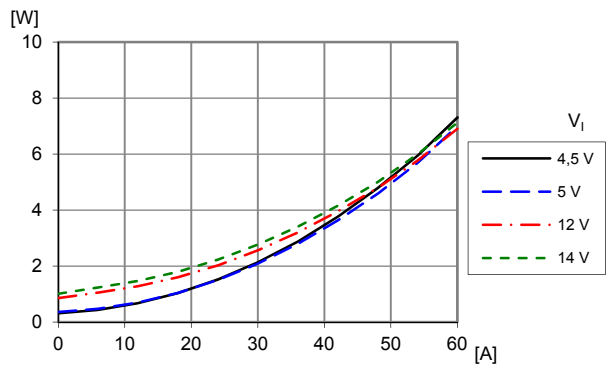
Standard configuration unless otherwise specified, T_{P1}=+25 °C

Efficiency



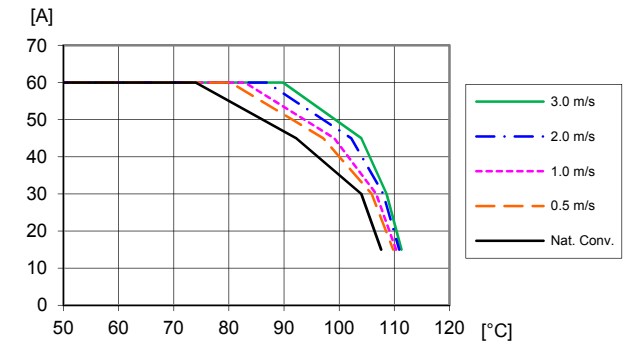
Efficiency vs. load current and input voltage.

Power Dissipation



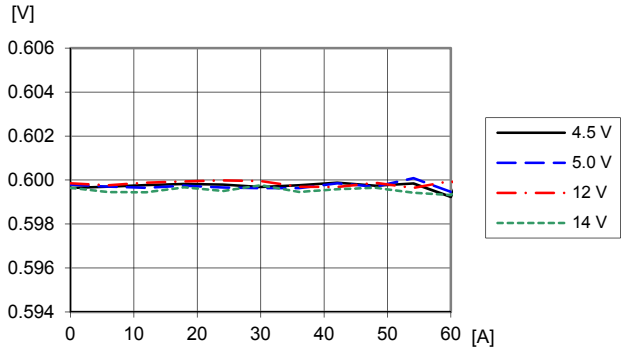
Dissipated power vs. load current and input voltage.

Output Current Derating



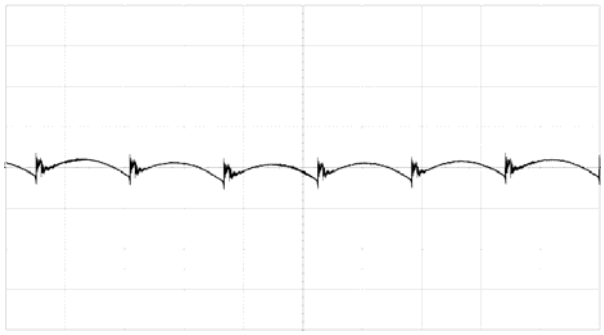
Available load current vs. ambient air temperature and airflow at V_I= 12 V. See section Thermal Consideration.

Load Regulation



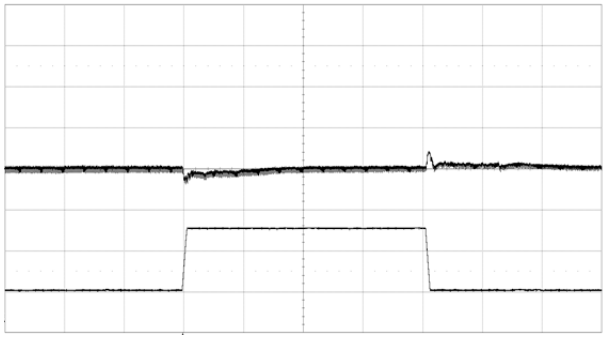
Output voltage vs load current.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = 60 A, C_{OUT} = 3 x 470 µF/4.5 mΩ + 10 x 100 µF
Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response

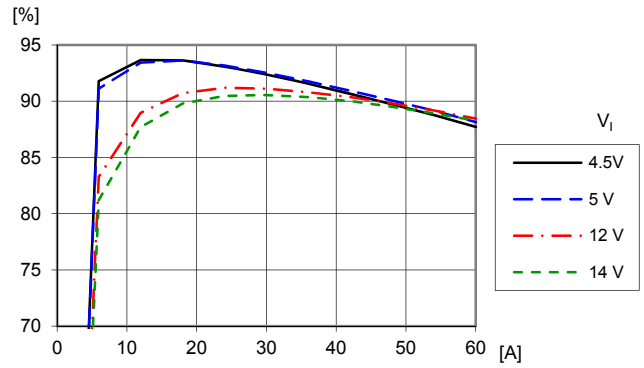


Output voltage response to load current step change (15–45–15 A), di/dt = 2 A/µs, at V_I = 12 V, C_{OUT} = 6 x 470 µF/4.5 mΩ + 10 x 100 µF.
Compensation settings by DLC and optimized NLR.
Scale: 50 mV/div, 20 A/div, 200 µs/div.

Typical Output Characteristics, V_O = 1.0 V

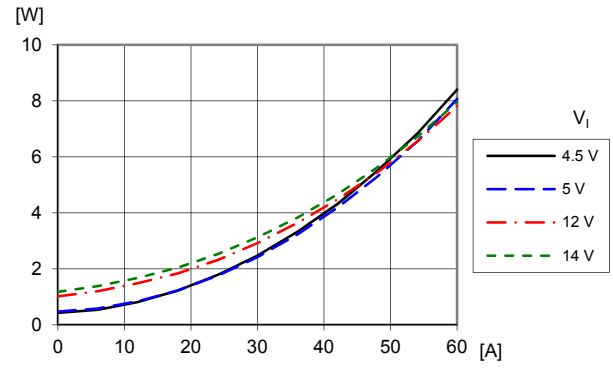
Standard configuration unless otherwise specified, T_{P1}=+25 °C

Efficiency



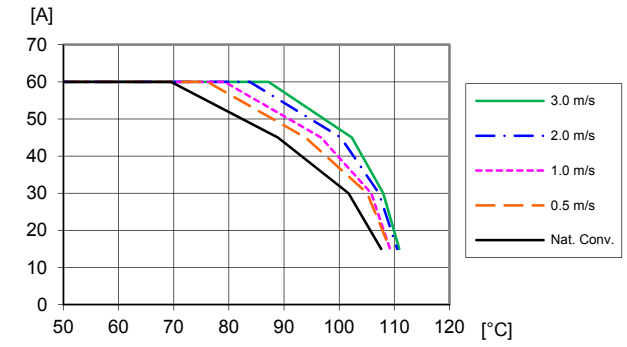
Efficiency vs. load current and input voltage.

Power Dissipation



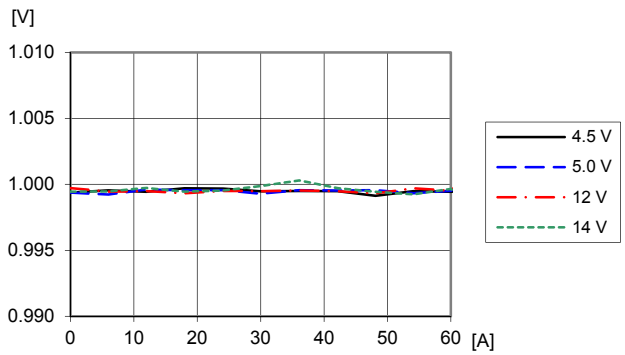
Dissipated power vs. load current and input voltage.

Output Current Derating



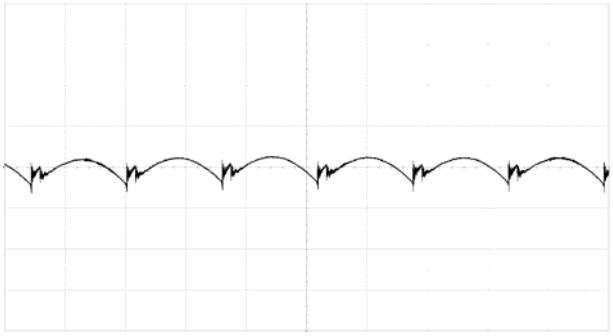
Available load current vs. ambient air temperature and airflow at V_I= 12 V. See section Thermal Consideration.

Load Regulation



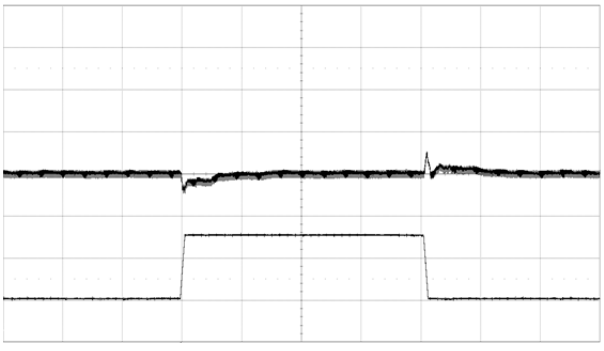
Output voltage vs load current.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = 60 A,
C_{OUT} = 3 x 470 µF/4.5 mΩ + 10 x 100 µF
Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response

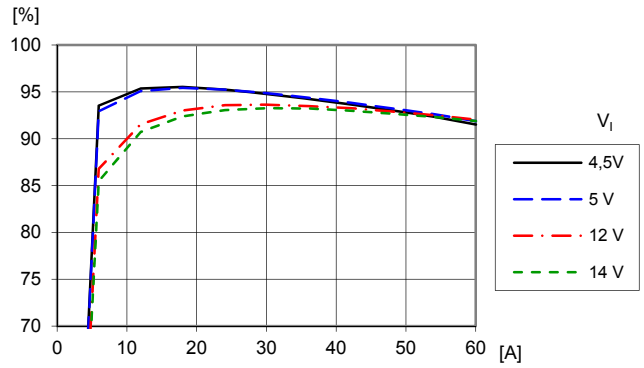


Output voltage response to load current step change (15–45–15 A),
di/dt = 2 A/µs, at V_I = 12 V, C_{OUT} = 6x470 µF/4.5 mΩ + 10x100 µF.
Compensation settings by DLC and optimized NLR.
Scale: 50 mV/div, 20 A/div, 200 µs/div.

Typical Output Characteristics, V_O = 1.8 V

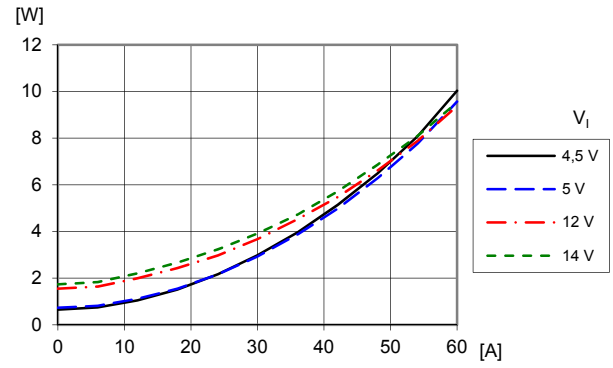
Standard configuration unless otherwise specified, T_{P1}=+25 °C

Efficiency



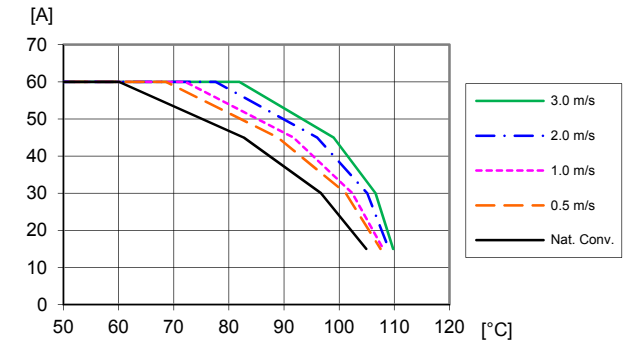
Efficiency vs. load current and input voltage.

Power Dissipation



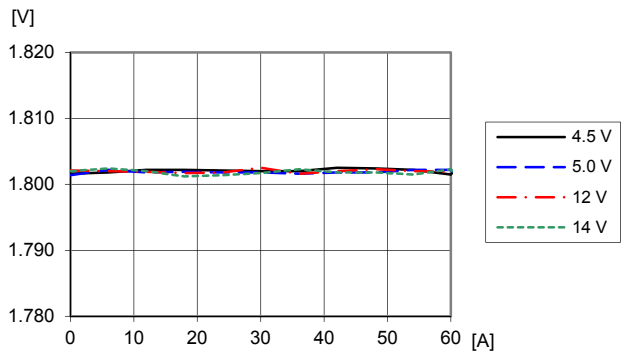
Dissipated power vs. load current and input voltage.

Output Current Derating



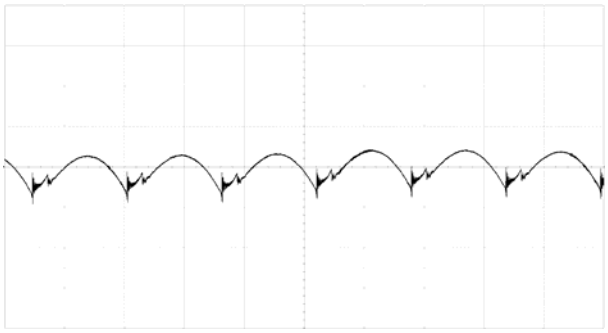
Available load current vs. ambient air temperature and airflow at V_I= 12 V. See section Thermal Consideration.

Load Regulation



Output voltage vs load current.

Output Ripple and Noise



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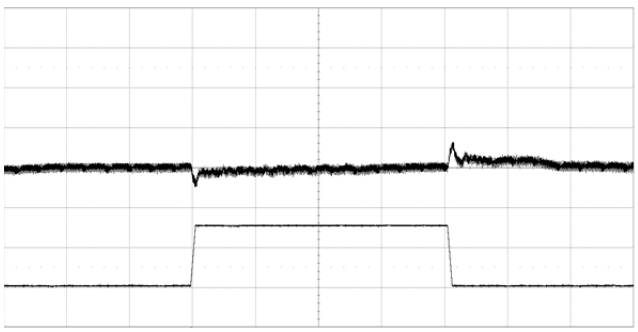
See section Output Ripple and Noise.

Transient Response

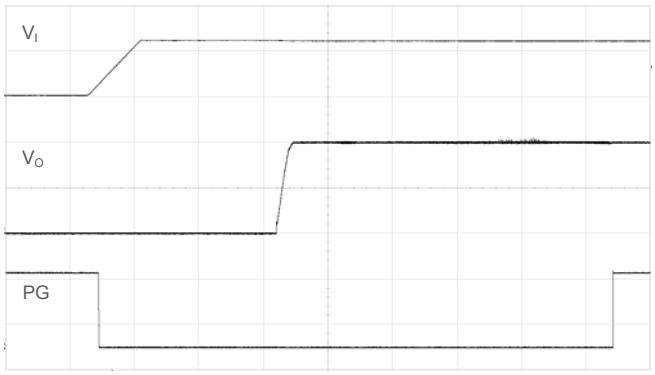


Output voltage response to load current step change (15–45–15 A),
di/dt = 2 A/µs, at V_I = 12 V, C_{OUT} = 6 x 470 µF/4.5 mΩ + 10 x 100 µF.
Compensation settings by DLC and optimized NLR.
Scale: 50 mV/div, 20 A/div, 200 µs/div.

Typical On/Off Characteristics

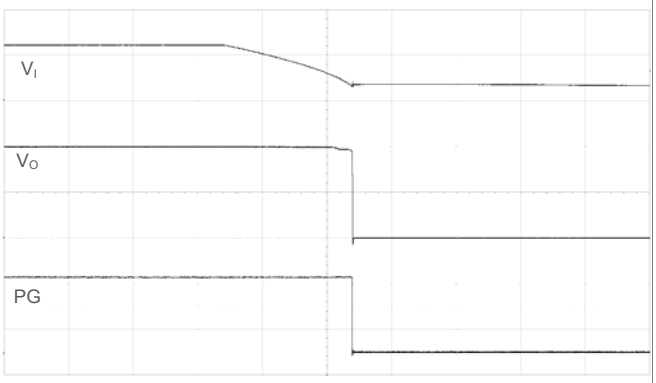
Standard configuration, T_{P1} = +25 °C, V_O = 1.0 V

Enable by input voltage – PG Open-Drain (default)



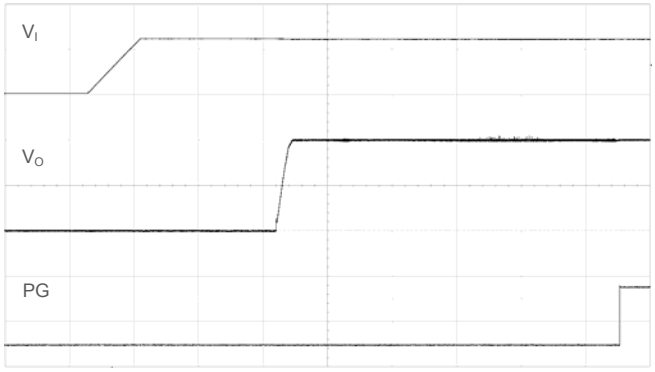
Output enabled by applying V_I. V_I = 12 V, I_O = max I_O.
TON_DELAY = TON_RISE = 5 ms, PG delay controlled by DLC.
MFR_CONFIG = 0x7F10 (default). PG pulled up to external voltage.
Note: PG being high before Vin applied can be avoided by pulling up PG to Vout.
Scale from top: 10, 0.5, 2 V/div, 20 ms/div.

Disable by input voltage – PG Open-Drain (default)



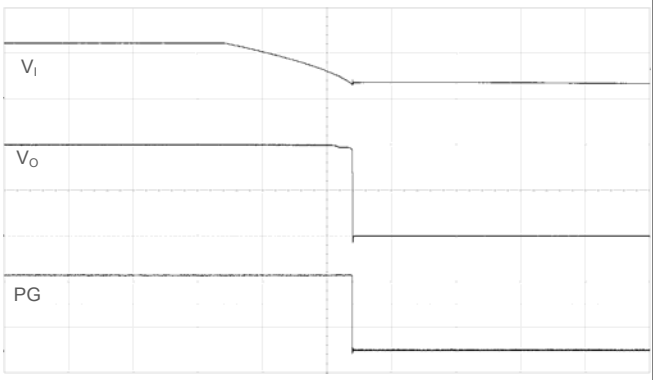
Output disabled by removing V_I. V_I = 12 V, I_O = max I_O.
Scale from top: 10, 0.5, 2 V/div, 20 ms/div.

Enable by input voltage – PG Push-Pull



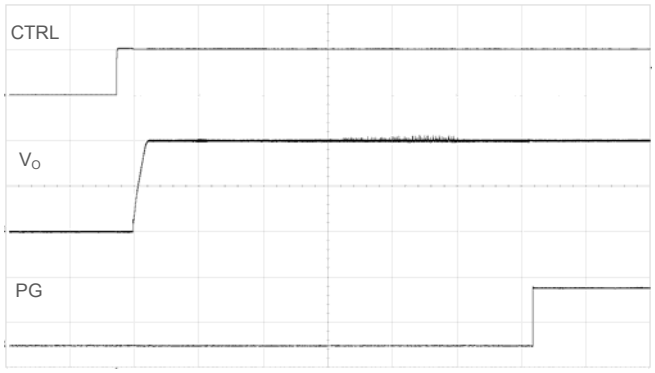
Output enabled by applying V_I. V_I = 12 V, I_O = max I_O.
TON_DELAY = TON_RISE = 5 ms, POWER_GOOD_DELAY = 2 ms.
MFR_CONFIG = 0x7F12 (PG push-pull).
Scale from top: 10, 0.5, 2 V/div, 20 ms/div.

Disable by input voltage – PG Push-Pull



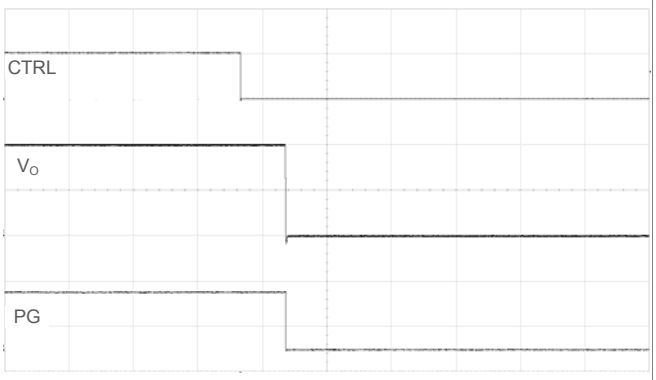
Output disabled by removing V_I. V_I = 12 V, I_O = max I_O.
Scale from top: 10, 0.5, 2 V/div, 20 ms/div.

Enable by CTRL pin



Output enabled by CTRL pin. V_I = 12 V, I_O = max I_O.
TON_DELAY = TON_RISE = 5 ms, PG delay controlled by DLC.
Scale from top: 5, 0.5, 2 V/div, 20 ms/div.

Disable by CTRL pin

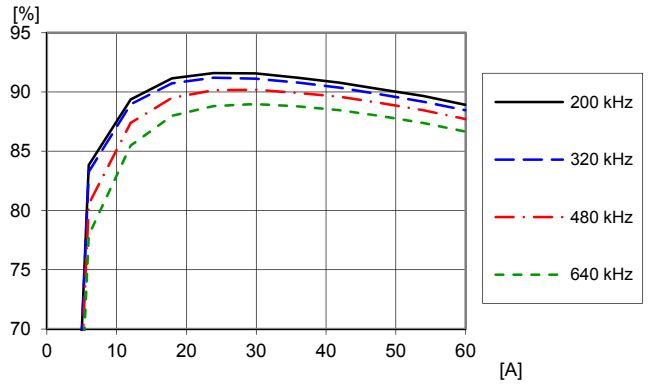


Output disabled by CTRL pin. V_I = 12 V, I_O = max I_O.
Scale from top: 5, 0.5, 2 V/div, 10 ms/div.

Typical Characteristics

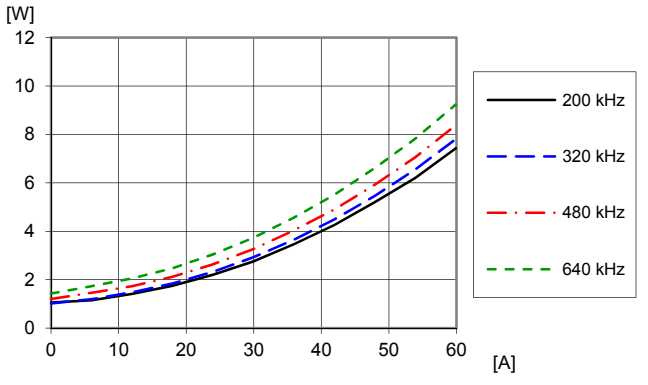
Standard configuration, T_{P1} = +25 °C

Efficiency vs. Output Current and Switching Frequency



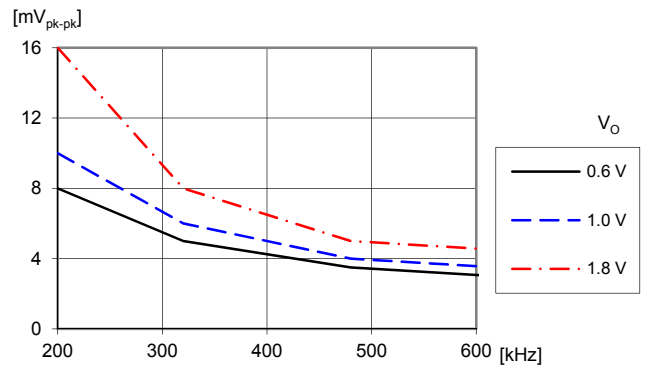
Efficiency vs. load current and switching frequency at V_I = 12 V, V_O = 1.0 V, C_{OUT} = 3 x 470 µF/4.5 mΩ + 10 x 100 µF. Frequency changed by PMBus command FREQUENCY_SWITCH.

Power Dissipation vs. Output Current and Switching Frequency



Dissipated power vs. load current and switching frequency at V_I = 12 V, V_O = 1.0 V, C_{OUT} = 3 x 470 µF/4.5 mΩ + 10 x 100 µF. Frequency changed by PMBus command FREQUENCY_SWITCH.

Output Ripple vs. Switching Frequency



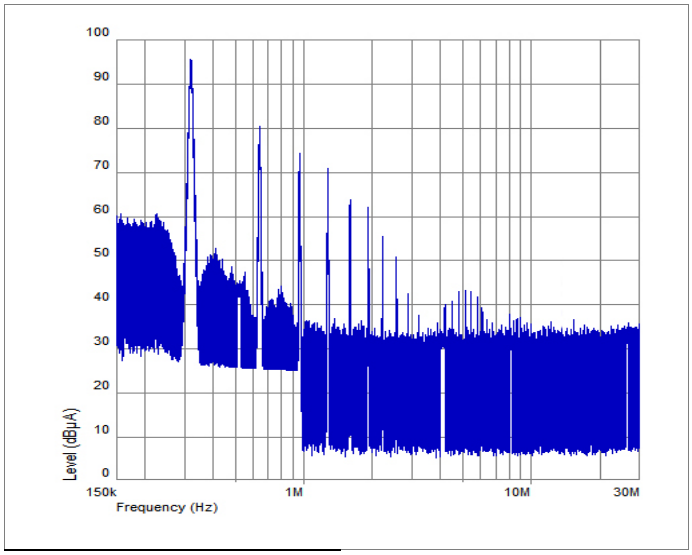
Output voltage ripple V_{pk-pk} vs. switching frequency at V_I = 12 V, I_O = max I_O, C_{OUT} = 3 x 470 µF/4.5 mΩ + 10 x 100 µF. Frequency changed by PMBus command FREQUENCY_SWITCH.

EMC Specification

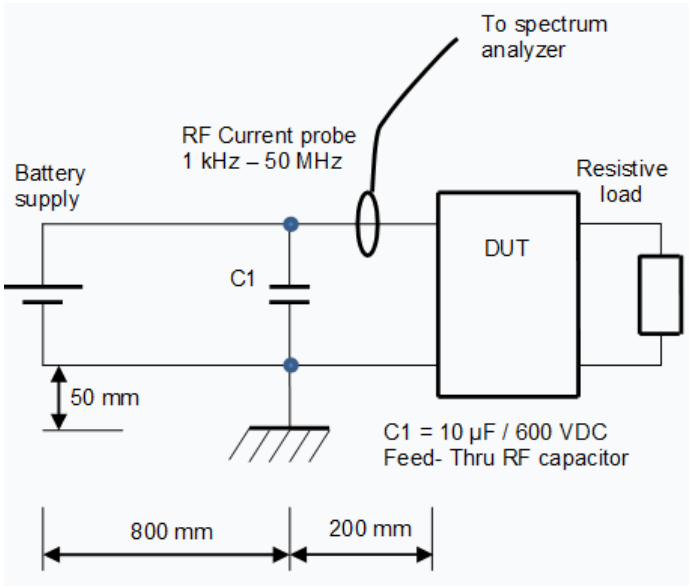
Conducted EMI is measured according to the test set-up below. The typical fundamental switching frequency is 320 kHz.

Conducted EMI

Input terminal value (typical for standard configuration). V_I = 12 V, V_O = 1.0 V, I_O = 60 A.



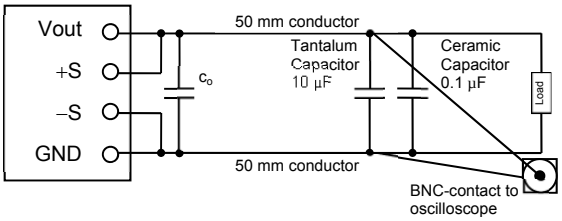
EMI without filter.



Test set-up conducted emission, power lead.
DUT = Product mounted on a 154 cm² test board with the external capacitances C_{IN} = 470 µF/10 mΩ + 8 x 47 µF and C_{OUT} = 3 x 470 µF/4.5 mΩ + 10 x 100 µF.

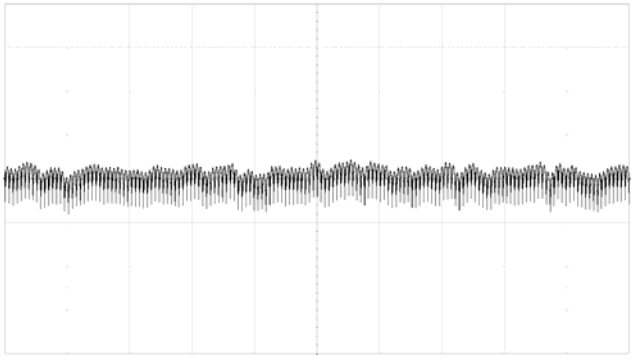
Output Ripple and Noise

Output ripple and noise are measured according to figure below. A 50 mm conductor works as a small inductor forming together with the two capacitances a damped filter.



Output ripple and noise test set-up.

The digital compensation of the product is designed to automatically provide stability, accurate line and load regulation and good transient performance for a wide range of operating conditions (switching frequency, input voltage, output voltage, output capacitance). Inherent from the implementation and normal to the product there will be some low frequency ripple at the output, in addition to the fundamental switching frequency output ripple. This low frequency ripple is not related to instability of control loop. The total output ripple and noise is maintained at a low level.



V_I=12 V, V_O=1.0 V, I_O=60 A, C_{OUT} = 10 x 100 µF + 3 x 470 µF/4.5 mΩ, 5 mV/div, 50 µs/div

Example of low frequency ripple at the output.

PMBus Interface

Power Management Overview

This product incorporates a wide range of configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults.

The product's standard configuration is suitable for a wide range of operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface.

Throughout this document, different PMBus commands are referenced. A detailed description of each command is provided in the appendix at the end of this specification.

SMBus Interface

The product can be used with any standard two-wire I²C or SMBus host device. See Electrical Specification for allowed clock frequency range. In addition, the product is compatible with PMBus version 1.1 and includes an SALERT line to help mitigate limitations related to continuous fault monitoring. The product supports 100 kHz bus clock frequency only. The PMBus signals SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\tau = R_P C_p \leq 1\mu s$$

where R_p is the pull-up resistor value and C_p is the bus loading. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.5 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

PMBus Addressing

The PMBus address should be configured with resistors connected between the SA0/SA1 pins and the PREF pin, as shown in the Typical Application Circuit. Recommended resistor values for hard-wiring PMBus addresses are shown in the table below. 1% tolerance resistors are required.

Index	R_{SA} [kΩ]	Index	R_{SA} [kΩ]
0	10	13	34.8
1	11	14	38.3
2	12.1	15	42.2
3	13.3	16	46.4
4	14.7	17	51.1
5	16.2	18	56.2
6	17.8	19	61.9
7	19.6	20	68.1
8	21.5	21	75
9	23.7	22	82.5
10	26.1	23	90.9
11	28.7	24	100
12	31.6		

The PMBus address follows the equation below:

PMBus Address (decimal) = 25 x (SA1 index) + (SA0 index)

The user can theoretically configure up to 625 unique PMBus addresses, however the PMBus address range is inherently limited to 128. Therefore, the user should use index values 0 - 4 on the SA1 pin and the full range of index values on the SA0 pin, which will provide 125 device address combinations. Note that address 0x4B is allocated for production needs and cannot be used.

Alternatively the PMBus address can be defined by connecting the SA0/SA1 pins according to the table below. SA1 = open for products with no SA1 pin.

		SA0		
		Low	Open	High
SA1	Low	20h	21h	22h
	Open	23h	24h	25h
	High	26h	27h	Reserved

Low = Shorted to PREF
Open = High impedance
High = Logic high, GND as reference,
Logic High definitions see Electrical Specification

Reserved Addresses

Addresses listed in the table below are reserved or assigned according to the SMBus specification and may not be usable. Refer to the SMBus specification for further information.

Address	Comment
0x00	General Call Address / START byte
0x01	CBUS address
0x02	Address reserved for different bus format
0x03 - 0x07	Reserved for future use
0x08	SMBus Host
0x09 - 0x0B	Assigned for Smart Battery
0x0C	SMBus Alert Response Address
0x28	Reserved for ACCESS.bus host
0x2C - 0x2D	Reserved by previous versions of the SMBus specification
0x37	Reserved for ACCESS.bus default address
0x40 - 0x44	Reserved by previous versions of the SMBus specification
0x48 - 0x4B	Unrestricted addresses
0x61	SMBus Device Default Address
0x78 - 0x7B	10-bit slave addressing
0x7C - 0x7F	Reserved for future use

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus Command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Total output current	READ_IOUT
Controller temperature	READ_TEMPERATURE_1
Switching frequency	READ_FREQUENCY
Duty cycle	READ_DUTY_CYCLE

Monitoring Faults

Fault conditions can be monitored using the SALERT pin, which will be asserted low when any number of pre-configured fault or warning conditions occur. The SALERT pin will be held low until faults and/or warnings are cleared by the CLEAR_FAULTS command, or until the output voltage has been re-enabled.

In response to the SALERT signal, the user may read a number of status commands to find out what fault or warning condition occurred, see table below.

Fault & Warning Status	PMBus Command
Overview, Power Good	STATUS_WORD STATUS_BYTE
Output voltage level	STATUS_VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

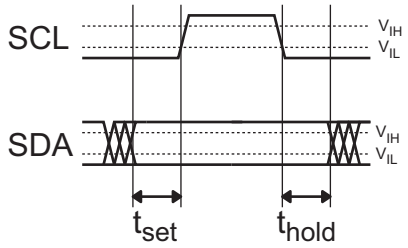
Snapshot Parameter Capture

This product offers a special feature that enables the user to capture parametric data during normal operation by a single PMBus command SNAPSHOT. The following parameters are stored:

- Input voltage
- Output voltage
- Output current
- Controller temperature
- Switching frequency
- Duty cycle
- Status and fault information

When a fault occurs the Snapshot functionality will automatically store this parametric data to NVM. The data can then later be read back to provide valueable information for analysis.

PMBus/I²C Timing



Setup and hold times timing diagram.

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the falling edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. Refer to the SMBus specification, for SMBus electrical and timing requirements.

This product does not support the BUSY flag in the status commands to indicate product being too busy for SMBus response. Instead a bus-free time delay according to this specification must occur between every SMBus transmission (between every stop & start condition).
The product supports PEC (Packet Error Checking) according to the SMBus specification.

When sending subsequent commands to the same module, it is recommended to insert additional delays according to the table below.

After sending PMBus Command	Required delay before additional command
STORE_USER_ALL	100 ms
STORE_DEFAULT_ALL	
RESTORE_USER_ALL	100 ms
RESTORE_DEFAULT_ALL	
VOUT_MAX	10 ms
Any other command	2 ms after reading 10 ms after writing

Non-Volatile Memory (NVM)

The product incorporates two Non-Volatile Memory areas for storage of the PMBus command values; the Default NVM and the User NVM.
The Default NVM is pre-loaded with factory default values. The Default NVM is write-protected and can be used to restore the factory default values through the command RESTORE_DEFAULT_ALL.

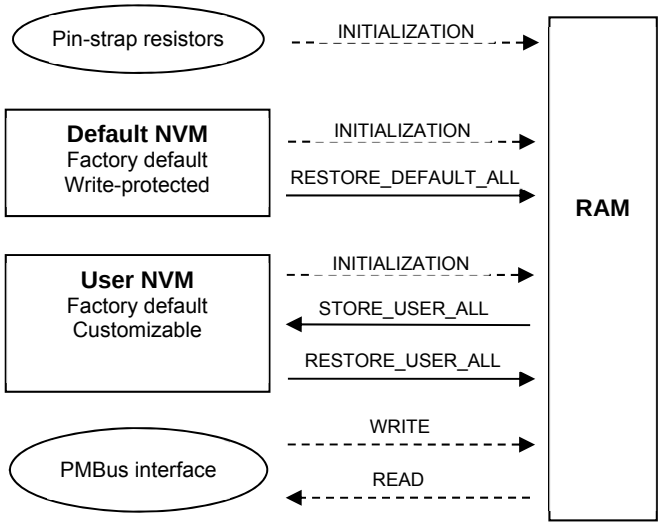


Illustration of memory areas of the product.

The User NVM is pre-loaded with factory default values. The User NVM is writable and open for customization. The values in NVM are loaded during initialization according to section Initialization Procedure, whereafter commands can be changed through the PMBus Interface. The STORE_USER_ALL command will store the changed parameters to the User NVM.

Command Protection

The user may write-protect specific PMBus commands in the User NVM by using the command UNPROTECT.

Initialization Procedure

The product follows an internal initialization procedure after power is applied to the VIN pins:

1. Self test and memory check.
2. The address pin-strap resistors are measured and the associated PMBus address is defined.
3. The output voltage pin-strap resistor is measured and the associated output voltage level will be loaded to operational RAM of PMBus command VOUT_COMMAND.
4. Factory default values stored in default NVM memory are loaded to operational RAM. This overwrites any previously loaded values.
5. Values stored in the User NVM are loaded into operational RAM memory. This overwrites any previously loaded values (e.g. VOUT_COMMAND by pin-strap).
6. Check for external clock signal at the SYNC pin and lock internal clock to the external clock if used.

Once this procedure is completed and the Initialization Time has passed (see Electrical Specification), the output voltage is ready to be enabled using the CTRL pin. The product is also ready to accept commands via the PMBus interface, which in case of writes will overwrite any values loaded during the initialization procedure.

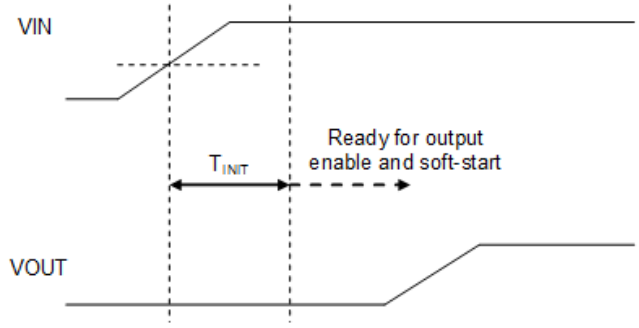


Illustration of Initialization time.

Operating Information

Input Voltage

The input voltage range 4.5-14V makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter.

Input Under Voltage Protection (IUVP)

The product monitors the input voltage and will turn-on and turn-off at configured thresholds (see Electrical Specification). The turn-on input voltage threshold is set higher than the corresponding turn-off threshold. Hence, there is a hysteresis between turn-on and turn-off input voltage levels. Once the input voltage falls below the turn-off threshold, the device can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage while the input voltage is below the turn-on threshold. Operation resumes automatically and the output is enabled when the input voltage has risen above the turn-on threshold.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until the output voltage is re-enabled.

The response for the standard configuration is option 2. The IUVP function can be reconfigured using the PMBus commands VIN_UV_FAULT_LIMIT (turn-off threshold), VIN_UV_WARN_LIMIT (turn-on threshold) and VIN_UV_FAULT_RESPONSE.

Input Over Voltage Protection (IOVP)

The product monitors the input voltage continously and will respond as configured when the input voltage rises above the configured threshold level (see Electrical Specification). Refer to section “Input Under Voltage Protection” for functionality, response configuration options and default setting.
The IOVP function can be reconfigured using the PMBus commands VIN_OV_FAULT_LIMIT (turn-off threshold), VIN_OV_WARN_LIMIT (turn-on threshold) and VIN_OV_FAULT_RESPONSE.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. If the input voltage source contains significant inductance, the addition of a capacitor with low ESR at the input of the product will ensure stable operation.

External Input Capacitors

The input ripple RMS current in a buck converter can be estimated to

$$I_{inputRMS} = I_{load}\sqrt{D(1-D)}$$

Where I_{load} is the output load current and D is the duty cycle. The maximum load ripple current becomes $I_{load}/2$. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor, and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors.

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage at large load transients.

If several products are connected in a phase spreading setup the amount of input ripple current, and capacitance per product, can be reduced. Input capacitors must be placed closely and with low impedance connections to the VIN and GND pins in order to be effective.

External Output Capacitors

The output capacitor requirement depends on two considerations; output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to achieve a small output deviation. Improved transient response can also be achieved by adjusting the settings of the control loop of the product. Adding output capacitance decreases loop band-width.

It is recommended to locate low ESR ceramic and low ESR electrolytic/polymer capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts and cabling in order for capacitance to be effective.

Control Loop

The product uses a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. Although the product uses a digital control loop, it operates much like a traditional analog PWM controller. As in the analog controller case, the control loop compares the output voltage to the desired voltage reference and compensation is added to keep the loop stable and fast. The resulting error signal is used to drive the PWM logic. Instead of using external resistors and capacitors required with traditional analog control loops, the product uses a digital Proportional-Integral-Derivative (PID) compensator in the control loop. The characteristics of the control loop is configured by setting PID compensation parameters. These PID settings can be reconfigured using the PMBus interface.

Control Loop Settings

Product variants without DLC have a standard configuration with a robust control loop compensation setting (PID setting) which allows for a wide range operation of input and output voltages and capacitive loads. For an application with a specific input voltage, output voltage, and capacitive load, the control loop can be optimized for a robust and stable operation and with an improved load transient response. This optimization will minimize the amount of required output decoupling capacitors for a given load transient requirement yielding an optimized cost and minimized board space.

Dynamic Loop Compensation (DLC)

This section applies to product variants with DLC (see section Ordering Information). The DLC feature might in some documents be referred to as "Auto Compensation" or "Auto Tuning" feature.

The DLC feature measures the characteristics of the power train and calculates the proper compensator PID coefficients.

The standard configuration is that once the output voltage ramp up has completed, the DLC algorithm will begin and a new optimized compensator solution (PID setting) will be found and implemented. The DLC algorithm typically takes between 50 ms and 200 ms to complete.

By the PMBus command AUTO_COMP_CONFIG the user may select between several different modes of operation:

- Disable
- Autocomp once, will run DLC algorithm each time the output is enabled (standard configuration)
- Autocomp every second will initiate a new DLC algorithm each 1 second
- Autocomp every minute will initiate a new DLC algorithm every minute.

The DLC can also be configured to run once only after the first ramp up (after input power have been applied) and to use that temporary stored PID settings in all subsequent ramps. If input power is cycled a new DLC algorithm will be performed after the first ramp up. The default setting is however to run the DLC algorithm after every ramp up.

The DLC algorithm can also be initiated manually by sending the AUTO_COMP_CONTROL command.

The DLC can also be configured with Auto Comp Gain Control. This scales the DLC results to allow a trade-off between transient response and steady-state duty cycle jitter. A setting of 100% will provide the fastest transient response while a setting of 10% will produce the lowest jitter. The default is 50%.

Changing DLC and PID Setting

Some caution must be considered while DLC is enabled and when it is changed from enabled or disabled.

When operating, the controller IC uses the settings loaded in its (volatile) RAM memory. When the input power is applied the RAM settings are retrieved from the pin-strap resistors and the two non-volatile memories (DEFAULT and USER). The sequence is described in the "Initialization Procedure" section.

When DLC is enabled:

When DLC is enabled, the normal sequence (after input power has been applied) that a value stored in the user non-volatile memory overwrites any previously loaded value does not apply for the PID setting (stored in the PID_TAPS register). The PID setting in the user non-volatile memory is ignored and a non-configurable default PID setting is loaded to RAM to act as a safe starting value for the DLC. Once the output has been enabled and the DLC algorithm has found a new optimized PID setting, it will be loaded in RAM and used by the control loop.

When saving changes to the user non-volatile memory, all changes made to the content of RAM will be saved. This also includes the default PID setting (loaded to RAM to act as a safe starting value) or the PID setting changed by the DLC algorithm after enabling output. The result is that as long as DLC is enabled the PID setting in the user non-volatile memory is ignored, but it might accidentally get overwritten.

When changing DLC from disabled to enabled:

A non-configurable default PID setting is loaded to RAM to act as a safe starting value for the DLC (same as above).

When changing DLC from enabled to disabled:

When changing DLC from enabled to disabled, the PID setting in the user non-volatile memory will be loaded to RAM. Any new optimized PID setting in RAM will be lost, if not first stored to the user non-volatile memory.

When DLC is disabled:

When DLC is disabled and input power has been applied, the PID setting in the user non-volatile memory will be loaded to RAM and used in the control loop.

The original PID setting in the user non-volatile memory is quite slow and not recommended for optimal performance. If DLC is disabled it is recommended to either:

1. Use the DLC to find optimized PID setting.
2. Use Universal PID as defined below.

The Universal PID setting (taps) is:

A = 1271.9,
B = -2309.9,
C = 1045.2

Write 0x7B82A5FC905F7B9EFD to PID_TAPS register and write command STORE_USER_ALL

Note that if DLC is enabled, for best results V_I must be stable before DLC algorithm begins.

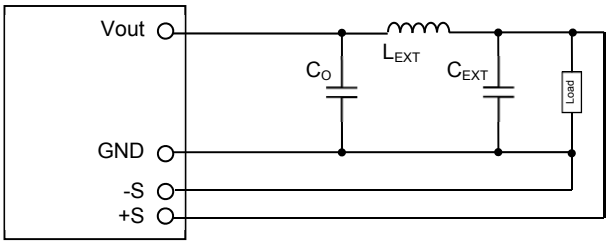
Load Transient Response Optimization (NLR)

The product incorporates a Non-Linear transient Response, NLR, loop that decreases the response time and the output voltage deviation during a load transient. The NLR results in a higher equivalent loop bandwidth than is possible using a traditional linear control loop. The standard configuration has appropriate NLR settings for robust and stable operation for a wide range of input voltage and a capacitive load range as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the NLR configuration can be optimized for a robust and stable operation and with an improved load transient response. This will also reduce the amount of output decoupling capacitors and yield a reduced cost. However, the NLR slightly reduces the efficiency. In order to obtain maximal energy efficiency the load transient requirement has to be met by the standard control loop compensation and the decoupling capacitors. The NLR settings can be reconfigured using the PMBus interface.

Remote Sense

The product has remote sense to compensate the voltage drops between the output and the point of load. The sense traces should be located close to each other and to the PCB ground layer to reduce noise susceptibility. If the remote sense is not needed +S must be connected to VOUT and –S must be connected to GND.

In cases where the external output filter includes an inductor (forming a pi filter) according to the picture below, the L_{EXT}/C_{EXT} resonant frequency places an upper limit on the controller loop bandwidth. If the resonant frequency is high the sense lines can be connected after the filter (as shown in the picture) – if the resonant frequency is low and the DC drop from L_{EXT} is acceptable, sensing before the filter may be better.



External output filter with inductor (pi filter).

Output Voltage Control

To control the output voltage the following options are available:

1. Output voltage is controlled through the CTRL pin.
2. Output voltage is controlled using the PMBus command OPERATION.
3. Output voltage is controlled by CTRL pin and PMBus command OPERATION.
4. Output voltage is controlled to be “always on”.

The CTRL pin can be used with active high (positive) logic or active low (negative) logic.

The setting for the standard configuration is option 1, using positive logic. The output voltage control can be reconfigured using the PMBus command ON_OFF_CONFIG.

The CTRL pin has an internal 10 kΩ pull-up resistor to 5 V. The external device must provide a minimum required sink current to guarantee a voltage not higher than the logic low threshold level (see Electrical Characteristics). When the CTRL pin is left open, the voltage generated on the CTRL pin is max 5.5 V.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to enabling the output voltage.

Output Voltage Adjust using Pin-strap Resistor

Using an external Pin-strap resistor, R_{SET}, the output voltage can be set to several predefined levels shown in the table below. The resistor should be applied between the VSET pin and the PREF pin as shown in the Typical Application Circuit. Maximum 1% tolerance resistors are required.

R_{SET} [kΩ]	V_{OUT} [V]
0 (short)	0.60
10	0.60
11	0.65
12.1	0.70
13.3	0.75
14.7	0.80
16.2	0.85
17.8	0.90
19.6	0.95
21.5	1.00
23.7	1.05

R_{SET} [kΩ]	V_{OUT} [V]
26.1	1.10
28.7	1.15
31.6	1.20
34.8	1.25
38.3	1.30
42.2	1.40
46.4	1.50
51.1	1.60
56.2	1.70
61.9	1.80
Infinite (open)	1.20

R_{SET} also sets the maximum output voltage; see section Output Voltage Range Limitation. The resistor is sensed only during the initialization procedure after application of input voltage. Changing the resistor value during normal operation will not change the output voltage. See Ordering Information for output voltage range.

Output Voltage Adjust using PMBus

The output voltage set by pin-strap can be overridden up to a certain level (see section Output Voltage Range Limitation) by using the PMBus command VOUT_COMMAND. See Electrical Specification for adjustment range.

For current sharing (parallel) operation, VOUT_COMMAND should not be used to change the output voltage on-the-fly. Instead broadcast voltage margining should be used. See sections Voltage Margining Up/Down and Broadcast Control for details.
Note that for product variants with DLC (see Ordering Information) broadcast voltage margining is not supported when ON_OFF_CONFIG is set to output voltage controlled by CTRL pin. Control by PMBus must be set in ON_OFF_CONFIG in order for margining command to be broadcasted to all devices in the current sharing group. This applies also when DLC is disabled.

When setting the output voltage by configuration file or by a PMBus command, the specified output voltage accuracy is valid only when the set output voltage level falls within the same bin range as the voltage level defined by the pin-strap resistor R_{SET}. The applicable bin ranges are defined in the table below. Valid accuracy for voltage levels outside the applicable bin range is two times the specified.

Example:
Nominal V_0 is set to 1.10 V by R_{SET} = 26.1 kΩ. 1.10 V falls within the bin range 0.988-1.383 V, thus specified accuracy is valid when adjusting V_0 within 0.988-1.383V.

V_0 bin ranges [V]
0.600 – 0.988
0.988 – 1.383
1.383 – 1.975
1.975 – 2.398
2.398 – 2.963
2.963 – 3.753

Voltage Margining Up/Down

Using the PMBus interface it is possible to adjust the output voltage to one of two predefined levels above or below the nominal voltage setting in order to determine whether the load device is capable of operating outside its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit outside its supply margin or range. It can also be used to verify the function of supply voltage supervisors. Margin limits of the nominal output voltage are ±5% in standard configuration, but the margin limits can be reconfigured using the PMBus commands VOUT_MARGIN_LOW and VOUT_MARGIN_HIGH. Margining is activated by the command OPERATION and can be used regardless of the output voltage being enabled by the CTRL pin or by the PMBus.

Output Voltage Trim

The actual output voltage can be trimmed to optimize performance of a specific load by setting a non-zero value for PMBus command VOUT_TRIM. The value of VOUT_TRIM is summed with the nominal output voltage set by VOUT_COMMAND, allowing for multiple products to be commanded to a common nominal value, but with slight adjustments per load.
The VOUT_TRIM command is not useable for products in current sharing operation.

Output Voltage Range Limitation

The output voltage range that is possible to set by configuration or by the PMBus interface is hardware limited by the pin-strap resistor R_{SET}. The maximum output voltage is set to 110% of the output value defined by R_{SET}. This protects the application circuit from an over voltage due to an accidental PMBus command.
The limitation applies to the actual regulated output voltage rather than to the configured value. Thus, it is possible to write and read back a VOUT_COMMAND value higher than the limit, but the actual output voltage will be limited.
The output voltage limit can be reconfigured to a *lower* value by writing the PMBus command VOUT_MAX.

Output Voltage Adjust Limitation using PMBus

In addition to the maximum output voltage limitation by the pin-strap resistor R_{SET}, there is also a limitation in how much the output voltage can be increased while the output is enabled. If output is disabled then R_{SET} resistor is the only limitation.

Example:
If the output is enabled with output voltage set to 1.0 V, then it is only possible to adjust/change the output voltage up to 1.7- V as long as the output is enabled.

V_0 setting when enabled [V]	V_0 set range while enabled [V]
0.000 – 0.988	~0.2 to >1.2
0.988 – 1.383	~0.2 to >1.7
1.383 – 1.975	~0.2 to >2.5
1.975 – 2.398	~0.2 to >2.97
2.398 – 2.963	~0.2 to >3.68
2.963 – 3.753	~0.2 to >4.65

Output Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. The product can be configured to respond in different ways to the output voltage exceeding the OVP limit:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continous restart attempts of the output voltage with a preset interval (“hiccup” mode).

The standard configuration setting is option 2. The OVP limit and fault response can be reconfigured using the PMBus commands VOUT_OV_FAULT_LIMIT, VOUT_OV_FAULT_RESPONSE and OVUV_CONFIG.

The standard configuration includes a crowbar function that will close the low side power switch at an OVP shutdown event, in order to force the output voltage to ground level. The crowbar function can be turn off by PMBus command OVUV_CONFIG.

Output Under Voltage Protection (UVP)

The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. Refer to section Output Over Voltage Protection for response configuration options and default setting.
The UVP limit and fault response can be reconfigured using the PMBus commands VOUT_UV_FAULT_LIMIT and VOUT_UV_FAULT_RESPONSE.

Power Good

The power good pin (PG) indicates when the product is ready to provide regulated output voltage to the load. During ramp-up and during a fault condition, PG is held low. In standard configuration, PG is asserted high after the output has ramped to a voltage above 90% of the nominal voltage, and deasserted if the output voltage falls below 85% of the nominal voltage. These thresholds may be changed using the PMBus commands POWER_GOOD_ON and VOUT_UV_FAULT_LIMIT.

The time between when the POWER_GOOD_ON threshold is reached and when the PG pin is actually asserted is set by the PMBus command POWER_GOOD_DELAY. See Electrical Specification for default value and range.
For products with DLC the PG signal is by default asserted directly after the DLC operation has been completed. If DLC is disabled the configured PG delay will be used. This can be reconfigured using the PMBus command AUTO_COMP_CONFIG.

In standard configuration the PG pin is configured as an open drain output but it is also possible to set the output in push-pull mode by the command MFR_CONFIG.

The PG output is not defined during ramp up of the input voltage due to the initialization of the product.

Over Current Protection (OCP)

The product includes robust current limiting circuitry for protection at continuous overload. After ramp-up is complete the product can detect an output overload/short condition. The following OCP response options are available:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continous restart attempts of the output voltage with a preset interval (“hiccup” mode).
3. Immediate shutdown of output voltage followed by a preset number of restart attempts of the output voltage with a preset interval.
4. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until the output voltage is re-enabled.

The standard configuration setting is option 2. Note that delayed shutdown is not supported. The load distribution should be designed for the maximum output short circuit current specified. The OCP limit and response can be reconfigured using the PMBus commands IOUT_AVG_OC_FAULT_LIMIT and MFR_IOUT_OC_FAULT_RESPONSE.

Under Current Protection (UCP)

The product includes robust current limiting circuitry for protection at continuous reversed current, due to a synchronous rectifier ability to sink current. Refer to section Over Current Protection for response configuration options and default setting. The UCP limit and response can be reconfigured using the PMBus commands IOUT_AVG_UC_FAULT_LIMIT and MFR_IOUT_UC_FAULT_RESPONSE.

Switching Frequency

The default switching frequency is chosen as the best tradeoff between efficiency and thermal performance, output ripple and load transient performance. The switching frequency can be re-configured in a certain range using the PMBus command FREQUENCY_SWITCH. Refer to Electrical Specification for default switching frequency and range.
Changing the switching frequency will affect efficiency and power dissipation, load transient response (control loop characteristics) and output ripple. Control loop settings may need to be adjusted.

Synchronization

Two or more products may be synchronized with an external clock to eliminate beat frequencies reflected back to the input supply rail. Eliminating the slow beat frequencies (usually <10 kHz) releases the filtering requirements. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.

The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC output, working as a source of synchronization signal for other products connected to the same synchronization line. The SYNC pin of products being synchronized must be configured as SYNC Input. The standard configuration setting is using the internal clock, independently of signal at the SYNC pin.
Synchronization is configured using PMBus commands USER_CONFIG and MFR_CONFIG.

Phase Spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and efficiency losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized using the SYNC pin.

The phase offset is measured from the rising edge of the applied external clock to the rising edge of the PWM pulse as illustrated below.

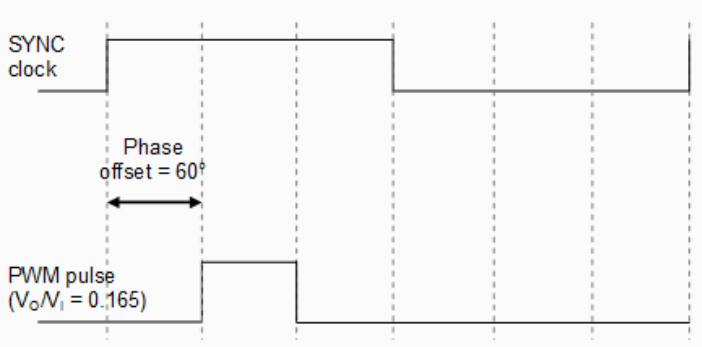


Illustration of phase offset.

The phase offset is configured using the PMBus command INTERLEAVE and is defined as:

$$Phase_offset(^\circ) = 360^\circ \times \frac{Interleave_order}{Number_in_group}$$

Interleave_order is in the range 0-15. *Number_in_group* is in the range 0-15 where a value of 0 means 16. The set resolution for the phase offset is 360° / 16 = 22.5°.

In standard configuration *Number_in_group = 0 and Interleave_order = 2 x* three LSB's of set PMBus address (see section PMBus Addressing).

Soft-start and Soft-stop

The soft-start and soft-stop control functionality allows the output voltage to ramp-up and ramp-down with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple controllers.
The rise time is the time taken for the output to ramp to its target voltage, while the fall time is the time taken for the output to ramp down from its regulation voltage to 0 V. The on delay time sets a delay from when the output is enabled until the output voltage starts to ramp up. The off delay time sets a delay from when the output is disabled until the output voltage starts to ramp down.

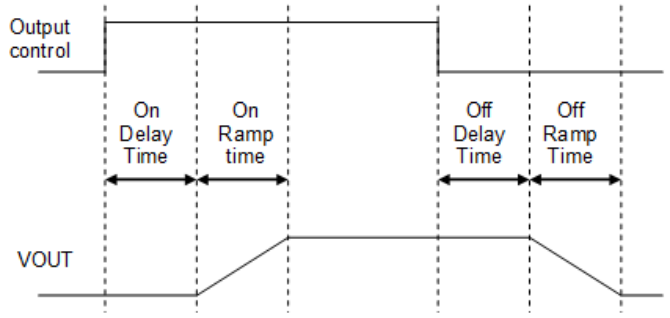


Illustration of Soft-Start and Soft-Stop.

In standard configuration soft-stop is disabled and the regulation of output voltage stops immediately when the output is disabled. Soft-stop can be enabled through the PMBus command ON_OFF_CONFIG. The delay and ramp times can be reconfigured using the PMBus commands TON_DELAY, TON_RISE, TOFF_DELAY and TOFF_FALL.

Output Voltage Sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another.

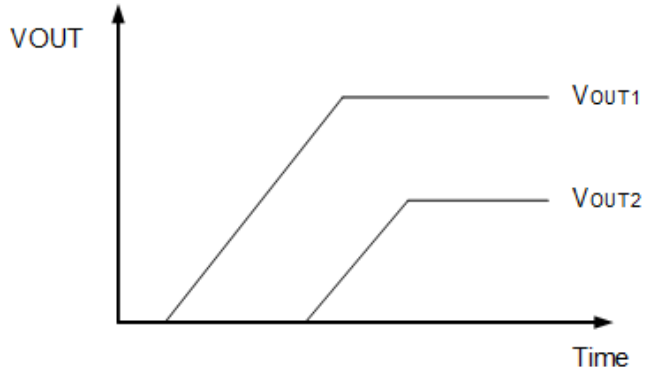


Illustration of Output Voltage Sequencing.

Different types of multi-product sequencing are supported:

1. Time based sequencing. Configuring the start delay and rise time of each module through the PMBus interface and by connecting the CTRL pin of each product to a common enable signal.

2. Event based sequencing. Routing the PG pin signal of one module to the CTRL pin of the next module in the sequence.

3. GCB based sequencing. Power Good triggered sequencing with the same flexibility as time based sequencing. Configured through the PMBus interface and uses the GCB bus, see section Group Communication Bus.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. There could also be still charged output capacitors when starting up shortly after turn-off.
The product incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition.

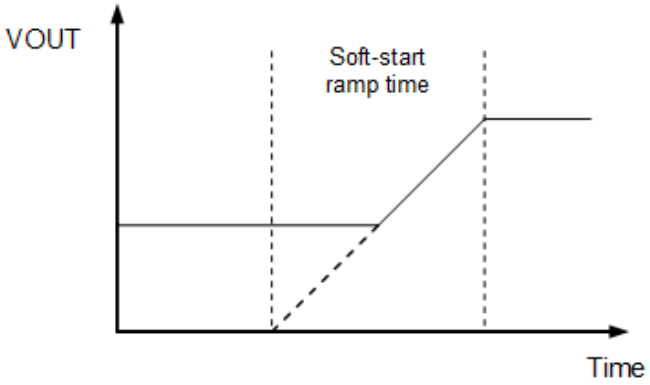


Illustration of Pre-Bias Startup.

Voltage Tracking

The product integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. During ramp-up, the output voltage follows the VTRK voltage until the preset output voltage level is met. The product offers two modes of tracking as follows:

1. Coincident. This mode configures the product to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.

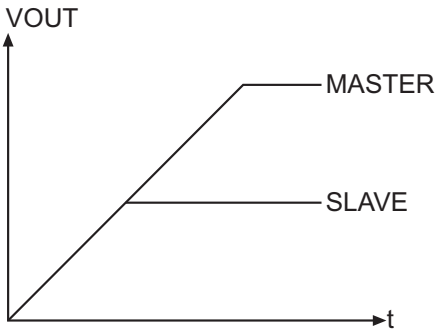


Illustration of Coincident Voltage Tracking.

2. Ratiometric. In this mode the product ramps its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. Ratiometric tracking is achieved by configuring the product for coincident tracking and adding an external resistive voltage divider.

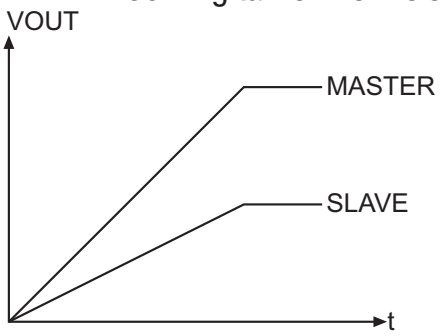


Illustration of Ratiometric Voltage Tracking.

The master device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. Any device configured in tracking mode will ignore its soft-start/stop settings and take on the turn-on/turn-off characteristics of the voltage present at the VTRK pin.
All of the CTRL pins in the tracking group must be connected and driven by a single logic source. Tracking is configured using the PMBus command TRACK_CONFIG.

Group Communication Bus

The Group Communication Bus, GCB, is used to communicate between products. This dedicated single wire bus provides the communication channel between devices for features such as sequencing, fault spreading and current sharing. The GCB solves the PMBus data rate limitation. The GCB pin on all devices in an application should be connected together. A pull-up resistor is required on the common GCB in order to guarantee the rise time as follows:

$$\tau = R_{GCB}\, C_{GCB} \leq 1\,\mu s$$

where R_{GCB} is the pull up resistor value and C_{GCB} is the bus loading. The pull-up resistor should be tied to an external supply voltage in range from 2.5 to 5.5 V, which should be present prior to or during power-up.

The GCB is an internal bus, such that it is only connected across the modules and not the PMBus system host. GCB addresses are assigned on a rail level, i.e. modules within the same current sharing group share the same GCB address. Addressing rails across the GCB is done with a 5 bit GCB ID (command GCB_CONFIG), yielding a theoretical total of 32 rails that can be shared with a single GCB bus.

Parallel Operation (Current Sharing)

Paralleling multiple products can be used to increase the output current capability of a single power rail. By connecting the GCB and SYNC pins of each device and configuring the devices as a current sharing rail, the units will share the current equally, enabling up to 100% utilization of the current capability for each device in the current sharing rail. The product uses a low-bandwidth, first-order digital current sharing by aligning the output voltage of the slave devices to deliver the same current as the master device. Artificial droop resistance is added to the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PWB layout. Up to 8 devices can be configured in a given current sharing group.

Broadcast Control

The product can be configured to broadcast output voltage enable or output voltage margining over the GCB bus to other devices in a group, for example in a current sharing group. If configured to do so, a device receiving a PMBus OPERATION command will broadcast the same command over the GCB bus, and devices on the GCB bus will respond synchronously to the same command, if configured to do so.
Broadcast control is configured using the PMBus command GCB_CONFIG and MISC_CONFIG.

Note that for product variants with DLC (see Ordering Information) broadcast voltage margining is not supported when ON_OFF_CONFIG is set to output voltage controlled by CTRL pin. Control by PMBus must be set in ON_OFF_CONFIG in order for margining command to be broadcasted to all devices in the current sharing group. This applies also when DLC is disabled.

Fault spreading

The product can be configured to broadcast a fault event over the GCB bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the GCB bus. The other devices on the GCB bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so. Fault spreading is configured using the PMBus command GCB_GROUP and USER_CONFIG.

Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at specified V_I.

The product is tested on a 254 x 254 mm, 35 µm (1 oz), test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 16 layers.

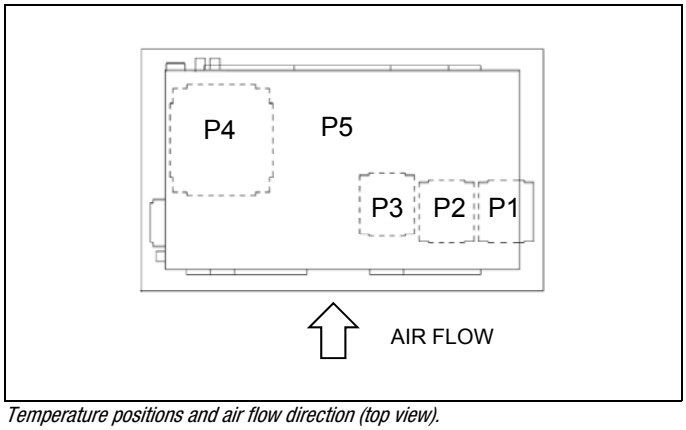
Definition of Product Operating Temperature

The temperature at positions P1, P2, P3, P4 and P5 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above specified maximum measured at the specified positions are not allowed and may cause permanent damage.

Note that the max values are the absolute maximum rating (non destruction) and that the provided Electrical Specification data is guaranteed up to T_{P1} = +95°C.

Position	Description	Max Temperature
P1	T9, Power Switch Reference point	T_{P1} = 130°C
P2	T8, Power Switch Hot spot	T_{P2} = 130°C
P3	T4, Power Switch	T_{P3} = 130°C
P4	N1, Control circuit	T_{P4} = 125°C
P5	L1, Power Inductor	T_{P5} = 125°C

Since it is difficult to access positions P1-P4, measuring the temperature at only position P5 is an alternative method to verify proper thermal conditions. If measuring only T_{P5} the maximum temperature of P5 must be lowered since typically T_{P1}, T_{P2} and T_{P3} will be higher than T_{P5}. Using a temperature limit of 115°C for T_{P5} will make sure that the temperatures at all positions stay below their maximum limits.



Temperature positions and air flow direction (top view).

Definition of Reference Temperature T_{P1}

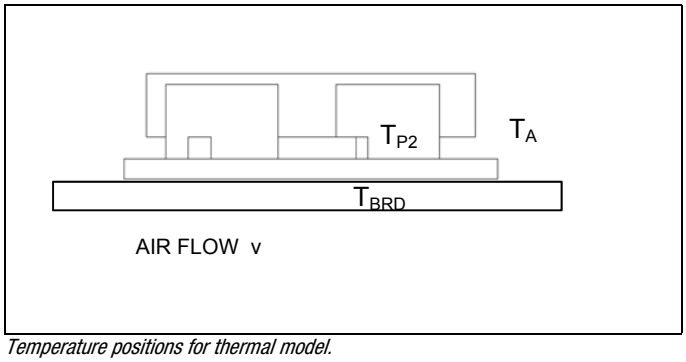
The temperature at position P1 has been used as a reference temperature for the Electrical Specification data provided.

Thermal Model

The thermal model described below can be used to estimate the temperature at the product's hot spot (P2, the point with the highest temperature), based on ambient and board temperatures. The equation can be used to make a first rough estimate of the conditions required to keep the hot spot temperature below specified maximum.

$$T_{P2} = \frac{P_d + \left(\frac{T_A}{R_A} + \frac{T_{BRD}}{R_{BRD}}\right)}{\frac{1}{R_A} + \frac{1}{R_{BRD}}}$$

T_{P2} = Hot spot temperature (°C).
P_d = Power dissipation of module (W).
T_A = Ambient temperature (°C).
$R_A = 58.6\ v^{-0.633}$ (°C/W), where v = Airflow (m/s).
T_{BRD} = Board temperature (°C) (close to module GND pads).
R_{BRD} = 3.3 (°C/W).



Temperature positions for thermal model.

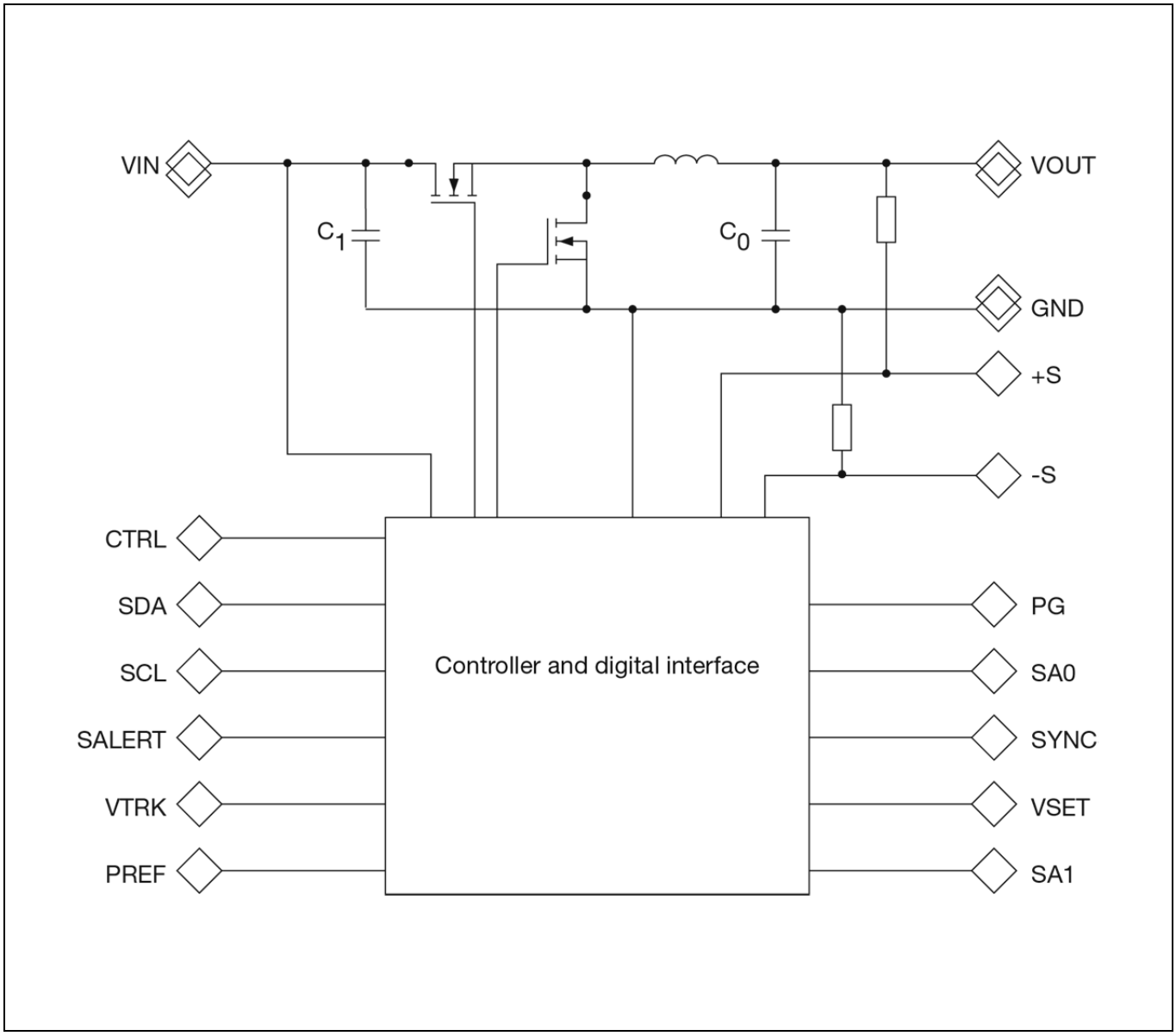
Over Temperature Protection (OTP)

The product is protected from thermal overload by an internal over temperature shutdown function in the controller N1, located in position P4. The temperature T_{P4} is continously monitored and when it rises above the configured fault threshold level the product will respond as configured. The product can respond in several ways as follows:

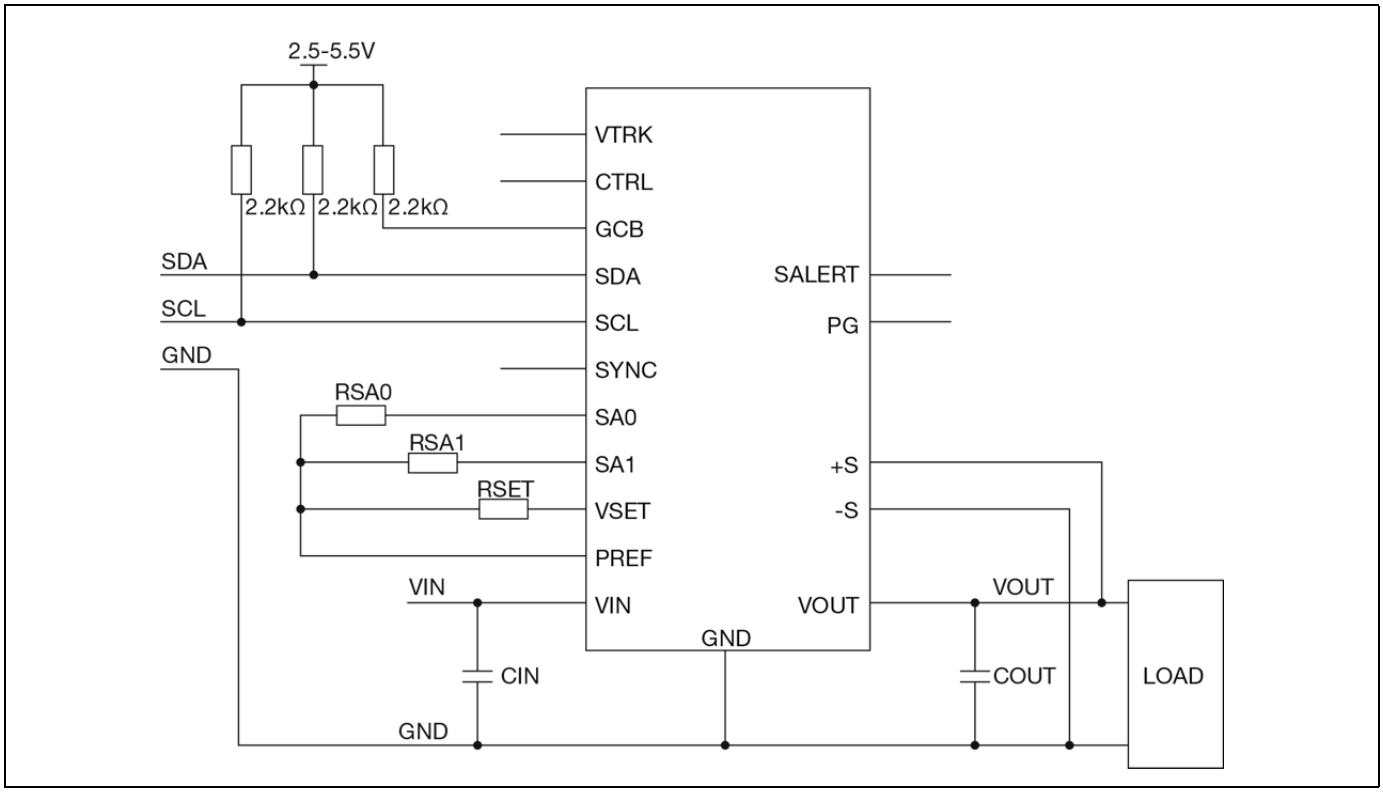
1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage while the temperature is above the warning threshold. Operation resumes automatically and the output is enabled when the temperature has fallen below the warning threshold, i.e. there is a hysteresis defined by the difference between the fault threshold and the warning threshold.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until the output voltage is re-enabled.

The standard configuration setting is option 2. The default OTP thresholds and hysteresis are specified in Electrical Characteristics.
The OTP limit, hysteresis and response are configured using the PMBus commands OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE.

Internal Circuit Diagram

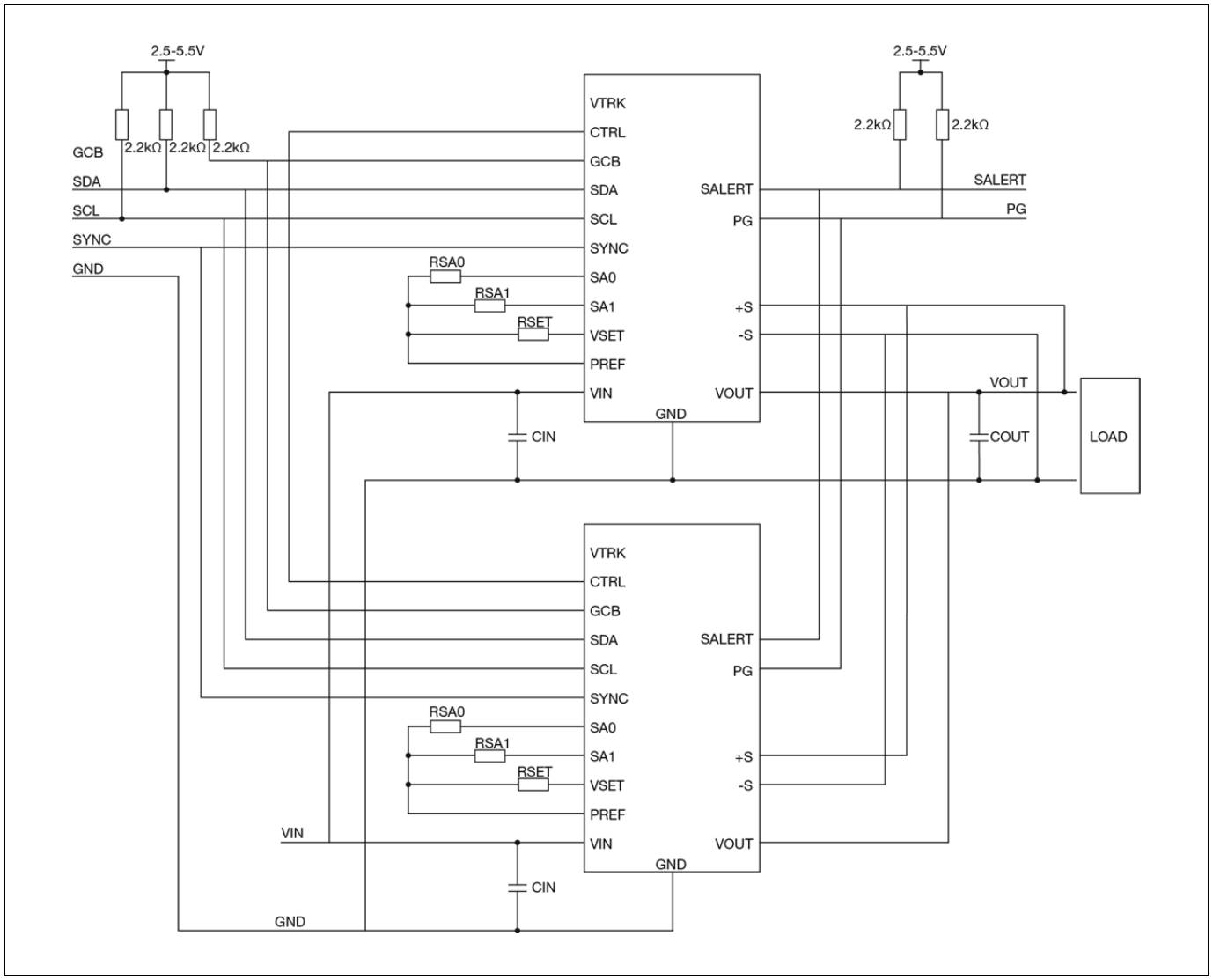


Typical Application Circuit



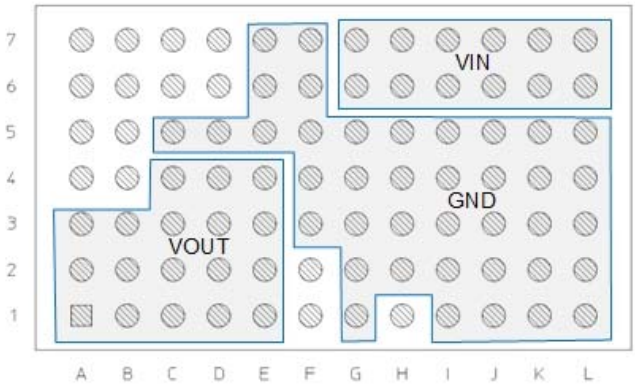
Standalone operation with PMBus communication.

Typical Application Circuit – Parallel Operation



Parallel operation.

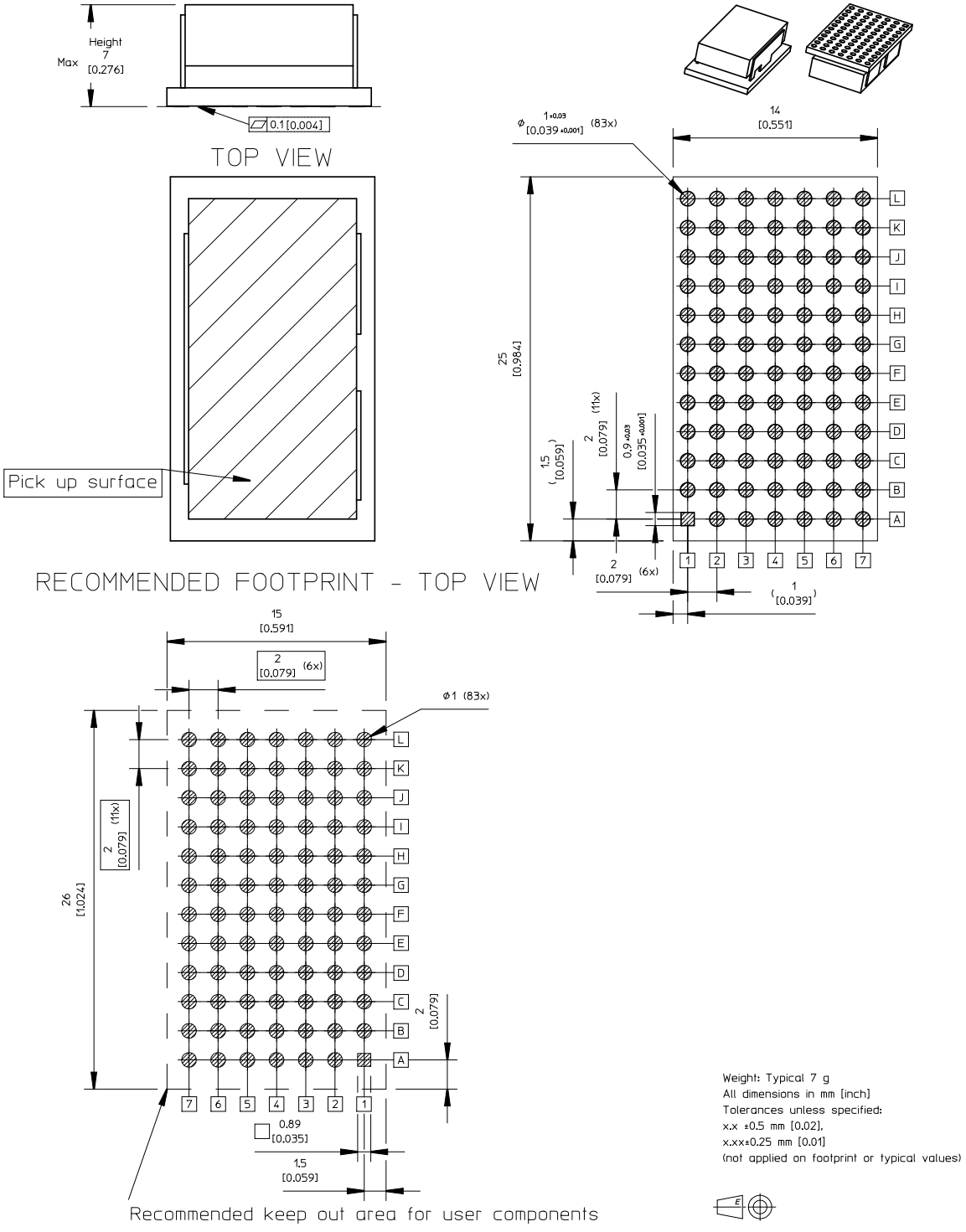
Pin Descriptions



Pin layout, top view.

Pin	Designation	Type	Function
1A-1E, 2A-2E, 3A-3E, 4C-4E	VOUT	Power	Output voltage
1G, 1I-1L, 2G-2L, 3F-3L, 4F-4L, 5C-5L, 6E-6F, 7E-7F	GND	Power	Power and digital ground.
6G-6L,7G-7L	VIN	Power	Input voltage
1F	+S	I	Positive sense. Connect to output voltage close to the load
2F	-S	I	Negative sense. Connect to power ground close to the load.
1H	SW	O	Connected to internal switch node. Should be left unconnected.
4A	SALERT	O Open Drain	PMBus Alert. Asserted low when any of the configured protection mechanisms indicate a fault.
4B	SCL	I	PMBus Clock. Clock for PMBus communication. Requires a pull-up resistor, also when unused. See section PMBus Interface.
5B	SDA	I/O	PMBus Data. Data signal for PMBus communication. Requires a pull-up resistor, also when unused. See section PMBus Interface.
5A	VSET	I	Output voltage pin strap. Used with external resistor to set the nominal level and limit of output voltage. See Output Voltage sections.
6A	SA0	I	PMBus address pin strap. Used with external resistors to assign a unique PMBus address to the product. May be left open if PMBus is not used. See section PMBus Interface.
6B	SA1	I	
6C	VTRK	I	Voltage Tracking input. Allows for tracking of output voltage to an external voltage. See section Voltage Tracking.
6D	GCB	I/O	Group Communication Bus. Used for current sharing, and inter- device communication. See section Group Communication Bus.
7A	PREF	Power	Pin-strap reference. Ground reference for pin-strap resistors.
7B	SYNC	I/O	External switching frequency synchronization input. May be left open if unused. See section Synchronization.
7C	PG	O Open Drain	Power Good output. Asserted high when the product is ready to provide regulated output voltage to the load. See section Power Good.
7D	CTRL	I	Remote Control. Used to enable/disable the output of the product. May be left open if unused due to internal pull-up. See section Remote Control.

Mechanical Information



Weight: Typical 7 g
All dimensions in mm [inch]
Tolerances unless specified:
x.x ±0.5 mm [0.02],
x.xx±0.25 mm [0.01]
(not applied on footprint or typical values)

All component placements – whether shown as physical components or symbolical outline – are for reference only and are subject to change throughout the product's life cycle, unless explicitly described and dimensioned in this drawing.

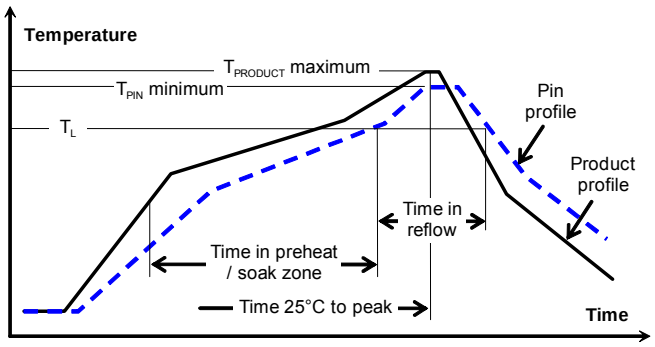
Soldering Information – Surface Mounting and Hole Mount through Pin in Paste Assembly

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PWB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up ($T_{PRODUCT}$)		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above T_L		30 s	30 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	$T_{PRODUCT}$	225°C	260°C
Average ramp-down ($T_{PRODUCT}$)		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Pin number 3C is chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L, 183°C for Sn63Pb37) for more than 30 seconds and a peak temperature of 210°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L, 217 to 221°C for SnAgCu solder alloys) for more than 30 seconds and a peak temperature of 235°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

Top of the product PCB near pin A2 or A5 is chosen as reference locations for the maximum (peak) allowed product temperature (TPRODUCT) since these will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

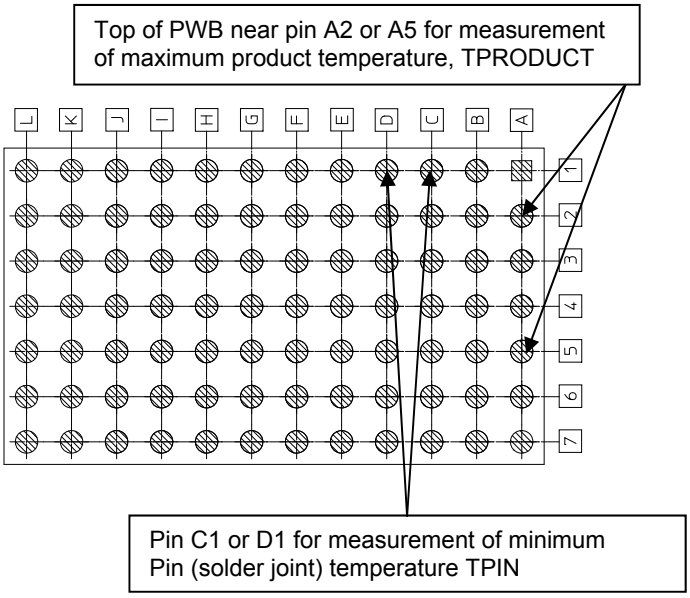
During reflow $T_{PRODUCT}$ must not exceed 260 °C at any time.

Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Thermocoupler Attachment



Surface Mount Assembly and Repair

The LGA of the product require particular care during assembly since the LGA´s are hidden between the host board and the product's PCB. Special procedures are required for successful rework of these products.

Assembly

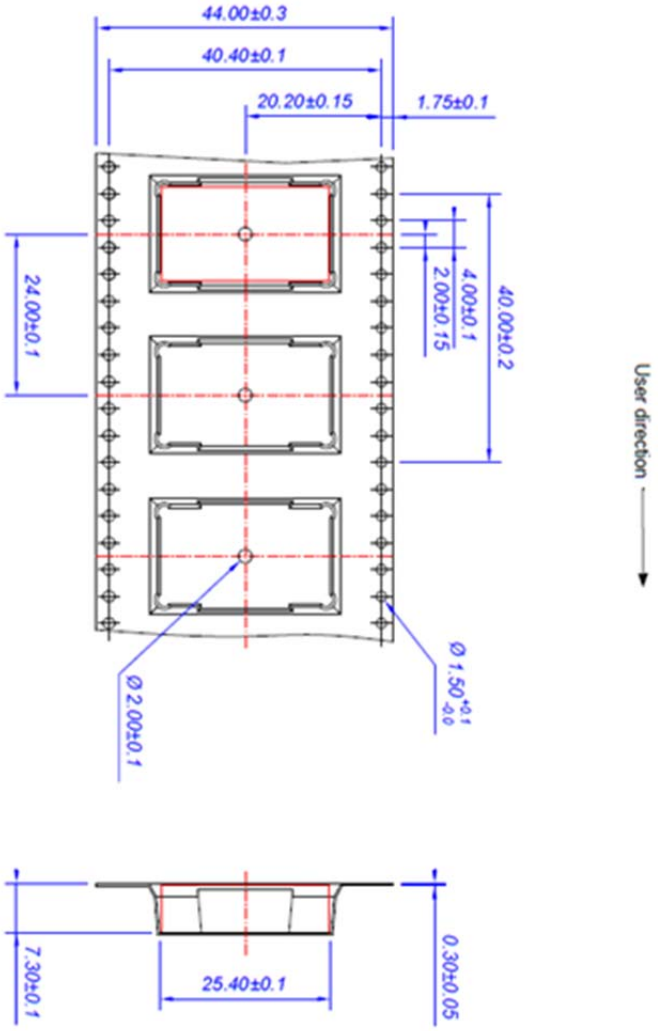
Automatic pick and place equipment should be used to mount the product on the host board. The use of a vision system, utilizing the fiducials on the bottom side of the product, will ensure adequate accuracy. Manual mounting of solder bump products is not recommended.

This module is not recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

Repair

For a successful repair (removal and replacement) of a LGA product, a dedicated rework system should be used. The rework system should preferably utilize a reflow station and a bottom side heater might also be needed for the operation.

The product is an open frame design with a pick up surface on a large central component (in this case the choke). This pick up surface can be used for removal of the module provided that it is glued against module PCB before removal to prevent it from separating from the module PCB.



Delivery Package Information

The products are delivered in antistatic carrier tape (EIA 481 standard)

Carrier Tape Specifications	
Material	PS, antistatic
Surface resistance	< 10^7 Ohm/square
Bakeability	The tape is not bakable
Tape width, W	44 mm [1.73 inch]
Pocket pitch, P_1	24 mm [0.95 inch]
Pocket depth, K_0	7.3 mm [0.287 inch]
Reel diameter	396 mm [15.6 inch]
Reel capacity	320 products /reel
Reel weight	2870 g/full reel

Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T_A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether Isopropyl alcohol	55°C 35°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity	J-STD-020E	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g^2/Hz 10 min in each 3 perpendicular directions

Appendix - PMBus Commands

This appendix contains a detailed reference of the PMBus commands supported by the product.

Data Formats

The products make use of a few standardized numerical formats, along with custom data formats. A detailed walkthrough of the above formats is provided in sections 7 and 8 of the PMBus Specification Part II. The custom data formats vary depending on the command, and are detailed in the command description.

Standard Commands

The functionality of commands with code 0x00 to 0xCF is usually based on the corresponding command specification provided in the PMBus Standard Specification Part II (see Power System Management Bus Protocol Documents below). However there might be different interpretations of the PMBus Standard Specification or only parts of the Standard Specification applied, thus the detailed command description below should always be consulted.

Forum Websites

The System Management Interface Forum (SMIF)
http://www.powersig.org/
The System Management Interface Forum (SMIF) supports the rapid advancement of an efficient and compatible technology base that promotes power management and systems technology implementations. The SMIF provides a membership path for any company or individual to be active participants in any or all of the various working groups established by the implementer forums.

Power Management Bus Implementers Forum
(PMBUS-IF)
http://pmbus.org/
The PMBus-IF supports the advancement and early adoption of the PMBus protocol for power management. This website offers recent PMBus specification documents, PMBus articles, as well as upcoming PMBus presentations and seminars, PMBus Document Review Board (DRB) meeting notes, and other PMBus related news.

PMBus – Power System Management Bus Protocol Documents

These specification documents may be obtained from the PMBus-IF website described above. These are required reading for complete understanding of the PMBus implementation. This appendix will not re-address all of the details contained within the two PMBus Specification documents.

Specification Part I – General Requirements Transport And Electrical Interface
Includes the general requirements, defines the transport and electrical interface and timing requirements of hard wired signals.

Specification Part II – Command Language
Describes the operation of commands, data formats, fault management and defines the command language used with the PMBus.

SMBus – System Management Bus Documents

System Management Bus Specification, Version 2.0, August 3, 2000
This specification specifies the version of the SMBus on which Revision 1.2 of the PMBus Specification is based. This specification is freely available from the System Management Interface Forum Web site at:
http://www.smbus.org/specs/

PMBus Command Summary and Factory Default Values

The default values provided in the table below is valid for the specified variant.

Code	Name	Data Format	Factory Default Value	
0x01	OPERATION	R/W Byte	0x04	
0x02	ON_OFF_CONFIG	R/W Byte	0x17	
0x03	CLEAR_FAULTS	Send Byte		
0x11	STORE_DEFAULT_ALL	Send Byte		
0x12	RESTORE_DEFAULT_ALL	Send Byte		
0x15	STORE_USER_ALL	Send Byte		
0x16	RESTORE_USER_ALL	Send Byte		
0x20	VOUT_MODE	Read Byte	0x13	
0x21	VOUT_COMMAND	R/W Word		
0x22	VOUT_TRIM	R/W Word	0x0000	0.0 V
0x23	VOUT_CAL_OFFSET	R/W Word	Unit Specific	
0x24	VOUT_MAX	R/W Word		
0x25	VOUT_MARGIN_HIGH	R/W Word		
0x26	VOUT_MARGIN_LOW	R/W Word		
0x27	VOUT_TRANSITION_RATE	R/W Word	0xBA00	1.0 V/ms
0x28	VOUT_DROOP	R/W Word	0x0000	0.0 mV/A
0x32	MAX_DUTY	R/W Word	0xEAF8	95.0 %
0x33	FREQUENCY_SWITCH	R/W Word	0xFA80	320.0 kHz
0x37	INTERLEAVE	R/W Word		
0x38	IOUT_CAL_GAIN	R/W Word	Unit Specific	
0x39	IOUT_CAL_OFFSET	R/W Word	Unit Specific	
0x40	VOUT_OV_FAULT_LIMIT	R/W Word		
0x41	VOUT_OV_FAULT_RESPONSE	R/W Byte	0xBF	
0x44	VOUT_UV_FAULT_LIMIT	R/W Word		
0x45	VOUT_UV_FAULT_RESPONSE	R/W Byte	0xBF	
0x46	IOUT_OC_FAULT_LIMIT	R/W Word	0xEAB8	87.0 A
0x4B	IOUT_UC_FAULT_LIMIT	R/W Word	0xDC40	-30.0 A
0x4F	OT_FAULT_LIMIT	R/W Word	0xEBE8	125.0 °C
0x50	OT_FAULT_RESPONSE	R/W Byte	0xBF	
0x51	OT_WARN_LIMIT	R/W Word	0xEB70	110.0 °C
0x52	UT_WARN_LIMIT	R/W Word	0xE4E0	-50.0 °C
0x53	UT_FAULT_LIMIT	R/W Word	0xE490	-55.0 °C
0x54	UT_FAULT_RESPONSE	R/W Byte	0xBF	
0x55	VIN_OV_FAULT_LIMIT	R/W Word	0xDA00	16.0 V
0x56	VIN_OV_FAULT_RESPONSE	R/W Byte	0xBF	
0x57	VIN_OV_WARN_LIMIT	R/W Word	0xD3C0	15.0 V
0x58	VIN_UV_WARN_LIMIT	R/W Word	0xCA1A	4.2 V
0x59	VIN_UV_FAULT_LIMIT	R/W Word	0xC3DA	3.9 V
0x5A	VIN_UV_FAULT_RESPONSE	R/W Byte	0xBF	
0x5E	POWER_GOOD_ON	R/W Word		
0x60	TON_DELAY	R/W Word	0xCA80	5.0 ms
0x61	TON_RISE	R/W Word	0xCA80	5.0 ms

Code	Name	Data Format	Factory Default Value	
0x64	TOFF_DELAY	R/W Word	0xCA80	5.0 ms
0x65	TOFF_FALL	R/W Word	0xCA80	5.0 ms
0x78	STATUS_BYTE	Read Byte		
0x79	STATUS_WORD	Read Word		
0x7A	STATUS_VOUT	Read Byte		
0x7B	STATUS_IOUT	Read Byte		
0x7C	STATUS_INPUT	Read Byte		
0x7D	STATUS_TEMPERATURE	Read Byte		
0x7E	STATUS_CML	Read Byte		
0x80	STATUS_MFR_SPECIFIC	Read Byte		
0x88	READ_VIN	Read Word		
0x8B	READ_VOUT	Read Word		
0x8C	READ_IOUT	Read Word		
0x8D	READ_TEMPERATURE_1	Read Word		
0x94	READ_DUTY_CYCLE	Read Word		
0x95	READ_FREQUENCY	Read Word		
0x98	PMBUS_REVISION	Read Byte		
0x99	MFR_ID	R/W Block (22)	Unit Specific	
0x9A	MFR_MODEL	R/W Block (14)	Unit Specific	
0x9B	MFR_REVISION	R/W Block (24)	Unit Specific	
0x9C	MFR_LOCATION	R/W Block (7)	Unit Specific	
0x9D	MFR_DATE	R/W Block (10)	Unit Specific	
0x9E	MFR_SERIAL	R/W Block (13)	Unit Specific	
0xB0	USER_DATA_00	R/W Block (23)	Unit Specific	
0xBC	AUTO_COMP_CONFIG	R/W Byte	0x49	
0xBD	AUTO_COMP_CONTROL	Send Byte		
0xBF	DEADTIME_MAX	R/W Word	0x3C3C	60 ns, 60 ns
0xD0	MFR_CONFIG	R/W Word	0xAB10	
0xD1	USER_CONFIG	R/W Word	0x2001	
0xD2	ISHARE_CONFIG	R/W Word	0x0000	
0xD3	GCB_CONFIG	R/W Word	0x0000	
0xD4	POWER_GOOD_DELAY	R/W Word	0xC200	2.0 ms
0xD5	PID_TAPS	R/W Block (9)	0x75B241F6AB2775F40C	
0xD6	INDUCTOR	R/W Word	0xA2E1	0.2 µH
0xD7	NLR_CONFIG	R/W Block (4)	0xFF111144	
0xD8	OVUV_CONFIG	R/W Byte	0x8F	
0xD9	XTEMP_SCALE	R/W Word	0xBA00	
0xDA	XTEMP_OFFSET	R/W Word	0x8000	0.0 °C
0xDB	VOUT_MAX_LIMIT	Read Word		
0xDC	TEMPCO_CONFIG	R/W Byte	0x26	38 100ppm/°C
0xDD	DEADTIME	R/W Word	0x0014	20 ns, 0 ns
0xDE	DEADTIME_CONFIG	R/W Word	0x0887	7 x 2ns, 8 x 2ns
0xE0	SEQUENCE	R/W Word	0x0000	
0xE1	TRACK_CONFIG	R/W Byte	0x00	
0xE2	GCB_GROUP	R/W Block (4)	0x00000000	
0xE4	DEVICE_ID	Read Block (16)		
0xE5	MFR_IOUT_OC_FAULT_RESPONSE	R/W Byte	0xBF	
0xE6	MFR_IOUT_UC_FAULT_RESPONSE	R/W Byte	0xBF	

Code	Name	Data Format	Factory Default Value	
0xE7	IOUT_AVG_OC_FAULT_LIMIT	R/W Word	0xEA60	76.0 A
0xE8	IOUT_AVG_UC_FAULT_LIMIT	R/W Word	0xDC40	-30.0 A
0xE9	MISC_CONFIG	R/W Word	0x2002	
0xEA	SNAPSHOT	Read Block (32)		
0xEB	BLANK_PARAMS	Read Block (16)		
0xF0	PHASE_CONTROL	R/W Byte	0x00	
0xF3	SNAPSHOT_CONTROL	R/W Byte	0x00	
0xFA	SECURITY_LEVEL	Read Byte		
0xFB	PRIVATE_PASSWORD	R/W Block (9)	Unit Specific	
0xFC	PUBLIC_PASSWORD	R/W Block (4)	Unit Specific	
0xFD	UNPROTECT	R/W Block (32)	Unit Specific	

PMBus Command Details

OPERATION (0x01)
Transfer Type: R/W Byte
Description: Controls enable and margin operations.

Bit	Function	Description	Value	Function	Description
7:6	Enable	Make the device enable or disable.	00	Immediate Off	Disable Immediately without sequencing.
			01	Soft Off	Disable "Softly" with sequencing.
			10	Enable	Enable device to the desired margin state.
5:4	Margin	Select between margin high/low states or nominal output.	00	Nominal	Operate at nominal output voltage.
			01	Margin Low	Operate at margin low voltage set in VOUT_MARGIN_LOW.
			10	Margin High	Operate at margin high voltage set in VOUT_MARGIN_HIGH.
3:2	Act on Fault	Set 10b to act on fault or set to 01b to ignore fault.	01	Ignore Faults	Ignore Faults when in a margined state. The device will ignore appropriate overvoltage/undervoltage warnings and faults and respond as programmed by the warning limit or fault response command.
			10	Act on Faults	Act on Faults when in a margined state. The device will handle appropriate overvoltage/undervoltage warnings and faults and respond as programmed by the warning limit or fault response command.

ON_OFF_CONFIG (0x02)
Transfer Type: R/W Byte
Description: Configures how the device is controlled by the CTRL pin and the PMBus.

Bit	Function	Description	Value	Function	Description
4	Powerup Operation	Sets the default to either operate any time power is present or for the on/off to be controlled by CTRL pin and PMBus commands.	0	Enable Always	Unit powers up any time power is present regardless of state of the CTRL pin.
			1	CTRL pin or PMBus	Unit does not power up until commanded by the CTRL pin and OPERATION command.
3	PMBus Enable Mode	Controls how the unit responds to commands received via the PMBus.	0	Ignore PMBus command	Unit ignores the on/off portion of the OPERATION command from serial bus.
			1	Use PMBus command	To start, the unit requires that the on/off portion of the OPERATION command is instructing the unit to run.
2	Enable Pin Mode	Controls how the unit responds to the CTRL pin.	0	Ignore CTRL pin	Unit ignores the CTRL pin.
			1	Use CTRL pin	Unit requires the CTRL pin to be asserted to start the unit.
1	Enable Pin Polarity	Polarity of the CTRL pin.	0	Active Low	CTRL pin will cause device to enable when driven low.
			1	Active High	CTRL pin will cause device to enable when driven high.
0	Disable Action	CTRL pin action when commanding the output to turn off.	0	Soft Off	Use the configured turn off delay and fall time.
			1	Immediate Off	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

CLEAR_FAULTS (0x03)
Transfer Type: Send Byte
Description: Clears all fault status bits

STORE_DEFAULT_ALL (0x11)
Transfer Type: Send Byte
Description: Commands the device to store its configuration into the Default Store.

RESTORE_DEFAULT_ALL (0x12)
Transfer Type: Send Byte
Description: Commands the device to restore its configuration from the Default Store.

STORE_USER_ALL (0x15)
Transfer Type: Send Byte
Description: Stores, at the USER level, all PMBus values that were changed since the last restore command. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. Wait 20 ms after a STORE_USER_ALL command before issuing another PMBus command.

RESTORE_USER_ALL (0x16)
Transfer Type: Send Byte
Description: Restores PMBus settings that were stored using STORE_USER_ALL. This command is automatically performed at power up. The values restored will overwrite the values previously loaded by the RESTORE_DEFAULT_ALL command. The security level is changed to Level 1 following this command. Wait 20 ms after a RESTORE_USER_ALL command before issuing another PMBus command.

VOUT_MODE (0x20)
Transfer Type: Read Byte
Description: Controls how future VOUT-related commands parameters will be interpreted.

Bit	Function	Description	Format
4:0		Five bit two's complement EXPONENT for the MANTISSA delivered as the data bytes for VOUT_COMMAND in VOUT_LINEAR Mode five bit VID code identifier per in VID Mode or always set to 00000b in Direct Mode.	Integer Signed

Bit	Function	Description	Value	Function	Description
7:5		Selection of mode for representation of output voltage parameters.	000	Linear	Linear Mode Format.
			001	VID	VID Mode.
			010	Direct	Direct Mode.

VOUT_COMMAND (0x21)
Transfer Type: R/W Word
Description: Commands the device to transition to a new output voltage.

Bit	Description	Format	Unit
15:0	Sets the nominal value of the output voltage. Factory default value is controlled by VSET pin-strap.	Vout Mode Unsigned	V

VOUT_TRIM (0x22)
Transfer Type: R/W Word
Description: Configures a fixed offset to be applied to the output voltage when enabled.

Bit	Description	Format	Unit
15:0	Sets VOUT trim value. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent set in VOUT_MODE.	Vout Mode Signed	V

VOUT_CAL_OFFSET (0x23)
Transfer Type: R/W Word
Description: Configures a fixed offset to be applied to the output voltage when enabled.

Bit	Description	Format	Unit
15:0	Sets VOUT calibration offset(same function as VOUT_TRIM). The two bytes are formatted as a two's complement binary mantissa, used in conjuction with the exponent set in VOUT_MODE.	Vout Mode Signed	V

VOUT_MAX (0x24)
Transfer Type: R/W Word
Description: Configures the maximum allowed output voltage.

Bit	Description	Format	Unit
15:0	If the device is commanded to a Vout value higher than this level, the output voltage will be clamped to this level. The max VOUT_MAX setting is 110% of the VSET pin-strap setting.	Vout Mode Unsigned	V

VOUT_MARGIN_HIGH (0x25)
Transfer Type: R/W Word
Description: Configures the target for margin-up commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin high. Factory default value is controlled by VSET pin-strap.	Vout Mode Unsigned	V

VOUT_MARGIN_LOW (0x26)
Transfer Type: R/W Word
Description: Configures the target for margin-down commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin low. Factory default value is controlled by VSET pin-strap.	Vout Mode Unsigned	V

VOUT_TRANSITION_RATE (0x27)
Transfer Type: R/W Word
Description: Configures the transition time for margins and VCOMMAND output changes.

Bit	Description	Format	Unit
15:0	Configures the transition time for margining and on-the-fly VOUT_COMMAND changes.	Linear	V/ms

VOUT_DROOP (0x28)
Transfer Type: R/W Word
Description: Configures the Isense voltage to load current ratio.

Bit	Description	Format	Unit
15:0	Sets the effective load line (V/I slope) for the rail in which the device is used.	Linear	mV/A

MAX_DUTY (0x32)
Transfer Type: R/W Word
Description: Configures the maximum allowed duty-cycle.

Bit	Description	Format	Unit
15:0	Value 0-100%. Sets the maximum allowable duty cycle of the switching frequency.	Linear	%

FREQUENCY_SWITCH (0x33)
Transfer Type: R/W Word
Description: Controls the switching frequency in 1kHz steps.

Bit	Description	Format	Unit
15:0	This parameter sets the switching frequency. The specified range is 200 - 640 kHz. Note: Changing the switching frequency means that the compensation and deadtime parameters have to be considered for redesign.	Linear	kHz

INTERLEAVE (0x37)
Transfer Type: R/W Word
Description: Configures the phase offset with respect to a common SYNC clock.

Bit	Function	Description	Format
11:8	Group ID Number	Value 0-15. Sets an ID number to a group of interleaved rails. This field is optional. Factory default value = 0.	Integer Unsigned
7:4	Number of Rails	Value 0-15. Sets the number of rails in the group. A value of 0 is interpreted as 16. Factory default value = 0.	Integer Unsigned
3:0	Rail Position	Value 0-15. Sets position of the device's rail within the group. Factory default value = Four LSB's of set PMBus address (SA pinstrap).	Integer Unsigned

IOUT_CAL_GAIN (0x38)
Transfer Type: R/W Word
Description: Sets the current sense resistance.

Bit	Description	Format	Unit
15:0	Sets the effective impedance for current sensing at +25°C.	Linear	mΩ

IOUT_CAL_OFFSET (0x39)
Transfer Type: R/W Word
Description: Sets the current-sense offset.

Bit	Description	Format	Unit
15:0	Sets an offset to IOUT readings. Use to compensate for delayed measurements of current ramp.	Linear	A

VOUT_OV_FAULT_LIMIT (0x40)
Transfer Type: R/W Word
Description: Sets the VOUT overvoltage fault threshold.

Bit	Description	Format	Unit
15:0	Sets the VOUT overvoltage fault threshold. Factory default value is controlled by VSET pin-strap.	Vout Mode Unsigned	V

VOUT_OV_FAULT_RESPONSE (0x41)
Transfer Type: R/W Byte
Description: Sets the VOUT OV fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable until clear	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times.
			011	Retry 3 times	The PMBus device attempts to restart 3 times.
			100	Retry 4 times	The PMBus device attempts to restart 4 times.
			101	Retry 5 times	The PMBus device attempts to restart 5 times.
			110	Retry 6 times	The PMBus device attempts to restart 6 times.

Bit	Function	Description	Value	Function	Description
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Number of delay time units. Used for either the amount of time the device (10 ms/unit) is to continue operating after a fault is detected or for the amount of time (8.2 ms/unit) between attempts to restart.	0	0	
			1	1	
			2	2	
			3	3	
			4	4	
			5	5	
			6	6	
			7	7	

VOUT_UV_FAULT_LIMIT (0x44)
Transfer Type: R/W Word
Description: Sets the VOUT under-voltage fault threshold. This threshold is also used for deasserting PG (Power Good).

Bit	Description	Format	Unit
15:0	Sets the VOUT under-voltage fault threshold. Factory default value is controlled by VSET pin-strap.	Vout Mode Unsigned	V

VOUT_UV_FAULT_RESPONSE (0x45)
Transfer Type: R/W Byte
Description: Sets the VOUT UV LIMIT Response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable until clear	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.

Bit	Function	Description	Value	Function	Description
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times.
			011	Retry 3 times	The PMBus device attempts to restart 3 times.
			100	Retry 4 times	The PMBus device attempts to restart 4 times.
			101	Retry 5 times	The PMBus device attempts to restart 5 times.
			110	Retry 6 times	The PMBus device attempts to restart 6 times.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Number of delay time units. Used for either the amount of time the device (10 ms/unit) is to continue operating after a fault is detected or for the amount of time (8.2 ms/unit) between attempts to restart.	0	0	
			1	1	
			2	2	
			3	3	
			4	4	
			5	5	
			6	6	
			7	7	

IOUT_OC_FAULT_LIMIT (0x46)
Transfer Type: R/W Word
Description: Sets the output over-current peak limit.

Bit	Description	Format	Unit
15:0	Sets the IOUT overcurrent peak fault threshold.	Linear	A

IOUT_UC_FAULT_LIMIT (0x4B)
Transfer Type: R/W Word
Description: Sets the output under-current peak limit.

Bit	Description	Format	Unit
15:0	Sets the IOUT undercurrent peak fault threshold.	Linear	A

OT_FAULT_LIMIT (0x4F)
Transfer Type: R/W Word
Description: Sets the over-temperature fault limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature fault threshold.	Linear	°C

OT_FAULT_RESPONSE (0x50)
Transfer Type: R/W Byte
Description: Sets the over-temperature fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable until clear	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.

Bit	Function	Description	Value	Function	Description
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times.
			011	Retry 3 times	The PMBus device attempts to restart 3 times.
			100	Retry 4 times	The PMBus device attempts to restart 4 times.
			101	Retry 5 times	The PMBus device attempts to restart 5 times.
			110	Retry 6 times	The PMBus device attempts to restart 6 times.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Number of delay time units. Used for either the amount of time the device (80 ms/unit) is to continue operating after a fault is detected or for the amount of time (32 ms/unit) between attempts to restart.	0	0	
			1	1	
			2	2	
			3	3	
			4	4	
			5	5	
			6	6	
			7	7	

OT_WARN_LIMIT (0x51)
Transfer Type: R/W Word
Description: Sets the over-temperature warning limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature warning threshold.	Linear	°C

UT_WARN_LIMIT (0x52)
Transfer Type: R/W Word
Description: Sets the under-temperature warning limit.

Bit	Description	Format	Unit
15:0	Sets the undertemperature warning threshold.	Linear	°C

UT_FAULT_LIMIT (0x53)
Transfer Type: R/W Word
Description: Sets the under-temperature fault limit.

Bit	Description	Format	Unit
15:0	Sets the undertemperature fault threshold.	Linear	°C

UT_FAULT_RESPONSE (0x54)
Transfer Type: R/W Byte
Description: Sets the under-temperature fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable until clear	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times.

Bit	Function	Description	Value	Function	Description
			011	Retry 3 times	The PMBus device attempts to restart 3 times.
			100	Retry 4 times	The PMBus device attempts to restart 4 times.
			101	Retry 5 times	The PMBus device attempts to restart 5 times.
			110	Retry 6 times	The PMBus device attempts to restart 6 times.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Number of delay time units. Used for either the amount of time the device (80 ms/unit) is to continue operating after a fault is detected or for the amount of time (32 ms/unit) between attempts to restart.	0	0	
			1	1	
			2	2	
			3	3	
			4	4	
			5	5	
			6	6	
			7	7	

VIN_OV_FAULT_LIMIT (0x55)
Transfer Type: R/W Word
Description: Sets the input over-voltage fault limit.

Bit	Description	Format	Unit
15:0	Sets the VIN overvoltage fault threshold.	Linear	V

VIN_OV_FAULT_RESPONSE (0x56)
Transfer Type: R/W Byte
Description: Sets the input over-voltage fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).

Bit	Function	Description	Value	Function	Description
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable until clear	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times.
			011	Retry 3 times	The PMBus device attempts to restart 3 times.
			100	Retry 4 times	The PMBus device attempts to restart 4 times.
			101	Retry 5 times	The PMBus device attempts to restart 5 times.
			110	Retry 6 times	The PMBus device attempts to restart 6 times.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Number of delay time units. Used for either the amount of time the device (10 ms/unit) is to continue operating after a fault is detected or for the amount of time (8.2 ms/unit) between attempts to restart.	0	0	
			1	1	
			2	2	
			3	3	
			4	4	
			5	5	
			6	6	
			7	7	

VIN_OV_WARN_LIMIT (0x57)
Transfer Type: R/W Word
Description: Sets the input over-voltage warning limit.

Bit	Description	Format	Unit
15:0	Sets the VIN overvoltage warning threshold.	Linear	V

VIN_UV_WARN_LIMIT (0x58)
Transfer Type: R/W Word
Description: Sets the input under-voltage warning limit.

Bit	Description	Format	Unit
15:0	Sets the VIN undervoltage warning threshold.	Linear	V

VIN_UV_FAULT_LIMIT (0x59)
Transfer Type: R/W Word
Description: Sets the input under-voltage fault limit.

Bit	Description	Format	Unit
15:0	Sets the VIN undervoltage fault threshold.	Linear	V

VIN_UV_FAULT_RESPONSE (0x5A)
Transfer Type: R/W Byte
Description: Sets the input under-voltage fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable until clear	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.

Bit	Function	Description	Value	Function	Description
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times.
			011	Retry 3 times	The PMBus device attempts to restart 3 times.
			100	Retry 4 times	The PMBus device attempts to restart 4 times.
			101	Retry 5 times	The PMBus device attempts to restart 5 times.
			110	Retry 6 times	The PMBus device attempts to restart 6 times.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Number of delay time units. Used for either the amount of time the device (10 ms/unit) is to continue operating after a fault is detected or for the amount of time (8.2 ms/unit) between attempts to restart.	0	0	
			1	1	
			2	2	
			3	3	
			4	4	
			5	5	
			6	6	
			7	7	

POWER_GOOD_ON (0x5E)
Transfer Type: R/W Word
Description: Sets the output voltage threshold for asserting PG (Power Good).

Bit	Description	Format	Unit
15:0	Sets the output voltage threshold for asserting PG (Power Good). Factory default value is controlled by VSET pin-strap.	Vout Mode Unsigned	V

TON_DELAY (0x60)
Transfer Type: R/W Word
Description: Sets the turn-on delay time

Bit	Description	Format	Unit
15:0	Sets the delay time from ENABLE to start of VOUT rise. The time can range from 5 ms up to 500 s, in steps of 125 ns.	Linear	ms

TON_RISE (0x61)
Transfer Type: R/W Word
Description: Sets the turn-on transition time.

Bit	Description	Format	Unit
15:0	Sets the rise time of VOUT after ENABLE and On Delay. The time can range from 0 ms to 200 ms, in steps of 12.5 µs.	Linear	ms

TOFF_DELAY (0x64)
Transfer Type: R/W Word
Description: Sets the turn-off delay.

Bit	Description	Format	Unit
15:0	Sets the delay time from DISABLE to start of VOUT fall. The time can range from 0 ms up to 500 s, in steps of 125 ns.	Linear	ms

TOFF_FALL (0x65)
Transfer Type: R/W Word
Description: Sets the turn-off transition time.

Bit	Description	Format	Unit
15:0	Sets the fall time for VOUT after DISABLE and Off Delay. The time can range from 0 ms to 200 ms, in steps of 12.5 µs.	Linear	ms

STATUS_BYTE (0x78)
Transfer Type: Read Byte
Description: Returns a brief fault/warning status byte.

Bit	Function	Description	Value	Description
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No fault
			1	Fault
6	Off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	0	No fault
			1	Fault
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No fault
			1	Fault
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No fault
			1	Fault
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No fault
			1	Fault
2	Temperature	A temperature fault or warning has occurred.	0	No fault
			1	Fault

Bit	Function	Description	Value	Description
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault
			1	Fault
0	None of the Above	A fault or warning not listed in bits [7:1] has occured.	0	No fault
			1	Fault

STATUS_WORD (0x79)
Transfer Type: Read Word
Description: Returns an extended fault/warning status byte.

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has occurred.	0	No fault
			1	Fault
14	Iout/Pout	An output current or output power fault or warning has occurred.	0	No Fault.
			1	Fault.
13	Input	An input voltage, input current, or input power fault or warning has occurred.	0	No Fault.
			1	Fault.
12	Mfr	A manufacturer specific fault or warning has occurred.	0	No Fault.
			1	Fault.
11	Power-Good	The Power-Good signal, if present, is negated.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No Fault.
			1	Fault.
6	Off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	0	No Fault.
			1	Fault.
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No Fault.
			1	Fault.
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No Fault.
			1	Fault.
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No Fault.
			1	Fault.
2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault.
			1	Fault.
0	None of the Above	A fault or warning not listed in bits [7:1] has occured.	0	No fault.
			1	Fault.

STATUS_VOUT (0x7A)
Transfer Type: Read Byte
Description: Returns Vout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vout Overvoltage Fault	Vout Overvoltage Fault.	0	No Fault.
			1	Fault.
4	Vout Undervoltage Fault	Vout Undervoltage Fault.	0	No Fault.
			1	Fault.

Bit	Function	Description	Value	Description
3	Vout Max Warning	Vout Max Warning (An attempt has been made to set the output voltage to value higher than allowed by the Vout Max command (Section 13.5).	0	No Warning.
			1	Warning.
2	Ton Max Fault	Ton-Max Fault.	0	No Fault
			1	Fault.
1	Toff Max Warning	Toff Max Warning.	0	No Warning.
			1	Warning.

STATUS_IOUT (0x7B)
Transfer Type: Read Byte
Description: Returns Iout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Iout Overcurrent Fault	Iout Overcurrent Fault.	0	No Fault.
			1	Fault.
4	Iout Undercurrent Fault	Iout Undercurrent Fault.	0	No Fault.
			1	Fault.

STATUS_INPUT (0x7C)
Transfer Type: Read Byte
Description: Returns VIN/IIN-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vin Overvoltage Fault	Vin Overvoltage Fault.	0	No Fault.
			1	Fault.
6	Vin Overvoltage Warning	VIN Overvoltage Warning.	0	No Warning.
			1	Warning.
5	Vin Undervoltage Warning	Vin Undervoltage Warning.	0	No Warning.
			1	Warning.
4	Vin Undervoltage Fault	Vin Undervoltage Fault.	0	No Fault.
			1	Fault.

STATUS_TEMPERATURE (0x7D)
Transfer Type: Read Byte
Description: Returns the temperature-related fault/warning status bits

Bit	Function	Description	Value	Description
7	Overtemperature Fault	Overtemperature Fault.	0	No Fault.
			1	Fault.
6	Overtemperature Warning	Overtemperature Warning.	0	No Warning.
			1	Warning.
5	Undertemperature Warning	Undertemperature Warning.	0	No Warning.
			1	Warning.
4	Undertemperature Fault	Undertemperature Fault.	0	No Fault.
			1	Fault.

STATUS_CML (0x7E)
Transfer Type: Read Byte
Description: Returns Communication/Logic/Memory-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Invalid Or Unsupported Command Received	Invalid Or Unsupported Command Received.	0	No Invalid Command Received.
			1	Invalid Command Received.
6	Invalid Or Unsupported Data Received	Invalid Or Unsupported Data Received.	0	No Invalid Data Received.
			1	Invalid Data Received.
5	Packet Error Check Failed	Packet Error Check Failed.	0	No Failure.
			1	Failure.
4	Memory Fault Detected	Memory Fault Detected.	0	No Fault.
			1	Fault.
3	Processor Fault Detected	Processor Fault Detected.	0	No Fault.
			1	Fault.
1	Other Communication Fault	A communication fault other than the ones listed in this table has occurred.	0	No Fault.
			1	Fault.
0	Memory Or Logic Fault	Other Memory Or Logic Fault has occurred.	0	No Fault.
			1	Fault.

STATUS_MFR_SPECIFIC (0x80)
Transfer Type: Read Byte
Description: Returns manufacturer specific status information.

Bit	Description	Value	Description
3	External Switching Period Fault (TSW); indicates loss of external SYNC clock.	0	No Fault.
		1	Fault.

READ_VIN (0x88)
Transfer Type: Read Word
Description: Returns the measured input voltage.

Bit	Description	Format	Unit
15:0	Returns the input voltage reading.	Linear	V

READ_VOUT (0x8B)
Transfer Type: Read Word
Description: Returns the measured output voltage.

Bit	Description	Format	Unit
15:0	Returns the measured output voltage.	Vout Mode Unsigned	V

READ_IOUT (0x8C)
Transfer Type: Read Word
Description: Returns the measured output current.

Bit	Description	Format	Unit
15:0	Returns the output current reading. The device will NACK this command when not enabled and not in the USER_CONFIG monitor mode.	Linear	A

READ_TEMPERATURE_1 (0x8D)
Transfer Type: Read Word
Description: Returns the measured temperature (internal).

Bit	Description	Format	Unit
15:0	Returns the measured temperature (internal).	Linear	°C

READ_DUTY_CYCLE (0x94)
Transfer Type: Read Word
Description: Returns the measured duty cycle in percent.

Bit	Description	Format	Unit
15:0	Returns the target duty cycle during the ENABLE state. The device will NACK this command when not enabled and not in the USER_CONFIG monitor mode.	Linear	%

READ_FREQUENCY (0x95)
Transfer Type: Read Word
Description: Returns the measured SYNC frequency.

Bit	Description	Format	Unit
15:0	Returns the measured operating switch frequency. The device will NACK this command when not enabled and not in the USER_CONFIG monitor mode.	Linear	kHz

PMBUS_REVISION (0x98)
Transfer Type: Read Byte
Description: Returns the PMBus revision number for this device.

Bit	Function	Description	Value	Function	Description
7:4	Part I Revision	Part I Revision.	0x0	1.0	Part I Revision 1.0.
			0x1	1.1	Part I Revision 1.1.
			0x2	1.2	Part I Revision 1.2.
3:0	Part II Revision	Part II Revision.	0x0	1.0	Part II Revision 1.0.
			0x1	1.1	Part II Revision 1.1.
			0x2	1.2	Part II Revision 1.2.

MFR_ID (0x99)
Transfer Type: R/W Block (22 bytes)
Description: Sets the MFR ID String.

Bit	Description	Format
21:0	Maximum of 22 characters.	ASCII

MFR_MODEL (0x9A)
Transfer Type: R/W Block (14 bytes)
Description: Sets the MFR MODEL string.

Bit	Description	Format
13:0	Maximum of 14 characters.	ASCII

MFR_REVISION (0x9B)
Transfer Type: R/W Block (24 bytes)
Description: Sets the MFR revision string.

Bit	Description	Format
23:0	Maximum of 24 characters.	ASCII

MFR_LOCATION (0x9C)
Transfer Type: R/W Block (7 bytes)
Description: Sets the MFR location string.

Bit	Description	Format
6:0	Maximum of 7 characters.	ASCII

MFR_DATE (0x9D)
Transfer Type: R/W Block (10 bytes)
Description: Sets the MFR date at YYMMDD.

Bit	Description	Format
9:0	Maximum of 10 characters.	ASCII

MFR_SERIAL (0x9E)
Transfer Type: R/W Block (13 bytes)
Description: Sets the MFR serial string.

Bit	Description	Format
12:0	Maximum of 13 characters.	ASCII

USER_DATA_00 (0xB0)
Transfer Type: R/W Block (23 bytes)
Description: Sets a user defined data string.

Bit	Description	Format
22:0	Maximum of 23 characters.	ASCII

AUTO_COMP_CONFIG (0xBC)
Transfer Type: R/W Byte
Description: Configures the Dynamic Loop Compensation (DLC) function

Bit	Function	Description	Value	Function	Description
7:4	Scaling of DLC results	Scale the gain of the DLC results by a factor of (G+1)*10%, where G is a integer value 0,1..9. G = 0 yieldes lowest jitter; G = 9 yields tightest transient response.	0	10%	
			1	20%	
			2	30%	
			3	40%	
			4	50%	
			5	60%	
			6	70%	
			7	80%	
			8	90%	
			9	100%	

Bit	Function	Description	Value	Function	Description
3	Power Good Assertion	Configuration of power good assertion after ramp-up.	0	Use configured PG delay	Use the power good delay time specified in POWER_GOOD_DELAY.
			1	Assert PG after completed DLC	Assert the Power Good signal after the DLC algorithm has completed.
2	DLC Result Store	Controls how DLC results are stored in RAM after completed algorithm.	0	Do not store DLC results in RAM	DLC results are not stored in RAM after completed algorithm, which means the DLC algorithm will be performed after each new ramp-up.
			1	Store DLC results in RAM for use on future ramps	DLC results are stored in RAM after completed algorithm, which means the DLC algorithm will only be performed after first ramp-up after input voltage is applied.
1:0	DLC Mode	Controls if and how the DLC algorithm is performed.	00	DLC algorithm disabled	Compensation parameters stored in command PID_TAPS will be used.
			01	Algorithm performed once after ramp	DLC algorithm is performed once after ramp-up of output voltage.
			10	Repeat algorithm every ~1 second	DLC algorithm is performed repeatedly, with ~1 second intervals. This mode can not be used for current sharing groups.
			11	Repeat algorithm every ~1 minute	DLC algorithm is performed repeatedly, with ~1 minute intervals. This mode can not be used for current sharing groups.

AUTO_COMP_CONTROL (0xBD)
Transfer Type: Send Byte
Description: Causes the DLC function to initiate, if DLC is enabled in AUTO_COMP_CONFIG.

DEADTIME_MAX (0xBF)
Transfer Type: R/W Word
Description: Sets the maximum deadtime value for the adaptive deadtime mode range.

Bit	Function	Description	Format	Unit
15:8	Deadtime max	Value -10 to 60 ns. Maximum allowed high-side to low-side deadtime (ns).	Integer Signed	ns
7:0	Deadtime max	Value -10 to 60 ns. Maximum allowed low-side to high-side deadtime (ns).	Integer Signed	ns

MFR_CONFIG (0xD0)
Transfer Type: R/W Word
Description: Sets misc. device configurations.

Bit	Function	Description	Value	Function	Description
15:11	ISense Blanking Delay	Sets the delay, D, in 32ns steps.	0	0 ns	
			1	32 ns	
			2	64 ns	
			3	96 ns	
			4	128 ns	
			5	160 ns	
			6	192 ns	
			7	224 ns	
			8	256 ns	
			9	288 ns	
			10	320 ns	
			11	352 ns	
			12	384 ns	
			13	416 ns	
			14	448 ns	
			15	480 ns	
			16	512 ns	
			17	544 ns	
			18	576 ns	
			19	608 ns	
			20	640 ns	
			21	672 ns	
			22	704 ns	
			23	736 ns	
			24	768 ns	
			25	800 ns	
			26	832 ns	
			27	864 ns	
			28	896 ns	
			29	928 ns	
			30	960 ns	
			31	996 ns	
10:8	Current Sense Fault Count	Sets the number of consecutive OC or UC violations required for a fault.	0	1	
			1	3	
			2	5	
			3	7	
			4	9	
			5	11	
			6	13	
			7	15	
5:4	Current Sense Control		00	GND-ref, down-slope	Current sense uses GND-referenced, down-slope sensing.
			01	Vout-ref, down-slope	Current sense uses output voltage referenced, down-slope sensing.

Bit	Function	Description	Value	Function	Description
			10	Vout-ref, up-slope	Current sense uses output voltage-referenced, up-slope sensing.
3	NLR During Ramp	NLR During Ramp	0	Wait For PG	Wait For Power Good
			1	Always On	Always on.
2	Alternate Ramp Control	Alternate Ramp Control.	0	Disabled	Alternate Ramp Disabled
			1	Enabled	Alternate Ramp Enabled
1	PG Pin Output Control	PG Pin Output Control.	0	Open-Drain	PG is open-drain
			1	Push-Pull	PG is push-pull
0	SYNC Pin Output Control	SYNC Pin Output Control.	0	Open-Drain	SYNC is open-drain
			1	Push-Pull	SYNC is push-pull

USER_CONFIG (0xD1)
Transfer Type: R/W Word
Description: Sets misc. device configurations.

Bit	Function	Description	Value	Function	Description
15:14	Minimum Duty Cycle	Sets the minimum duty cycle to value / 256 x Tsw during a ramp when enabled by Bit 13 (Tsw = switching period).	00	1/256 x Tsw	
			01	2/256 x Tsw	
			10	3/256 x Tsw	
			11	4/256 x Tsw	
13	Enable Minimum Duty Cycle	Enable Minimum Duty Cycle	1		Minimum Duty Cycle is Enabled.
			0		Minimum Duty Cycle is Disabled.
12	Alternate Ramp Down	Alternate Ramp Down	0	Use normal TOFF_FALL	Output follows TOFF_FALL ramp time.
			1	High Impedance Mode	Output is set to high impedance/open mode during ramp down until VOUT_UV threshold is reached.
11	SYNC Time-out Enable	SYNC Time-out Enable	0	SYNC Always On	SYNC output remains on after device is disabled.
			1	SYNC Off in 500 ms	SYNC turns off 500 ms after device is disabled.
9	PID Feed-Forward Ctrl	0: PID Coefficients are corrected for VIN variation; 1: PID Coefficients are not corrected for VIN variations.	0	Correct for VIN	PID Coefficients are corrected for VIN variation.
			1	No Correction	PID Coefficients are not corrected for VIN variations.
8	Fault Spreading Mode	0: Received faults are ignored; 1: Received faults cause shutdown.	0	Ignore Faults	If sequencing is disabled, this device will ignore faults from other devices. If sequencing is enabled, the devices will sequence down from the failed device outward.
			1	Act on Faults	Faults received from any device selected by the GCB_GROUP command will cause this device to shut down immediately.

Bit	Function	Description	Value	Function	Description
6	SYNC Input Mode	0: Auto-configure using the SYNC pin and FREQUENCY_SWITCH parameter; 1: Switch using the SYNC input.	0	Pinstrap Input	Auto-configure using the SYNC pin and FREQUENCY_SWITCH parameter.
			1	Use External Clock	Switch using the SYNC input.
5	SYNC Output Control	SYNC Utilization Control	0	Input Only	Configure the SYNC pin as an input-only.
			1	Output Int. Signal	Drive the switch clock out of SYNC when using the internal oscillator.
2	Lowside FET Mode	0: The low-side drive is off when device is disabled; 1: The low-side drive is on when device is disabled.	0	Off when disabled	The low side drive is off when device is disabled.
			1	On when disabled	The low side drive is on when device is disabled.
1:0	Standby Mode	00: Enter low-power mode when device is disabled (no READ_xxxx data available); 01: Monitor for faults when device is disabled (READ_xxxx data available); 10: Reserved; 11: Monitor for faults using pulsed mode. (READ_xxxx data available upon read command).	00	Low Power	Enter low power mode when device is disabled. When disabled, READ_* commands are unavailable and will trigger a STATUS_CML fault if they are read.
			01	Monitor Always	Monitor for faults when device is disabled.
			11	Pulsed Monitor	Monitor for faults using pulsed mode.

ISHARE_CONFIG (0xD2)
Transfer Type: R/W Word
Description: Configures the device for current sharing communication over the GCB bus.

Bit	Function	Description	Format
15:8	IShare GCB ID	Value 0-31. Sets the current share rail's GCB ID for each device within a current share rail. Must be set to the same GCB ID as in GCB_CONFIG. This GCB ID is used for sequencing and fault spreading when used in a current share rail.	Integer Unsigned

Bit	Function	Description	Value	Function	Description
7:5	Number of Members	Number of devices in current share rail.	0	1 device	
			1	2 devices	
			2	3 devices	
			3	4 devices	
			4	5 devices	
			5	6 devices	
			6	7 devices	
			7	8 devices	
4:2	Member Position	Position of device within current share rail.	0	Position 1	
			1	Position 2	
			2	Position 3	
			3	Position 4	
			4	Position 5	

Bit	Function	Description	Value	Function	Description
			5	Position 6	
			6	Position 7	
			7	Position 8	
0	IShare Control	I-share control.	0	Current Sharing Disabled	Device is not a member of a current share rail.
			1	Current Sharing Enabled	Device is a member of a current share rail.

GCB_CONFIG (0xD3)
Transfer Type: R/W Word
Description: Configures the GCB bus

Bit	Function	Description	Format
12:8	Broadcast Group	Value 0-31. Group number used for broadcast events. (i.e. Broadcast Enable and Broadcast Margin). Set this number to the same value for all rails/devices that should respond to each other's broadcasted event. This function is enabled by the bits 15 and 14 in the MISC_CONFIG command.	Integer Unsigned
4:0	GCB ID	Value 0-31. Sets the rail's GCB ID for sequencing and fault spreading. For the current-sharing applications, set this value the same as the ID value in ISHARE_CONFIG for all devices in the current sharing rail.	Integer Unsigned

Bit	Function	Description	Value	Description
5	GCB Tx Inhibit	GCB tx inhibit.	0	GCB transmission enabled.
			1	GCB transmission inhibited.

POWER_GOOD_DELAY (0xD4)
Transfer Type: R/W Word
Description: Sets the delay from POWER_GOOD_ON to asserting PG.

Bit	Description	Format	Unit
15:0	Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The factory value is equal to TON_RISE. The delay time can range from 0 ms up to 500 s, in steps of 125ns. A 1 ms minimum configured value is a recommended to apply proper debounce to this signal.	Linear	ms

PID_TAPS (0xD5)
Transfer Type: R/W Block (9 bytes)
Description: Configures the linear control loop filter coefficients.

Bit	Function	Description	Format
8:6	Tap C	Contains Pid coefficient C.	Custom
5:3	Tap B	Contains Pid coefficient B.	Custom
2:0	Tap A	Contains Pid coefficient A.	Custom

INDUCTOR (0xD6)
Transfer Type: R/W Word
Description: Informs the device of circuit's inductor value.

Bit	Description	Format	Unit
15:0	This is used in adaptive algorithm calculations relating to the inductor ripple current.	Linear	µH

NLR_CONFIG (0xD7)
Transfer Type: R/W Block (4 bytes)
Description: Configures the non-linear response (NLR) control parameters.

Bit	Function	Description	Value	Function	Description
31:30	Outer Threshold Multiplier	Sets the mulitplier of inner threshold for outer threshold settings.	3	Disable Outer Correction	
			0	x 2	
			1	x 3	
			2	x 4	
29:27	NLR threshold: Load-Inner	Sets the inner comparator threshold for a loading event (% of Vout).	0	-0.5 %	
			1	-1.0 %	
			2	-1.5 %	
			3	-2.0 %	
			4	-2.5 %	
			5	-3.0 %	
			6	-3.5 %	
			7	-4.0 %	
26:24	NLR threshold: Unload-Inner	Sets the inner comparator threshold for an unloading event (% of Vout).	0	0.5 %	
			1	1.0 %	
			2	1.5 %	
			3	2.0 %	
			4	2.5 %	
			5	3.0 %	
			6	3.5 %	
			7	4.0 %	
23:20	Max Load-Outer Correction Time	Sets the outer threshold, maximum correction time for a loading event.	0	0 x Tsw/64	
			1	1 x Tsw/64	
			2	2 x Tsw/64	
			3	3 x Tsw/64	
			4	4 x Tsw/64	
			5	5 x Tsw/64	
			6	6 x Tsw/64	
			7	7 x Tsw/64	
			8	8 x Tsw/64	
			9	9 x Tsw/64	
			10	10 x Tsw/64	
			11	11 x Tsw/64	
			12	12 x Tsw/64	
			13	13 x Tsw/64	
			14	14 x Tsw/64	
			15	15 x Tsw/64	

Bit	Function	Description	Value	Function	Description
19:16	Max Load-Inner Correction Time	Sets the inner threshold, maximum correction time for a loading event.	0	0 x Tsw/64	
			1	1 x Tsw/64	
			2	2 x Tsw/64	
			3	3 x Tsw/64	
			4	4 x Tsw/64	
			5	5 x Tsw/64	
			6	6 x Tsw/64	
			7	7 x Tsw/64	
			8	8 x Tsw/64	
			9	9 x Tsw/64	
			10	10 x Tsw/64	
			11	11 x Tsw/64	
			12	12 x Tsw/64	
			13	13 x Tsw/64	
			14	14 x Tsw/64	
			15	15 x Tsw/64	
15:12	Max Unload-Outer Correction Time	Sets the outer threshold, maximum correction time for an unloading event.	0	0 x Tsw/64	
			1	1 x Tsw/64	
			2	2 x Tsw/64	
			3	3 x Tsw/64	
			4	4 x Tsw/64	
			5	5 x Tsw/64	
			6	6 x Tsw/64	
			7	7 x Tsw/64	
			8	8 x Tsw/64	
			9	9 x Tsw/64	
			10	10 x Tsw/64	
			11	11 x Tsw/64	
			12	12 x Tsw/64	
			13	13 x Tsw/64	
			14	14 x Tsw/64	
			15	15 x Tsw/64	
11:8	Max Unload-Inner Correction Time	Sets the inner threshold, maximum correction time for an unloading event.	0	0 x Tsw/64	
			1	1 x Tsw/64	
			2	2 x Tsw/64	
			3	3 x Tsw/64	
			4	4 x Tsw/64	
			5	5 x Tsw/64	
			6	6 x Tsw/64	
			7	7 x Tsw/64	
			8	8 x Tsw/64	
			9	9 x Tsw/64	
			10	10 x Tsw/64	
			11	11 x Tsw/64	
			12	12 x Tsw/64	
			13	13 x Tsw/64	
			14	14 x Tsw/64	
			15	15 x Tsw/64	

Bit	Function	Description	Value	Function	Description
7:4	Load Blanking Time Control	Sets the NLR blanking time for a loading event.	0	0 x Tsw/64	
			1	1 x Tsw/64	
			2	2 x Tsw/64	
			3	4 x Tsw/64	
			4	8 x Tsw/64	
			5	16 x Tsw/64	
			6	32 x Tsw/64	
			7	48 x Tsw/64	
			8	64 x Tsw/64	
			9	80 x Tsw/64	
			10	96 x Tsw/64	
			11	128 x Tsw/64	
			12	160 x Tsw/64	
			13	176 x Tsw/64	
			14	192 x Tsw/64	
			15	224 x Tsw/64	
3:0	Unload Blanking Time Control	Sets the NLR blanking time for an unloading event.	0	0 x Tsw/64	
			1	1 x Tsw/64	
			2	2 x Tsw/64	
			3	4 x Tsw/64	
			4	8 x Tsw/64	
			5	16 x Tsw/64	
			6	32 x Tsw/64	
			7	48 x Tsw/64	
			8	64 x Tsw/64	
			9	80 x Tsw/64	
			10	96 x Tsw/64	
			11	128 x Tsw/64	
			12	160 x Tsw/64	
			13	176 x Tsw/64	
			14	192 x Tsw/64	
			15	224 x Tsw/64	

OVUV_CONFIG (0xD8)
Transfer Type: R/W Byte
Description: Sets output OV/UV control features.

Bit	Function	Description	Format
3:0	No Of Limit Violations	Value 0-15. Value + 1 consecutive OV or UV violations initiate a fault response.	Integer Unsigned

Bit	Function	Description	Value	Description
7	Low-Side OV Fault Control (Crowbar)	0: An OV fault does not enable the low-side power device; 1: An OV fault enables the low-side power device.	0	An OV fault does not enable the low-side power device.
			1	An OV fault enables the low-side power device.

XTEMP_SCALE (0xD9)
Transfer Type: R/W Word
Description: Sets a scalar value that is used for calibrating the external temperature. Not applicable in this product.

Bit	Description	Format
15:0	The constant is applied to the equation READ_TEMPERATURE_2 = ExternalTemperature / XTEMP_SCALE + XTEMP_OFFSET to produce the read value of XTEMP via the PMBus command READ_TEMPERATURE_2.	Linear

XTEMP_OFFSET (0xDA)
Transfer Type: R/W Word
Description: Sets an offset value that is used for calibrating the external temperature. Not applicable in this product.

Bit	Description	Format	Unit
15:0	The constant is applied to the equation READ_TEMPERATURE_2 = ExternalTemperature / XTEMP_SCALE + XTEMP_OFFSET to produce the read value of XTEMP via the PMBus command READ_TEMPERATURE_2.	Linear	°C

VOUT_MAX_LIMIT (0xDB)
Transfer Type: Read Word
Description: Read the pin-strapped max value of Vout.

Bit	Description	Format	Unit
15:0	Read the pin-strapped maximum possible value setting of VOUT.	Vout Mode Unsigned	V

TEMPCO_CONFIG (0xDC)
Transfer Type: R/W Byte
Description: Configures the correction factor when performing temperature coefficient correction for current sense. This value is set at the factory and should not be changed.

Bit	Description	Format	Unit
7:0	Isense Temperature Correction.	Integer Unsigned	100ppm/°C

DEADTIME (0xDD)
Transfer Type: R/W Word
Description: Sets the non-overlap between PWM transitions. This value is set at the factory and should not be changed.

Bit	Function	Description	Format	Unit
15:8	Deadtime H-L	Value -10 to 60 ns. Controls the high-side to low-side deadtime value. Positive values imply a non-overlap of the FET drive on-times. Negative values imply an overlap of the FET drive on-times. The default value of the maximum deadtime for the adaptive deadtime algorithm is 60ns. Writing a value to this command immediately before writing the DEADTIME_CONFIG command will set a new maximum for the adaptive deadtime algorithm. The device will operate at the deadtime values written to this command when adaptive deadtime is disabled.	Integer Signed	ns

Bit	Function	Description	Format	Unit
7:0	Deadtime L-H	Value -10 to 60 ns. Controls the low-side to high-side deadtime value. Positive values imply a non-overlap of the FET drive on-times. Negative values imply an overlap of the FET drive on-times. Writing a value to this command immediately before writing the DEADTIME_CONFIG command will set a new maximum for the adaptive deadtime algorithm. The device will operate at the deadtime values written to this command when adaptive deadtime is disabled.	Integer Signed	ns

DEADTIME_CONFIG (0xDE)
Transfer Type: R/W Word
Description: Configures the deadtime optimization mode. Also sets the minimum deadtime value for the adaptive deadtime mode range. This value is set at the factory and should not be changed.

Bit	Function	Description	Format	Unit
14:8	Min Deadtime H-L	Value -5 to 28 ns. Limits the minimum allowed H-to-L deadtime to value x 2 ns (signed).	Integer Signed	x 2ns
6:0	Min. L-H Deadtime	Value -5 to 28 ns. Limits the minimum allowed L-to-H deadtime to value x 2ns (signed).	Integer Signed	x 2ns

Bit	Function	Description	Value	Function	Description
15	H-L Deadtime Mode	0: Adaptive H-to-L deadtime control; 1: Freezes the H-to-L deadtime.	0	Adaptive	Adaptive H-to-L deadtime control.
			1	Freeze	Freeze the H-to-L deadtime.
7	L-H Deadtime Mode	0: Adaptive L-to-H deadtime control; 1: Freezes the L-to-H deadtime.	0	Adaptive	Adaptive L-to-H deadtime control.
			1	Freeze	Freeze the L-to-H deadtime.

SEQUENCE (0xE0)
Transfer Type: R/W Word
Description: The SEQEUNCE command identifies the Rail GCB ID of the prequel and sequel rails when performing multi-rail sequencing.

Bit	Function	Description	Format
12:8	Prequel Rail GCB ID	Value 0-31. Set to the Rail GCB ID of the rail that should precede this device's rail in a sequence order.	Integer Unsigned
4:0	Sequel Rail GCB ID	Value 0-31. Set to the Rail GCB ID of the rail that should follow this device's rail in a sequence order.	Integer Unsigned

Bit	Function	Description	Value	Description
15	Prequel Enable	Prequel Enable/Disable.	0	Disable, no prequel preceding this rail.
			1	Enable, prequel to this rail is defined by bits 12:8.
7	Sequel Enable	Sequel Enable/Disable.	0	Disable, no sequel following this rail.
			1	Enable, sequel to this rail is defined by bits 4:0.

TRACK_CONFIG (0xE1)
Transfer Type: R/W Byte
Description: Configures the voltage tracking modes of the device

Bit	Function	Description	Value	Function	Description
7	Enable Voltage Tracking	Enables voltage tracking.	0		Tracking is disabled.
			1		Tracking is enabled.
2	Upper Tracking Ratio	Controls upper tracking ratio.	0	Output Tracks 100% Of VTRK	Output tracks 100% of VTRK.
			1	Output Tracks 50% Of VTRK	Output tracks 50% of VTRK.
1	Upper Track Limit	Controls upper track limit.	0	Limited By Target Voltage	Output is limited by target voltage.
			1	Limited By VTRK	Output is limited by VTRK pin.
0	Ramp-up Behavior	Controls ramp-up behavior.	0		The output is not allowed to track VTRK down before Power Good.
			1		The output is allowed to track VTRK down before power-good.

GCB_GROUP (0xE2)
Transfer Type: R/W Block (4 bytes)
Description: This command sets which rail GCB IDs should be.listened to for fault spreading information. The data sent is a 4-byte, 32-bit, bit vector where every bit represents a rail's GCB ID. A bit set to 1 indicates a device GCB ID to which the configured device will respond upon receiving a fault spreading event. In this vector, bit 0 of byte 0 corresponds to the rail with GCB ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with GCB ID 31

Bit	Description	Format
31:0	Sets the rail's GCB ID for sequencing and fault spreading. For the current-sharing applications, set this value the same as the ID value in ISHARE_CONFIG for all devices in the current sharing rail	Byte Array

DEVICE_ID (0xE4)
Transfer Type: Read Block (16 bytes)
Description: Returns the 16-byte (character) device identifier string.

Bit	Description	Format
15:0	Returns the 16-byte (character) device identifier string.	ASCII

MFR_IOUT_OC_FAULT_RESPONSE (0xE5)
Transfer Type: R/W Byte
Description: Configures the output overcurrent fault response. The command format is the same as the PMBus standard responses for voltage and temperature faults except that it sets the overcurrent status bit.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable until clear	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times.
			011	Retry 3 times	The PMBus device attempts to restart 3 times.
			100	Retry 4 times	The PMBus device attempts to restart 4 times.
			101	Retry 5 times	The PMBus device attempts to restart 5 times.
			110	Retry 6 times	The PMBus device attempts to restart 6 times.

Bit	Function	Description	Value	Function	Description
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Number of delay time units. Used for either the amount of time the device (10 ms/unit) is to continue operating after a fault is detected or for the amount of time (8.2 ms/unit) between attempts to restart.	0	0	
			1	1	
			2	2	
			3	3	
			4	4	
			5	5	
			6	6	
			7	7	

MFR_IOUT_UC_FAULT_RESPONSE (0xE6)
Transfer Type: R/W Byte
Description: Configures the output undercurrent fault response. The command format is the same as the PMBus standard responses for voltage and temperature faults except that it sets the undercurrent status bit.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	The PMBus device continues operation without interruption.
			01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable until clear	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.

Bit	Function	Description	Value	Function	Description
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared. The time between the start of each attempt to restart is set by the value in bits [2:0] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times.
			011	Retry 3 times	The PMBus device attempts to restart 3 times.
			100	Retry 4 times	The PMBus device attempts to restart 4 times.
			101	Retry 5 times	The PMBus device attempts to restart 5 times.
			110	Retry 6 times	The PMBus device attempts to restart 6 times.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Number of delay time units. Used for either the amount of time the device (10 ms/unit) is to continue operating after a fault is detected or for the amount of time (8.2 ms/unit) between attempts to restart.	0	0	
			1	1	
			2	2	
			3	3	
			4	4	
			5	5	
			6	6	
			7	7	

IOUT_AVG_OC_FAULT_LIMIT (0xE7)
Transfer Type: R/W Word
Description: This command sets the average output current overcurrent fault threshold. Shares the fault bit operation and OC fault response with IOUT_OC_FAULT_LIMIT.

Bit	Description	Format	Unit
15:0	Sets the average Iout over-current fault limit.	Linear	A

IOUT_AVG_UC_FAULT_LIMIT (0xE8)
Transfer Type: R/W Word
Description: This command sets the average output sink current (under-current) fault threshold. Shares the fault bit operation and UC fault response with IOUT_UC_FAULT_LIMIT.

Bit	Description	Format	Unit

Bit	Description	Format	Unit
15:0	Sets the average Iout under-current fault limit.	Linear	A

MISC_CONFIG (0xE9)
Transfer Type: R/W Word
Description: This command sets a few options pertaining to ramp timing accuracy and current-driven control.

Bit	Function	Description	Value	Function	Description
15	Enable Broadcast Margin	Broadcast margin (see GCB_CONFIG).	00		Disabled
			01		Enabled
14	Enable Broadcast	Broadcast Enable (see GCB_CONFIG).	00		Disabled
			01		Enabled
13	Phase Enable Select	Phase Enable Select.	00	Use CTRL pin	Use CTRL pin to add/drop current-share phases.
			01	Use PHASE_CONTROL command	Use PHASE_CONTROL command to add/drop phases.
6	Diode Emulation	Diode Emulation	00	Disabled	Disabled.
			01	Enabled	Enabled, enter diode emulation at low current loads to improve efficiency.
2	Minimum GL Pulse	Minimum GL pulse (Pulse Skip Control)	00	Disabled	Disabled.
			01	Enabled	Enabled, limited to 10% × 1/Fswitch minimum during diode emulation.
1	Snapshot	Snapshot	00	Disabled	Disabled.
			01	Enabled	Enabled.

SNAPSHOT (0xEA)
Transfer Type: Read Block (32 bytes)
Description: The SNAPSHOT command is a 32-byte read-back of parametric and status values.

Bit	Function	Description	Format
21	Manufacturer Specific Status Byte	Manufacturer specific status byte.	Integer Unsigned
20	Status CML	Status CML.	Integer Unsigned
19	Status Temperature	Status temperature.	Integer Unsigned
18	Status Vin	Status Vin.	Integer Unsigned
17	Status Iout	Status iout.	Integer Unsigned
16	Status Vout	Status vout.	Integer Unsigned
15:14	Switching Frequency	Switching frequency.	Linear
11:10	Internal Temperature	Internal temperature.	Linear
9:8	Duty Cycle	Duty cycle.	Linear
7:6	Peak Current	Peal current.	Linear

Bit	Function	Description	Format
5:4	Load Current	Load current.	Linear
3:2	Output Voltage	Output voltage.	Vout Mode Unsigned
1:0	Input Voltage	Input voltage.	Linear

BLANK_PARAMS (0xEB)
Transfer Type: Read Block (16 bytes)
Description: Returns a 16-byte string which indicates which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A one indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Bit	Description	Format
15:0		Byte Array

PHASE_CONTROL (0xF0)
Transfer Type: R/W Byte
Description: This command controls the adding and shedding of phases when the device is set up for current sharing.

Bit	Description	Value	Function	Description
0	This command controls the adding and shedding of phases when the device is set up for current sharing.	0	Disabled	Disables the devices and stops power transfer to the load.
		1	Active	Causes the device to be active (supplying power to the load).

SNAPSHOT_CONTROL (0xF3)
Transfer Type: R/W Byte
Description: Used to save a set of current information about the operation of the regulator.

Bit	Description	Value	Function	Description
0	Used to save a set of current information about the operation of the regulator.	0x01	Copy Flash to RAM	Causes the current SNAPSHOT values to be copied to the data registers.
		0x02	Store RAM to Flash	Causes the values to be stored in set location in flash memory.

SECURITY_LEVEL (0xFA)
Transfer Type: Read Byte
Description: Returns the current security level.

Bit	Description	Value	Function	Description
7:0	The device provides write protection for individual commands.	0x03	Level 3	Security Level 3 – Module Vendor.
		0x02	Level 2	Security Level 2 – User.
		0x01	Level 1	Security Level 1 – Public.
		0x00	Level 0	Security Level 0 - Unprotected.

PRIVATE_PASSWORD (0xFB)
Transfer Type: R/W Block (9 bytes)
Description: Sets the private password string for the USER_STORE. Password strings have the same format as the MFR_ID parameters.

Bit	Description	Format
8:0	Sets the private password string for the USER_STORE. Password strings have the same format as the MFR_ID parameters.	ASCII

PUBLIC_PASSWORD (0xFC)
Transfer Type: R/W Block (4 bytes)
Description: Sends a password to the device.

Bit	Description	Format
3:0	Sets the public password string.	ASCII

UNPROTECT (0xFD)
Transfer Type: R/W Block (32 bytes)
Description: Assigned command groups to a security level.

Bit	Description	Format
31:0		Byte Array

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