ISL6553EVAL1 - Two-Phase Power Conversion for Intel® VRM8.5-Compliant Celeron™ Motherboards

Application Note | October 2001 | AN9961.1

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Introduction

Power supply designers are continually faced with next generation microprocessors which draw higher peak currents while demanding faster slew rates. Intersil's Endura™ multiphase product family provides a wide variety of controllers and drivers to address these changing requirements.

Intersil ISL6553 and HIP6601A

The ISL6553 controller coupled with two HIP6601A single channel drivers form a highly integrated solution for high current, high slew rate applications. This controller is recommended specifically for VRM8.5-compliant Pentium® processor core-voltage regulation.

The ISL6553 regulates the output voltage and balances load currents for two synchronous rectified buck converter channels. A five-bit DAC provides a digital interface to program the 1% accurate reference over a range of 1.050V to 1.825V. Overvoltage and overcurrent protection monitors ensure a microprocessor safe environment. For a more detailed description of the ISL6553 functionality, refer to the ISL6553 Data Sheet [1].

The HIP6601A is a dual MOSFET driver specifically designed to drive two N-Channel Power MOSFETs in a synchronous-rectified bridge configuration. A single logic signal input controls both the upper and lower MOSFETs. Shoot-through protection is provided on both switching edges to provide optimal dead time. Internal bootstrap circuitry only requires an external capacitor and provides better enhancement of the upper MOSFET. For a more detailed description of the HIP6601A, refer to the HIP6601A data sheet [2]. The HIP6602A dual-channel driver provides equivalent functionality with some space savings [3].

ISL6553EVAL1 Reference Design

The ISL6553EVAL1 evaluation board is designed to meet the high end requirements of Intel Celeron processors covered by the VRM8.5 specification. The entire circuit fits within the slightly less than 5 in^2 white outline rectangle on the top side of the board. The components outside the box simplify the evaluation process. These include input and output power connectors, VID selection jumpers, critical probe points, power-good indicator and a load transient generator. The evaluation board is implemented on a two-ounce, four-layer, printed circuit board. See pp. 7–9 for layout plots.

With the VID jumpers set to 10110 (1.5V), the evaluation board meets the design specifications indicated in Table 1.

TABLE 1. ISL6553EVAL1 DESIGN PARAMETERS

PARAMETER	MAX	MIN
Static Regulation	1.565V	1.435V
Transient Regulation	1.590V	1.410V
Overvoltage Protection	1.800V	1.650V
Continuous Load Current	30A	-
Load-Current Transient	210A/μs	-
Overcurrent Trip Level	52A	36A

Quick Start Evaluation

Output Voltage Selection

The ISL6553EVAL1 will arrive with the VID jumper combination (JP1) set to 1.5V (10110). This can easily be changed to the desired output voltage by changing the VID jumpers per the DAC table in the ISL6553 data sheet [1]. VID0 and VID4 on the board correspond to VID25mV and VID3 respectively. The output voltage of the ISL6553 can be set from 1.05V to 1.825V in steps of 25mV.

Input Power Connections

The ISL6553EVAL1 provides two options for powering the evaluation board. A 20-pin header, J1, is provided to mate with a standard ATX supply main power connector. If an ATX is not available, bench supplies can be connected to female banana jacks. Connect 12V and 5V supplies to J2 and J3 respectively. Connect the grounds from both supplies to J4. Using bench-top supplies allows easy evaluation of power-on levels and power sequencing issues.

Power Supply Considerations

When using bench-top supplies the sequencing of the supplies is important. Applying the 5V supply prior to the 12V supply is not desirable. This sequencing could result in the ISL6553 starting before the HIP6601A drivers are initialized. The ISL6553 could complete its soft-start interval and produce maximum duty cycle PWM drive signals before the drivers are capable of switching power to the output. This can result in an overcurrent trip due to the lack of soft-start, followed by a new soft-start interval. This abnormal start-up sequence can be avoided by applying the 5V supply after or at the same time as the 12V supply. Power supply sequencing is not an issue when using an ATX power supply.

The power-on reset function of the ISL6553 can be inadvertently activated when operating the transient load generator. Not all bench-top and ATX power supplies are capable of responding to load transients, and they may cause a momentary dip of VCC5. If low enough, this dip can

trigger the power-on-reset function of the ISL6553 and cause the output power to cycle. A simple remedy is to connect a 5600µF or larger capacitor between VCC5 (J3) and ground (J4). The capacitor, if necessary, simulates the distributed capacitance that exists on a computer motherboard.

On-Board Load Transient Generator

Most bench-top electronic loads are not capable of emulating the slew rates specified by Intel's VRM 8.5 specification. For this reason, a discrete load-transient generator is provided on the evaluation board. See the schematic in Figure 1. The load generator produces a load pulse of 100µs in duration with a period of 6ms. The pulse magnitude is approximately 32A with rise and fall slew rates of approximately 210A/µs. The short load current pulse and long duty cycle are required to limit the power dissipation in the load resistors (R14, R15, R16) and MOSFETs (Q6, Q7).

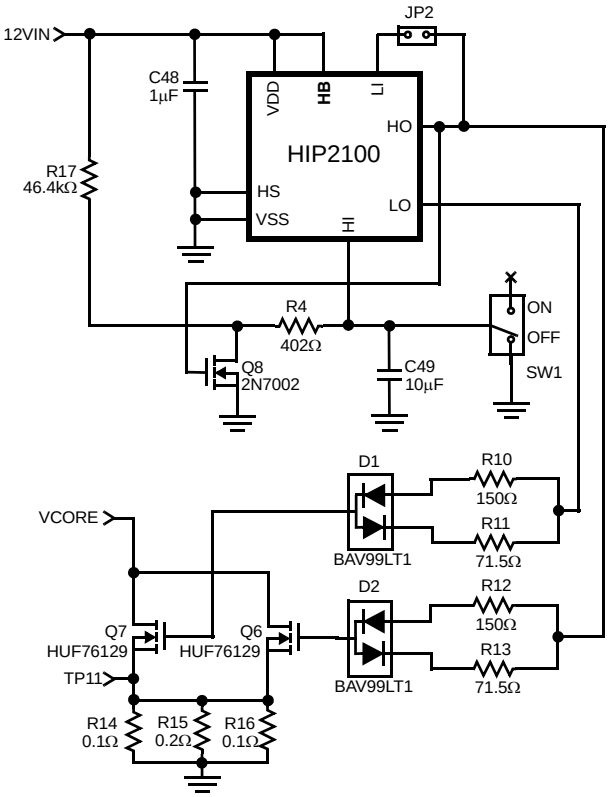

FIGURE 1. LOAD TRANSIENT GENERATOR

If a slightly less severe transient is desired, the magnitude and edge rates can be reduced by removing the HO/LI jumper (JP2). The load generator then produces a 28.5A magnitude transient with edge rates of 175A/µs. The load generator is controlled by the switch labeled SW1.

To engage the load generator simply place the switch marked Transient (SW1) in the ON position. The resulting load pulse and output voltage response is shown in Figure 2. Further analysis of the converter's response to the transient generator load is given in the ISL6553EVAL1 *Performance* section under the *Transient Response* sub-section.

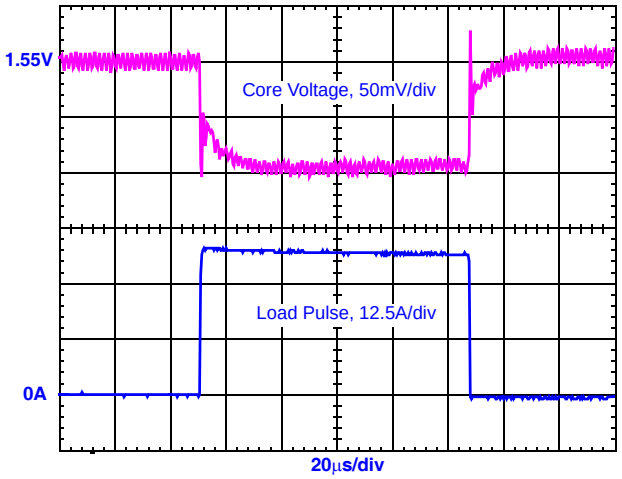

FIGURE 2. TRANSIENT RESPONSE AND LOAD GENERATOR PULSE

ISL6553EVAL1 Performance

Soft-Start Interval

Powered by a standard ATX power supply, the ISL6553 insures a controlled start-up of the converter. ISL6553EVAL1 start-up into a 50mΩ load is shown in Figure 3. The soft-start interval is triggered by the release of the FS/EN pin from ground potential. The converter output voltage, VCORE, slowly ramps up to the full load set point of 1.455V. This controlled ramp of output voltage and supply current reduces the strain on the 5V supply. The internal pull down on the PGOOD pin is then released to provide an indication that the output voltage is within regulation limits.

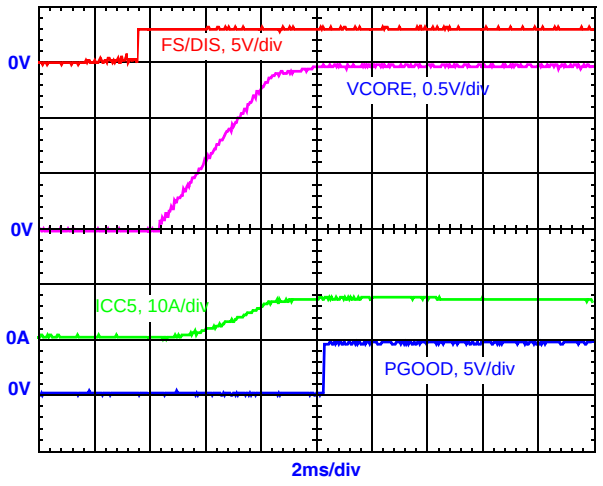

FIGURE 3. SOFT-START INTERVAL WAVEFORMS

Transient Response

The VRM 8.5 specification requires a DC-DC converter to support loading at the processor socket pins over the range of 19–28A with transient slew rates ranging from 159A/µs to 209.5A/µs. The on-board load generator simulates the worse case of these conditions.

The leading edge transient response of the ISL6553EVAL1 to the load generator is captured in Figure 4. The core voltage immediately drops when the transient is applied as the bulk and ceramic output capacitors begin to support the output voltage. The controller quickly detects the voltage deviation and responds by pushing the PWM signals toward their maximum of 75% for the first pulse following the transient. The inductor currents rapidly increase to meet this new demand, supplying an increasing portion of the load. The inductors assume the majority of load current in about 5µs, thereby reducing the bulk capacitance required to support the transient. The output voltage is quickly driven to the droop level set for full load of 1.455V.

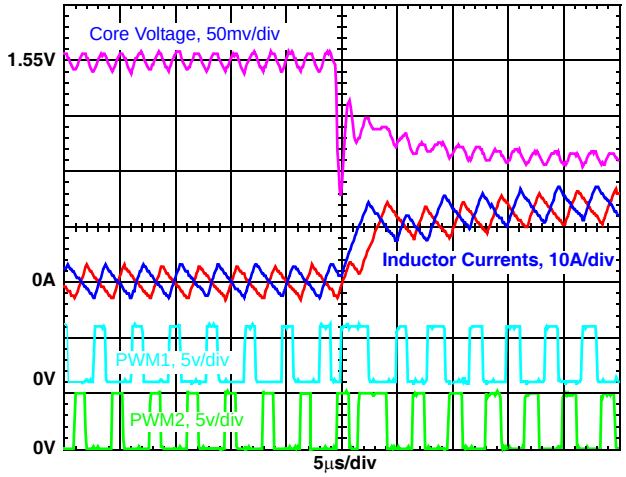

FIGURE 4. LEADING EDGE TRANSIENT RESPONSE

Figure 5 shows the core voltage, inductor current and PWM signals changing in response to the trailing edge of the transient load current. When the load is removed, the output voltage rises quickly in response. The controller detects the load change and immediately decreases the duty cycle to zero for one cycle. During this zero duty cycle period, the output capacitors sustain the output voltage, while the inductors shed load current at the maximum rate. The output voltage is brought back to the no-load offset level of 1.545V in approximately 5µs.

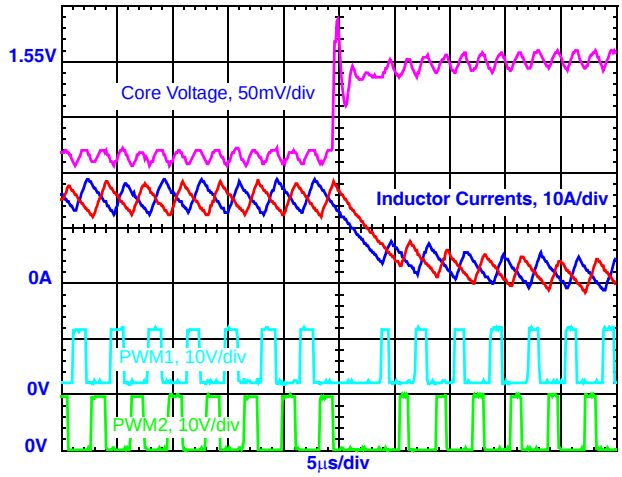

FIGURE 5. TRAILING EDGE TRANSIENT RESPONSE

Output Overcurrent Protection

The ISL6553 monitors the output current level via the ISEN pins. The R_{ISEN} resistors (R1, R2) are selected such that the current out of the ISEN pins is 50µA at maximum load current. When excessive load current forces the average of the ISEN currents to exceed 165% of 50µA or 82.5µA, the converter detects an overcurrent event. The ISL6553 immediately transitions the PWM signals from their current state into a high impedance state, quickly removing gate drive to the HIP6601A drivers. The core voltage begins to decay as the output capacitors discharge. Once the output voltage falls below the undervoltage threshold, the PGOOD signal transitions low. This series of events is captured in Figure 6.

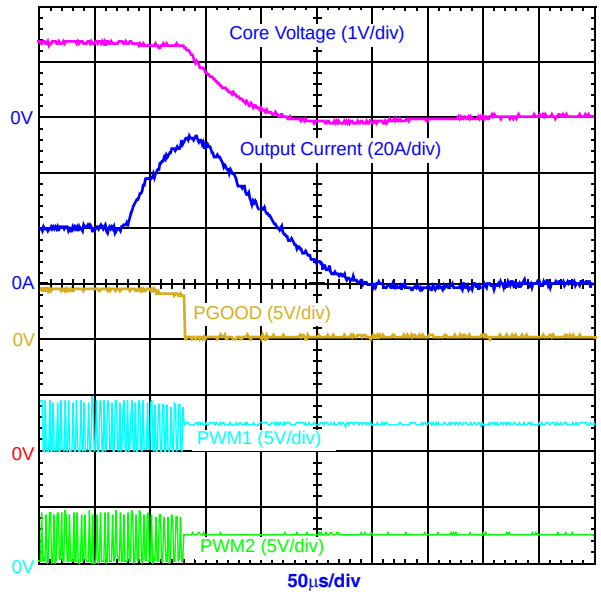

FIGURE 6. OVERCURRENT RESPONSE

After the overcurrent event is detected, the controller waits a short delay time before attempting a soft-start cycle to allow the disturbance to clear. The delay time for the ISL6553EVAL1 board is about 8ms in duration and is set by the switching frequency of the converter ($2048/f_{SW}$). If, during the soft-start cycle, another overcurrent trip is detected, the PWM signals are again tri-stated and PGOOD remains low. The controller waits another 8ms before another soft-start cycle is attempted.

Figure 7 illustrates how the controller recovers from an overcurrent trip caused by a temporary short on the output. After detecting the initial application of the short while regulating the core under a 30A load, the controller halts PWM operation and places the PWM outputs into Tri-State®. See the PWM1 waveform in Figure 7. A soft-start cycle is attempted after an 8ms delay. The output remains shorted during the first soft-start cycle. The ISL6553 detects the short as an overcurrent event during the soft-start cycle and places the PWM outputs into Tri-State. The short is removed during the 8ms delay before initiating a second soft-start cycle. The converter safely resumes regulation of the 30A

load and the PGOOD signal transitions high once the soft-start cycle is complete.

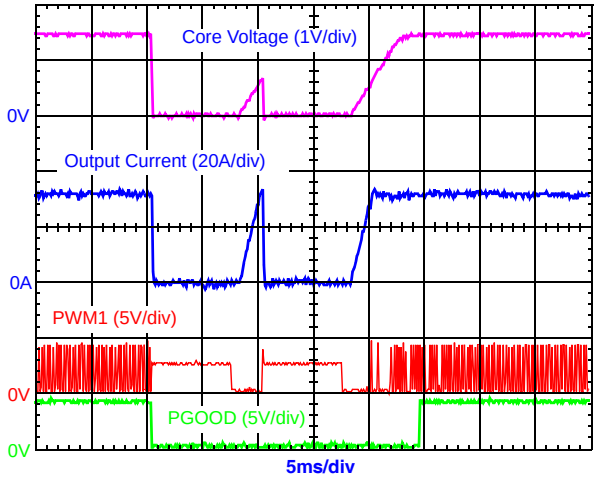

FIGURE 7. RESPONSE TO TEMPORARY OUTPUT SHORT

Under most circumstances an overcurrent event will remain until the fault is found and removed. The ISL6553 will continue to cycle through the same delay time and soft-start cycle sequence until that time. The worst-case power delivered during overcurrent cycling is less than that of normal operation due to the addition of delay time. Indefinite overcurrent cycling does not create any thermal issues.

Efficiency

The performance of the ISL6553EVAL1 board loaded from 5A to 30A is plotted in Figure 8. The measurements were made at thermal equilibrium under room temperature conditions with no air flow.

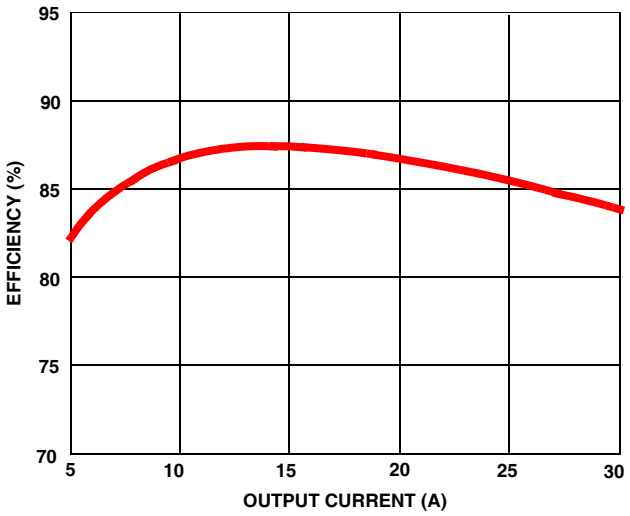

FIGURE 8. EFFICIENCY vs LOAD CURRENT

Adapting Circuit Performance

This evaluation board showcases one solution to meet the present requirements of voltage regulator modules powering Intel Pentium III processors. The balance between meeting specifications and cost can be tilted depending on the performance expectations desired. For example, implementation cost could be reduced if additional motherboard space is available. The OSCON output capacitors could be replaced with less costly aluminum capacitors with higher ESR, but more than four capacitors would be required to meet the same transient specifications. Efficiency could be improved by selecting MOSFETs with a slightly lower $r_{DS(on)}$ and comparable total gate charge.

Summary

The ISL6553EVAL1 is an adaptable evaluation tool which showcases the performance of the ISL6553 / HIP6601A chip set. Designed to meet the performance requirements of Intel's VRM-8.5 specification, the board allows the user the flexibility to configure the board for current as well as future microprocessor offerings.

The following pages provide a schematic of the board, bill of materials and layout drawings to support implementation of this solution.

References

Intersil documents are available on the web at http://www.intersil.com/.

[1] ISL6553 Data Sheet, Intersil Corporation, FN4931

[2] HIP6601A/HIP6603A Data Sheet, Intersil Corporation, FN4819

[3] HIP6602A Data Sheet, Intersil Corporation, FN4902

Schematic

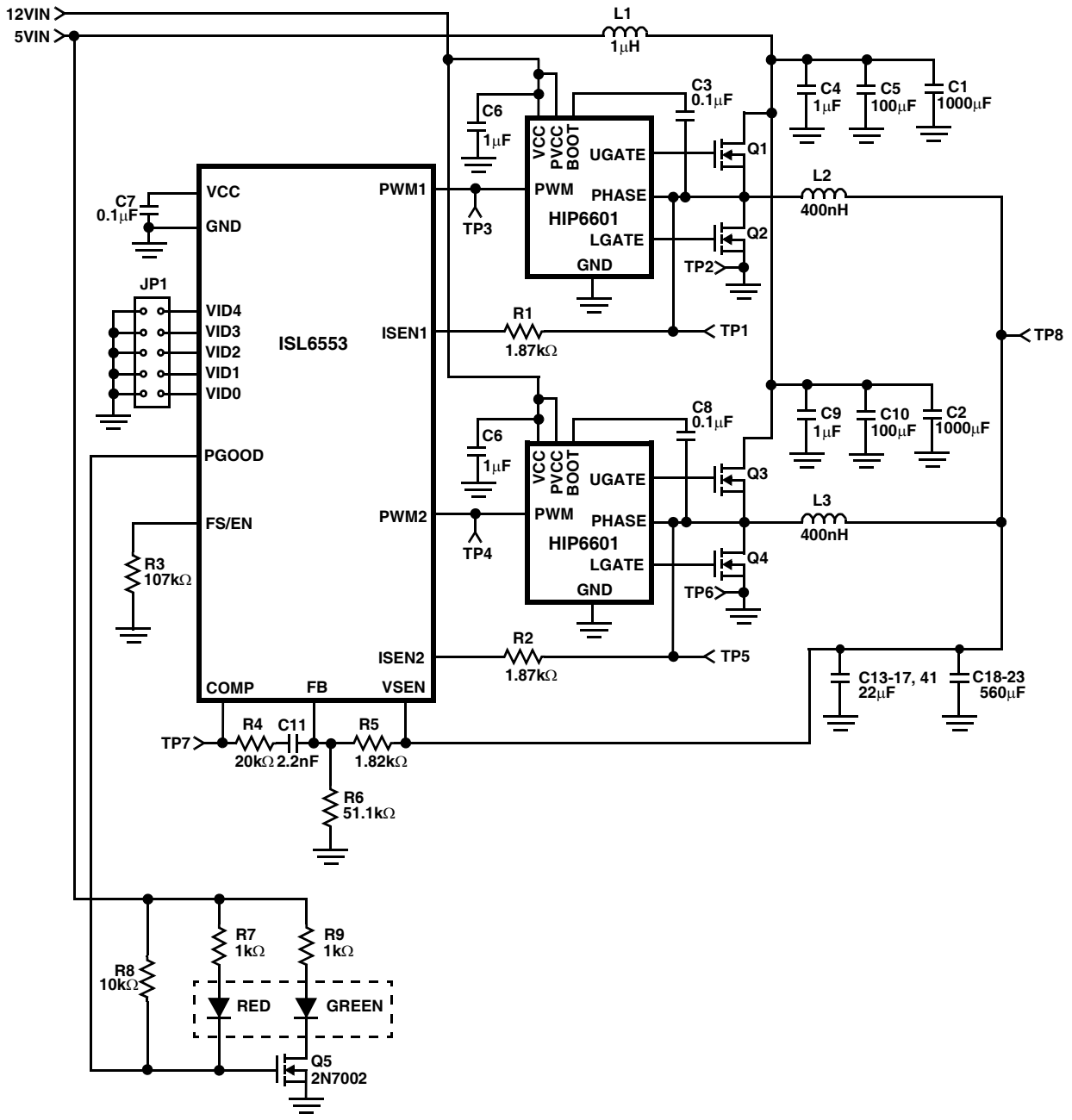

FIGURE 9. APPLICATION CIRCUIT

Bill of Materials

QTY	REFERENCE	DESCRIPTION	PACKAGE	VENDOR	PART NO.
1	CR1	RED/GREEN LED	SMT	Lumex	SLL-LXA3025IGC
2	C1, C2	1000µF, 10V, Aluminum Capacitor	Radial	Panasonic	EEUFC1A102L
3	C3, C7, C8	0.1µF, 25V, Y5V, Ceramic Capacitor	0603	Various	
5	C4, C6, C9, C12, C48	1.0µF, 25V, Y5V, Ceramic Capacitor	0805	Various	
2	C5, C10	100µF, 16V, Organic Capacitor	Radial	Sanyo	16SP100M
1	C11	2.2nF, 25V, X7R, Ceramic Capacitor	0603	Various	
6	C13-17, C41	22µF,10V,Y5V,Ceramic Capacitorr	1206	Various	
4	C19, C20, C22, C23	560µF, 4V, Organic Capacitor	Radial	Sanyo	4SP560M
14	C18, C21, C24-C35	Spare	Radial		
12	C36-C40, C42-C47	Spare	1206		
1	C49	22uF, 6.3V, X5R, Ceramic Capacitor	1206	Various	
2	D1, D2	Dual Diode	SOT-23	Various	BAV99
1	JP1	5-Position Jumper Header	100mil Centers	Berg	68000-236
5		Jumpers		Berg	71363-102
1	JP2	1-Position Header	100mil Centers	Berg	68000-236
1		Jumper		Berg	71363-102
1	J1	ATX Power Header		Berg	39-29-9203
2	J2, J3	Female Banana Connector, Red	Screw On	Johnson Components	111-0702-001
1	J4	Female Banana Connector, Black	Screw On	Johnson Components	111-0703-001
2	J5, J6	Terminal Connector	Solder Mount	Burndy	KPA8CTP
1	L1	1µH	Thru Hole	Falco	TTID1305-838
2	L2, L3	450nH	Thru Hole	Falco	TTIB1506-478
4	Q1, Q2, Q3, Q4	Power MOSFET	TO-263AB	Intersil	HUF76139S3S
2	Q5, Q8	General Purpose MOSFET	SOT-23	Various	2N7002
2	Q6, Q7	Power MOSFET	TO-252AA	Intersil	HUF76129D3S
2	R1, R2	Resistor, 1.87kΩ, 1%, 1/10W	0603	Various	
1	R3	Resistor, 107kΩ, 1%, 1/10W	0603	Various	
1	R4	Resistor, 20.0kΩ, 1%, 1/10W	0603	Various	
1	R5	Resistor,1.82kΩ,1%,1/10W	0603	Various	
1	R6	Resistor,51.1kΩ,1%,1/10W	0603	Various	
2	R7, R9	Resistor, 1.0kΩ, 5%, 1/8W	0603	Various	
1	R8	Resistor, 10kΩ, 5%, 1/10W	0603	Various	
2	R10, R12	Resistor, 150Ω, 1%, 1/8W	0805	Various	
2	R11, R13	Resistor, 71.5Ω, 1%, 1/8W	0805	Various	
2	R14, R16	Resistor, 0.100Ω, 1%, 1W	2512	Vishay	WSL2512R100FB43
1	R15	Resistor, 0.200Ω, 1%, 1W	2512	Vishay	WSL2512R200FB43
1	R17	Resistor, 46.4kΩ, 1%, 1/8W	0805	Various	
1	R18	Resistor, 402Ω, 1%, 1/8W	0805	Various	
1	SW1	Switch, DPST	SMT	C&K Components	GT21MSKE
6	TP1, TP3, TP4, TP5, TP7, TP8	Small Test Point	Thru Hole	Jolo	SPCJ-123-01
3	TP2, TP6, TP10	Large Test Point	Thru Hole	Keystone	1514-2
2	TP9, TP11	Probe Socket	Thru Hole	Tektronics	1314353-00
2	U1, U3	Synchronous Buck Driver IC	8-Lead SOIC	Intersil	HIP6601ACB
1	U2	Multiphase Buck Controller IC	16-Lead SOIC	Intersil	ISL6553CB
1	U4	MOSFET Driver IC	8-Lead SOIC	Intersil	HIP2100IB

HIP6553EVAL1 Layout

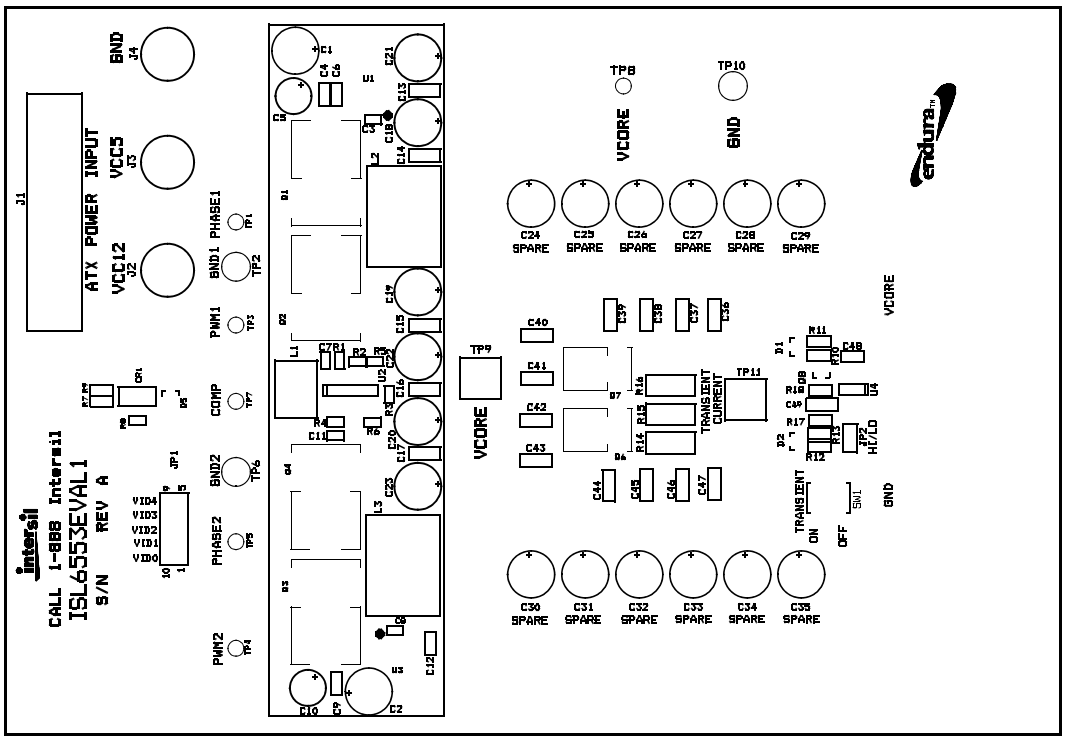

FIGURE 10. TOP SILK SCREEN

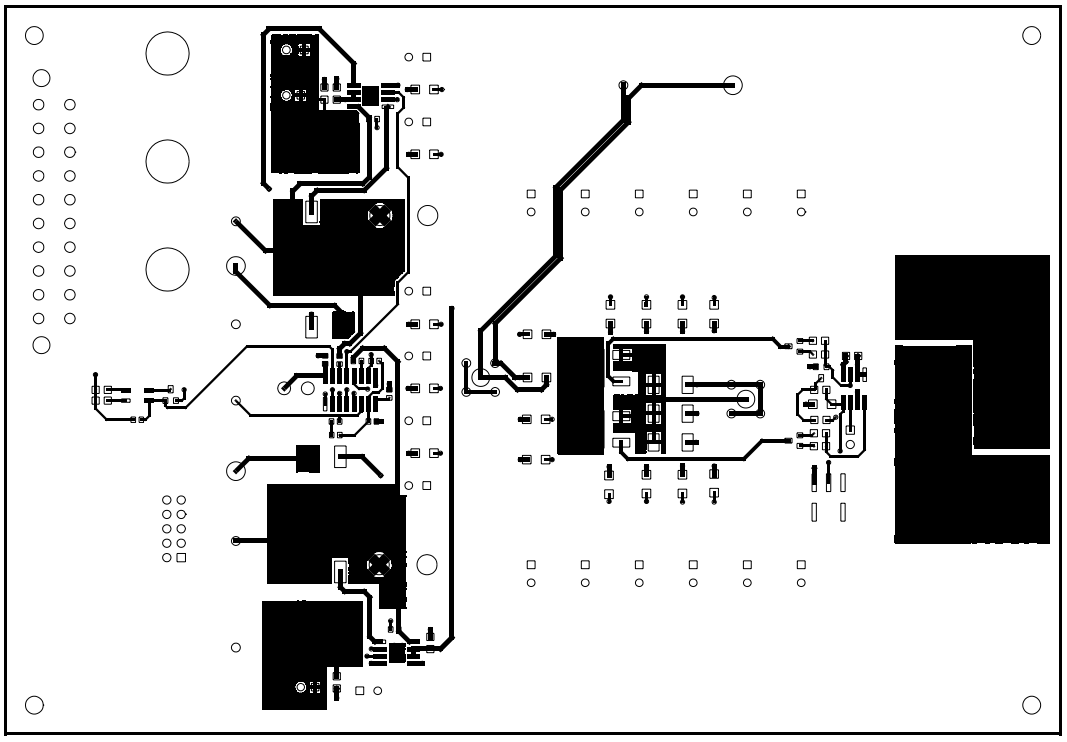

FIGURE 11. TOP COPPER

HIP6553EVAL1 Layout (Continued)

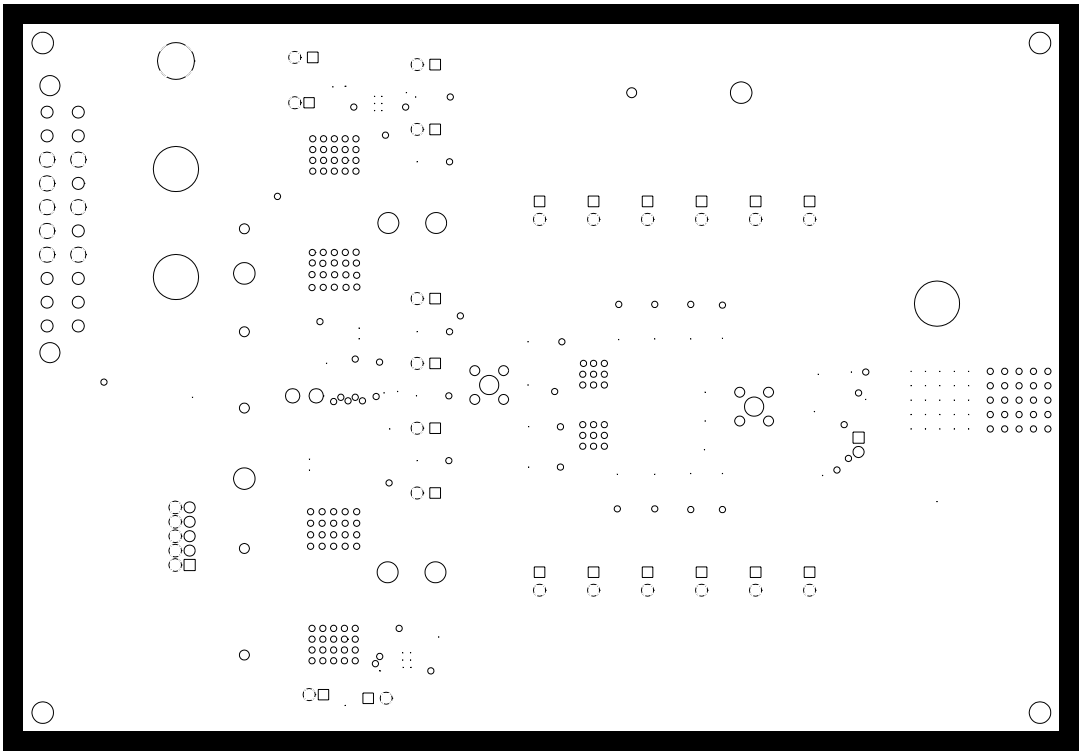

FIGURE 12. GROUND PLANE

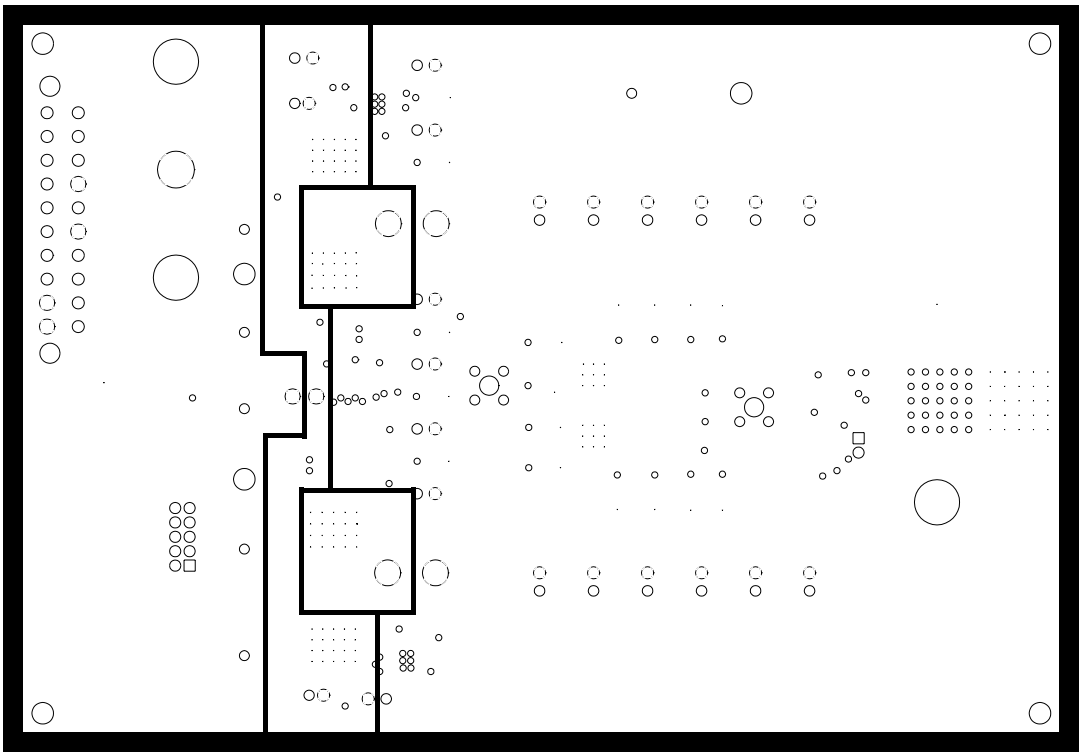

FIGURE 13. POWER PLANE

HIP6553EVAL1 Layout (Continued)

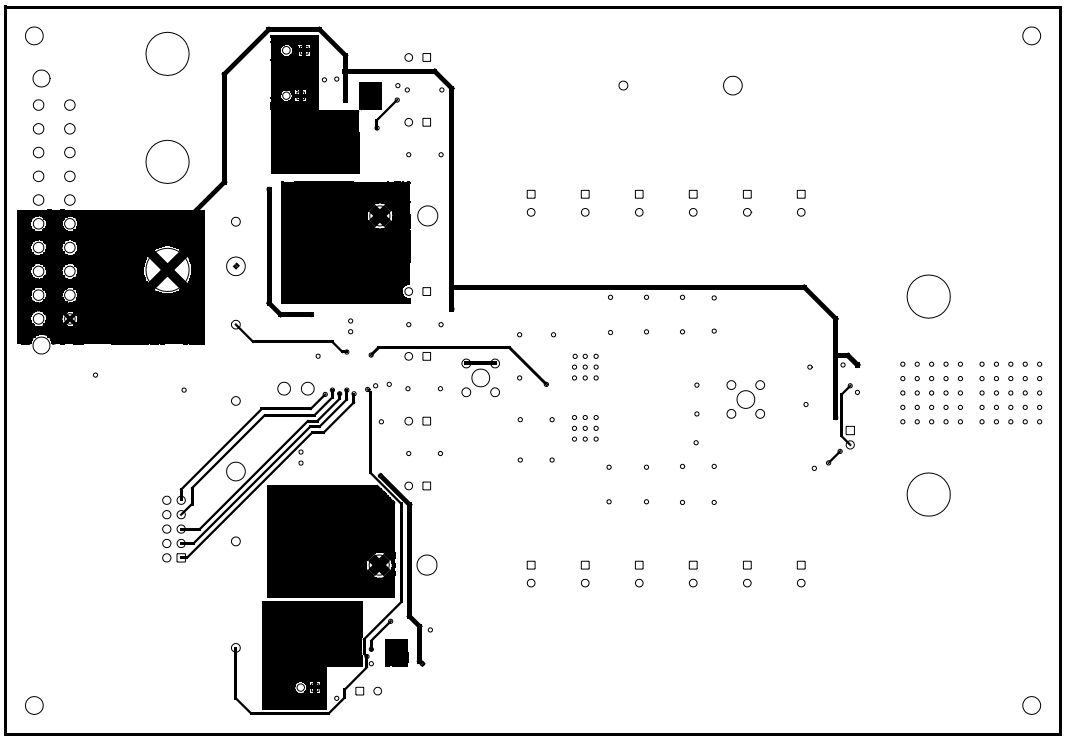

FIGURE 14. BOTTOM COPPER