



# STD15NF10

N-channel 100 V, 0.060  $\Omega$ , 23 A, DPAK  
low gate charge STripFET™ II Power MOSFET

## Features

| Type      | V <sub>DSS</sub> | R <sub>DS(on)</sub> max | I <sub>D</sub> |
|-----------|------------------|-------------------------|----------------|
| STD15NF10 | 100 V            | < 0.065 $\Omega$        | 23 A           |

- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

## Application

- Switching applications

## Description

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for telecom and computer applications. It is also intended for any applications with low gate drive requirements.

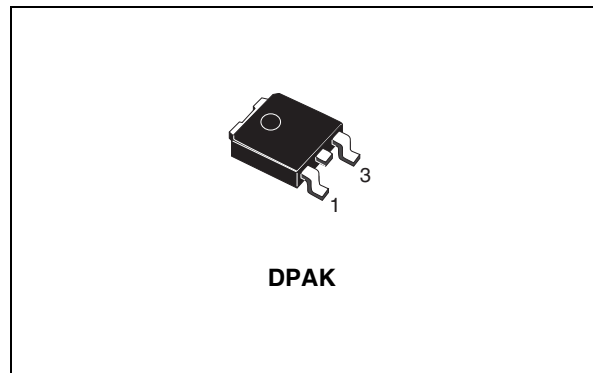


Figure 1. Internal schematic diagram

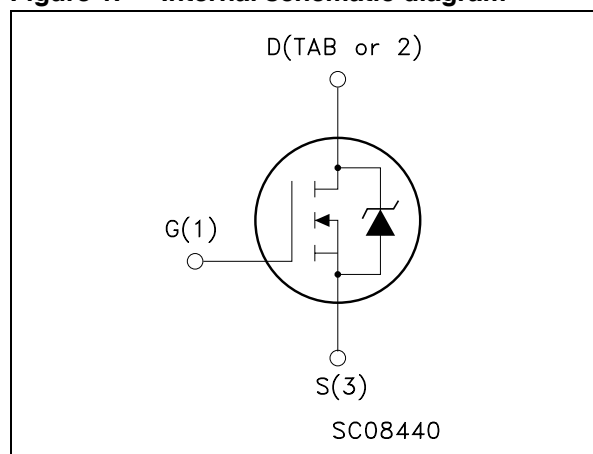


Table 1. Device summary

| Order code  | Marking | Package | Packaging     |
|-------------|---------|---------|---------------|
| STD15NF10T4 | D15NF10 | DPAK    | Tape and reel |

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol         | Parameter  | Value      | Unit                |
|----------------|--|------------|---------------------|
| $V_{DS}$       | Drain-source voltage ( $V_{GS} = 0$ )                            | 100        | V                   |
| $V_{DGR}$      | Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )             | 100        | V                   |
| $V_{GS}$       | Gate-source voltage  | $\pm 20$   | V                   |
| $I_D$          | Drain current (continuous) at $T_C = 25 \text{ }^\circ\text{C}$  | 23         | A                   |
| $I_D$          | Drain current (continuous) at $T_C = 100 \text{ }^\circ\text{C}$ | 16         | A                   |
| $I_{DM}^{(1)}$ | Drain current (pulsed)   | 92         | A                   |
| $P_{TOT}$      | Total dissipation at $T_C = 25 \text{ }^\circ\text{C}$           | 70         | W                   |
|                | Derating factor  | 0.46       | W/ $^\circ\text{C}$ |
| $E_{AS}^{(2)}$ | Single pulse avalanche energy                                    | 180        | mJ                  |
| $dv/dt^{(3)}$  | Peak diode recovery voltage slope                                | 9          | V/ns                |
| $T_{stg}$      | Storage temperature  | -55 to 175 | $^\circ\text{C}$    |
| $T_J$          | Max. operating junction temperature                              |            |                     |

1. Pulse width limited by safe operating area
2. Starting  $T_J = 25 \text{ }^\circ\text{C}$ ,  $I_D = 10\text{A}$ ,  $V_{DD} = 30\text{V}$
3.  $I_{SD} \leq 13 \text{ A}$ ,  $di/dt \leq 300 \text{ A}/\mu\text{s}$ ,  $V_{DS} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$

**Table 3. Thermal data**

| Symbol     | Parameter                                      | Value | Unit                      |
|------------|--|-------|---------------------------|
| $R_{thJC}$ | Thermal resistance junction-case max           | 2.14  | $^\circ\text{C}/\text{W}$ |
| $R_{thJA}$ | Thermal resistance junction-ambient max        | 100   | $^\circ\text{C}/\text{W}$ |
| $T_I$      | Maximum lead temperature for soldering purpose | 300   | $^\circ\text{C}$          |

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On<sup>(1)</sup> /off states**

| Symbol        | Parameter  | Test conditions  | Min. | Typ. | Max.      | Unit                           |
|---------------|--|--|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                   | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$                                  | 100  |      |           | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = \text{Max rating}$<br>$V_{DS} = \text{Max rating, @ } 125\text{ °C}$ |      |      | 1<br>10   | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 20\text{ V}$   |      |      | $\pm 100$ | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                             | 2    | 3    | 4         | V                              |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10\text{ V}$ , $I_D = 12\text{ A}$                                   |      | 0.06 | 0.065     | $\Omega$                       |

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 5. Dynamic**

| Symbol         | Parameter                    | Test conditions  | Min. | Typ. | Max. | Unit |
|----------------|------------------------------|--|------|------|------|------|
| $g_{fs}^{(1)}$ | Forward transconductance     | $V_{DS} = 15\text{ V}$ , $I_D = 7.5\text{ A}$                          |      | 12   |      | S    |
| $C_{iss}$      | Input capacitance            | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$          |      | 870  |      | pF   |
| $C_{oss}$      | Output capacitance           |  |      | 125  |      | pF   |
| $C_{rss}$      | Reverse transfer capacitance |  |      | 50   |      | pF   |
| $Q_g$          | Total gate charge            | $V_{DD} = 80\text{ V}$ , $I_D = 24\text{ A}$<br>$V_{GS} = 10\text{ V}$ |      | 30   | 40   | nC   |
| $Q_{gs}$       | Gate-source charge           |  |      | 6    |      | nC   |
| $Q_{gd}$       | Gate-drain charge            |  |      | 10   |      | nC   |

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions  | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 50\text{ V}$ , $I_D = 12\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br><i>Figure 13 on page 8</i> |      | 60   |      | ns   |
| $t_r$        | Rise time           |  |      | 45   |      | ns   |
| $t_{d(off)}$ | Turn-off delay time |  |      | 49   |      | ns   |
| $t_f$        | Fall time           |  |      | 17   |      | ns   |

Table 7. Source drain diode

| Symbol                            | Parameter  | Test conditions  | Min | Typ.              | Max | Unit          |
|-----------------------------------|--|--|-----|-------------------|-----|---------------|
| $I_{SD}$                          | Source-drain current   |  |     |                   | 23  | A             |
| $I_{SDM}^{(1)}$                   | Source-drain current (pulsed)  |  |     |                   | 92  | A             |
| $V_{SD}^{(2)}$                    | Forward on voltage   | $I_{SD} = 20 \text{ A}$ , $V_{GS} = 0$   |     |                   | 1.5 | V             |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD} = 24 \text{ A}$ ,<br>$di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 30 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$<br><i>Figure 15 on page 8</i> |     | 100<br>375<br>7.5 |     | ns<br>nC<br>A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

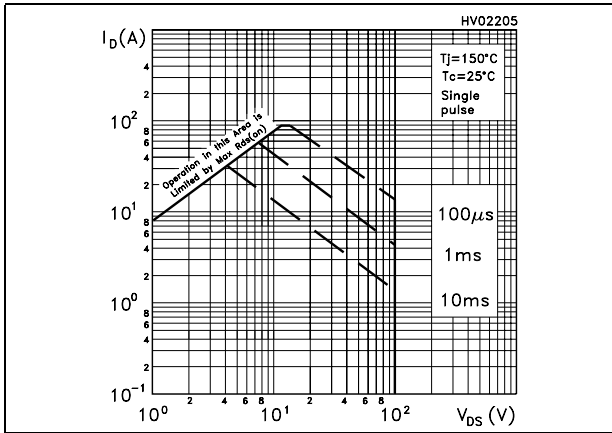


Figure 3. Thermal impedance

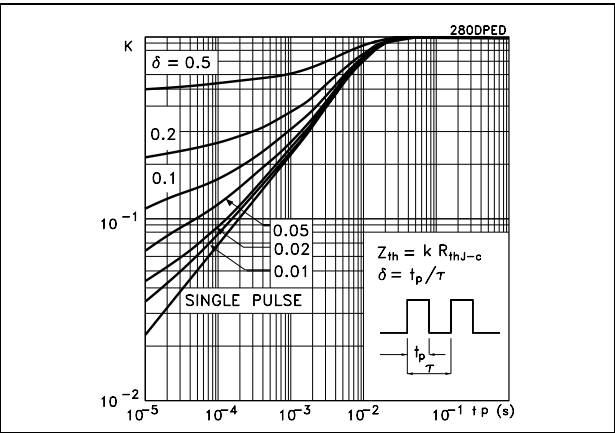


Figure 4. Output characteristics

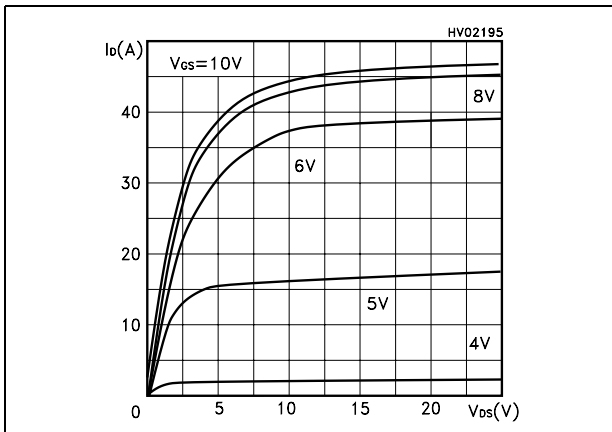


Figure 5. Transfer characteristics

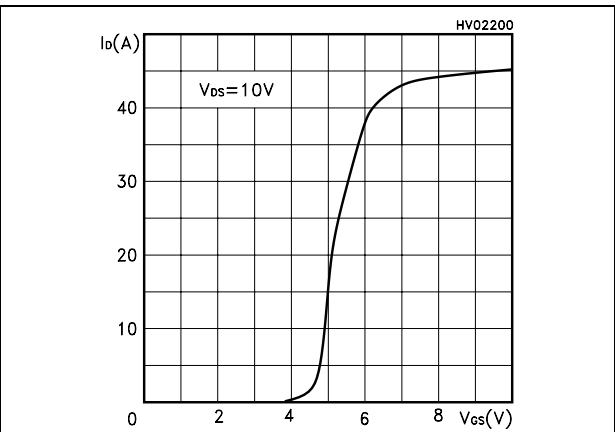


Figure 6. Transconductance

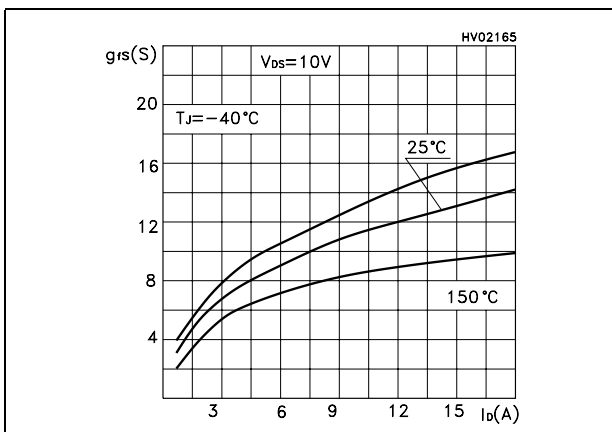


Figure 7. Static drain-source on resistance

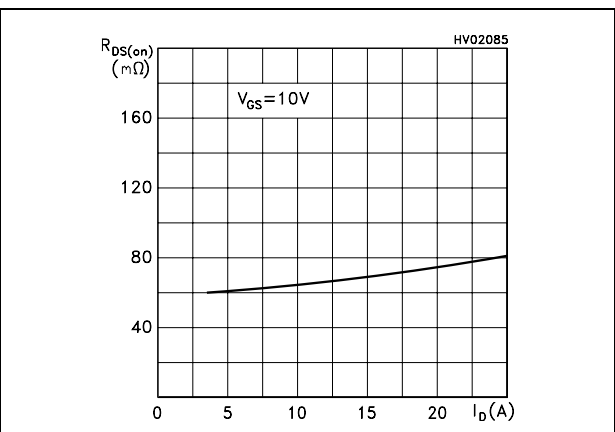


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

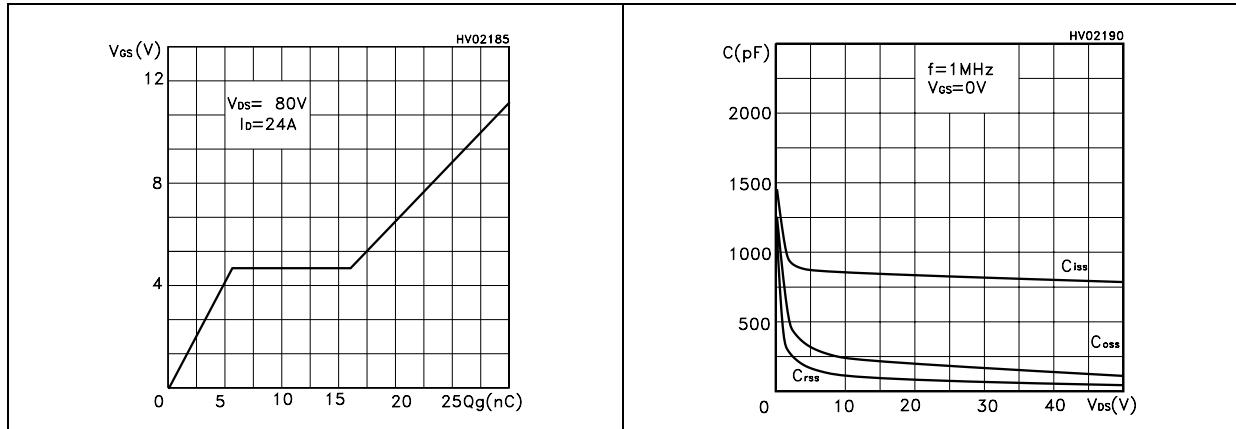


Figure 10. Normalized gate threshold voltage vs. temperature Figure 11. Normalized on resistance vs. temperature

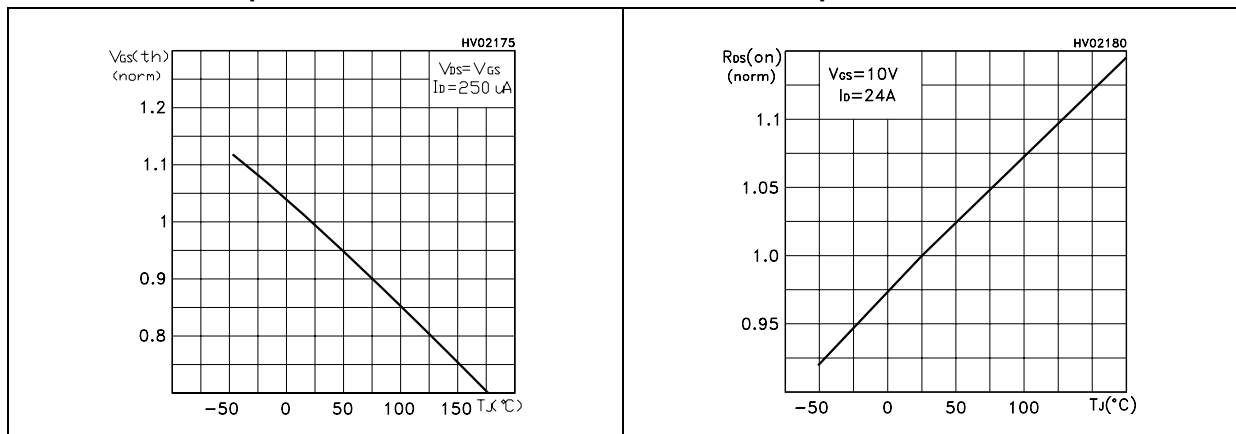
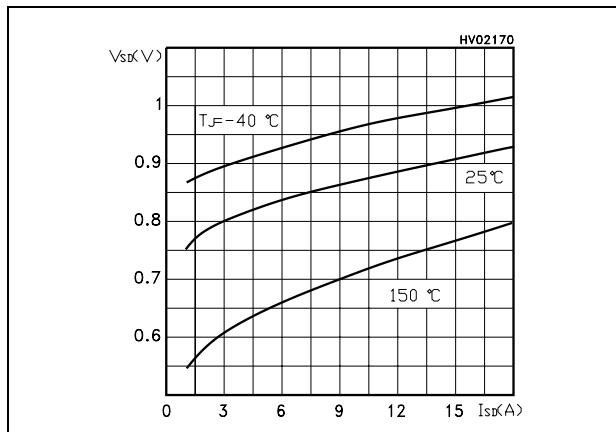


Figure 12. Source-drain diode forward characteristics



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

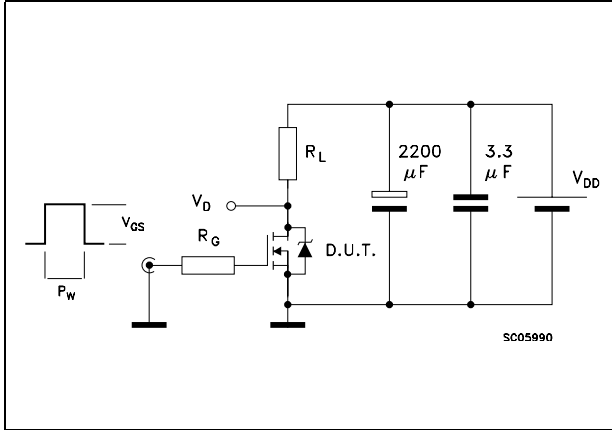


Figure 14. Gate charge test circuit

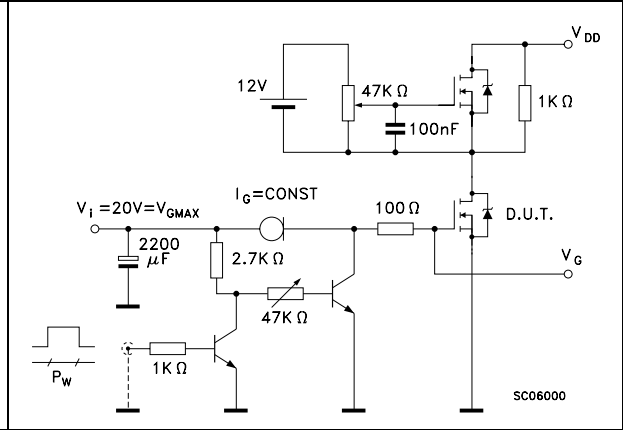


Figure 15. Test circuit for inductive load switching and diode recovery times

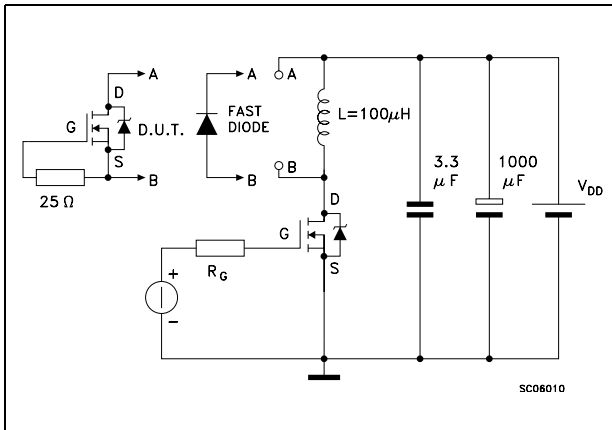


Figure 16. Unclamped Inductive load test circuit

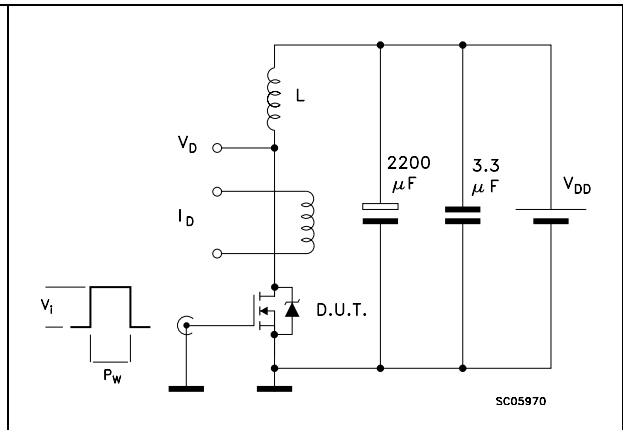
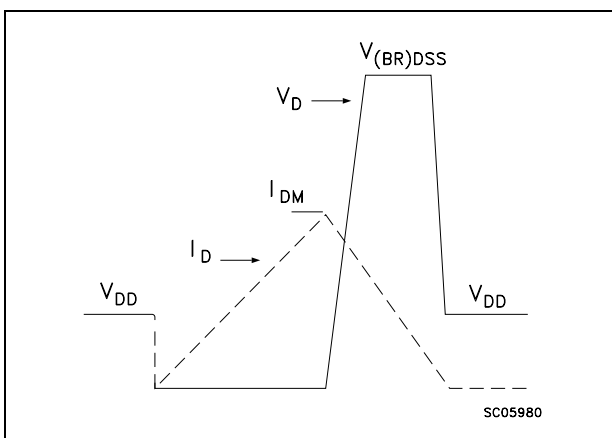


Figure 17. Unclamped inductive waveform



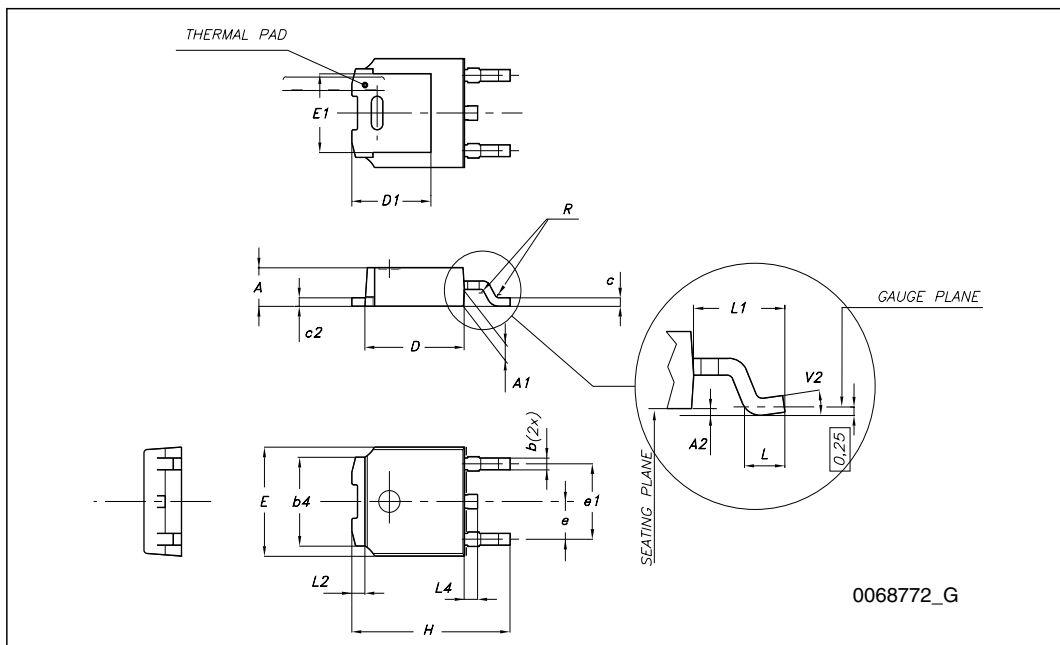


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

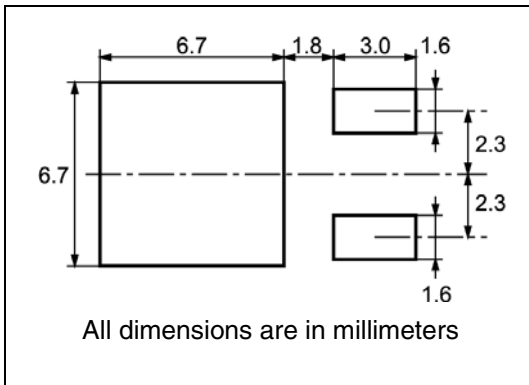
**TO-252 (DPAK) mechanical data**

| DIM. | mm.  |      |       |
|------|------|------|-------|
|      | min. | typ  | max.  |
| A    | 2.20 |      | 2.40  |
| A1   | 0.90 |      | 1.10  |
| A2   | 0.03 |      | 0.23  |
| b    | 0.64 |      | 0.90  |
| b4   | 5.20 |      | 5.40  |
| c    | 0.45 |      | 0.60  |
| c2   | 0.48 |      | 0.60  |
| D    | 6.00 |      | 6.20  |
| D1   |      | 5.10 |       |
| E    | 6.40 |      | 6.60  |
| E1   |      | 4.70 |       |
| e    |      | 2.28 |       |
| e1   | 4.40 |      | 4.60  |
| H    | 9.35 |      | 10.10 |
| L    | 1    |      |       |
| L1   |      | 2.80 |       |
| L2   |      | 0.80 |       |
| L4   | 0.60 |      | 1     |
| R    |      | 0.20 |       |
| V2   | 0°   |      | 8°    |



# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

| DIM. | mm   |      | inch  |        |
|------|------|------|-------|--------|
|      | MIN. | MAX. | MIN.  | MAX.   |
| A    |      | 330  |       | 12.992 |
| B    | 1.5  |      | 0.059 |        |
| C    | 12.8 | 13.2 | 0.504 | 0.520  |
| D    | 20.2 |      | 0.795 |        |
| G    | 16.4 | 18.4 | 0.645 | 0.724  |
| N    | 50   |      | 1.968 |        |
| T    |      | 22.4 |       | 0.881  |

| BASE QTY |  | BULK QTY |  |
|----------|--|----------|--|
| 2500     |  | 2500     |  |

| DIM. | mm   |      | inch  |       |
|------|------|------|-------|-------|
|      | MIN. | MAX. | MIN.  | MAX.  |
| A0   | 6.8  | 7    | 0.267 | 0.275 |
| B0   | 10.4 | 10.6 | 0.409 | 0.417 |
| B1   |      | 12.1 |       | 0.476 |
| D    | 1.5  | 1.6  | 0.059 | 0.063 |
| D1   | 1.5  |      | 0.059 |       |
| E    | 1.65 | 1.85 | 0.065 | 0.073 |
| F    | 7.4  | 7.6  | 0.291 | 0.299 |
| K0   | 2.55 | 2.75 | 0.100 | 0.108 |
| P0   | 3.9  | 4.1  | 0.153 | 0.161 |
| P1   | 7.9  | 8.1  | 0.311 | 0.319 |
| P2   | 1.9  | 2.1  | 0.075 | 0.082 |
| R    | 40   |      | 1.574 |       |
| W    | 15.7 | 16.3 | 0.618 | 0.641 |

10 pitches cumulative tolerance on tape +/- 0.2 mm

User Direction of Feed

Center line of cavity

TRL

FEED DIRECTION

Bending radius R min.

## 6 Revision history

**Table 8. Revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 21-Jun-2004 | 3        | No history because migration.   |
| 09-Sep-2004 | 4        | Complete document   |
| 08-Aug-2006 | 5        | New template, updated SOA   |
| 04-Nov-2008 | 6        | Q <sub>G</sub> max value in <a href="#">Table 5</a> has been corrected. |

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