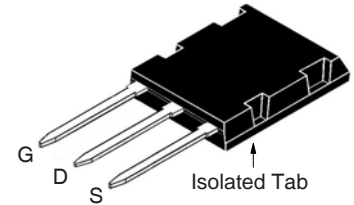


**Polar3™ HiPerFET™
Power MOSFET**
IXFL210N30P3
(Electrically Isolated Tab)

 N-Channel Enhancement Mode
 Avalanche Rated
 Fast Intrinsic Rectifier


$$\begin{aligned} V_{DSS} &= 300V \\ I_{D25} &= 108A \\ R_{DS(on)} &\leq 16m\Omega \\ t_{rr} &\leq 250ns \end{aligned}$$

ISOPLUS264


 G = Gate D = Drain
 S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	300	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	300	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	108	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	550	A
I_A	$T_C = 25^\circ\text{C}$	105	A
E_{AS}	$T_C = 25^\circ\text{C}$	4	J
dv/dt	$I_S \leq I_{DM}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150^\circ\text{C}$	35	V/ns
P_D	$T_C = 25^\circ\text{C}$	520	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
F_C	Mounting Force	40..120 / 9..27	N/lb
V_{ISOL}	50/60 Hz, RMS $t = 1$ min	2500	V~
	$I_{ISOL} \leq 1$ mA $t = 1$ s	3000	V~
Weight		8	g

Features

- Silicon Chip on Direct-Copper-Bond Substrate
 - High Power Dissipation
 - Isolated Mounting Surface
 - 2500V~ Electrical Isolation
- Dynamic dv/dt Rating
- Avalanche Rated
- Fast Intrinsic Rectifier
- Low $R_{DS(on)}$
- Low Drain-to-Tab Capacitance
- Low Package Inductance

Advantages

- Easy to Mount
- Space Savings

Applications

- DC-DC Converters
- Battery Chargers
- Switch-Mode and Resonant-Mode Power Supplies
- Uninterrupted Power Supplies
- AC Motor Drives
- High Speed Power Switching Applications

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 3mA$	300		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8mA$	2.5		5.0 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ Note 2, $T_J = 125^\circ\text{C}$			50 μA 1.5 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 105A$, Note 1			16 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}, I_D = 60\text{A}$, Note 1	60	100	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		16.2	nF
C_{oss}			2550	pF
C_{rss}			42	pF
R_{Gi}	Gate Input Resistance		1.0	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{DSS}$ $R_G = 1\Omega$ (External)		46	ns
t_r			25	ns
$t_{d(off)}$			94	ns
t_f			13	ns
$Q_{g(on)}$		$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{DSS}$		268
Q_{gs}			80	nC
Q_{gd}			72	nC
R_{thJC}				0.24°C/W
R_{thCS}		0.15		$^\circ\text{C/W}$

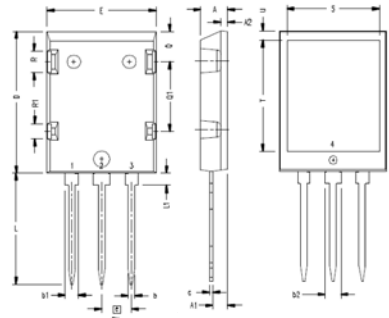
Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_s	$V_{GS} = 0\text{V}$			210 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			840 A
V_{SD}	$I_F = 100\text{A}, V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 105\text{A}, -di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}, V_{GS} = 0\text{V}$			250 ns
Q_{RM}			4.1	μC
I_{RM}			28	A

Notes:

1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
2. Part must be heatsunk for high-temp I_{DSS} measurement.

ISOPLUS264 (IXFL) OUTLINE



1 = Gate
2,4 = Drain
3 = Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.055	1.17	1.40
b	.045	.055	1.14	1.40
b1	.087	.102	2.21	2.59
b2	.111	.126	2.82	3.20
c	.020	.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	.770	.799	19.56	20.29
e	.215 BSC		5.46 BSC	
L	.780	.820	19.81	20.83
L1	.080	.102	2.03	2.59
Q	.210	.235	5.33	5.97
Q1	.490	.513	12.45	13.03
R	.150	.180	3.81	4.57
R1	.100	.130	2.54	3.30
S	.668	.690	16.97	17.53
T	.801	.821	20.34	20.85
U	.065	.080	1.65	2.03

PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

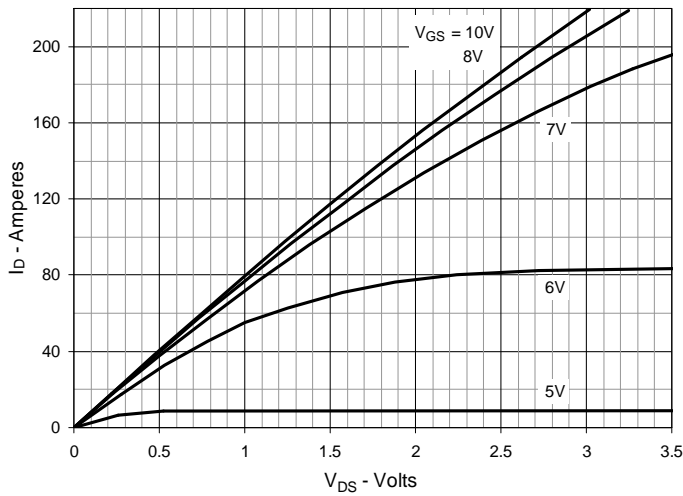
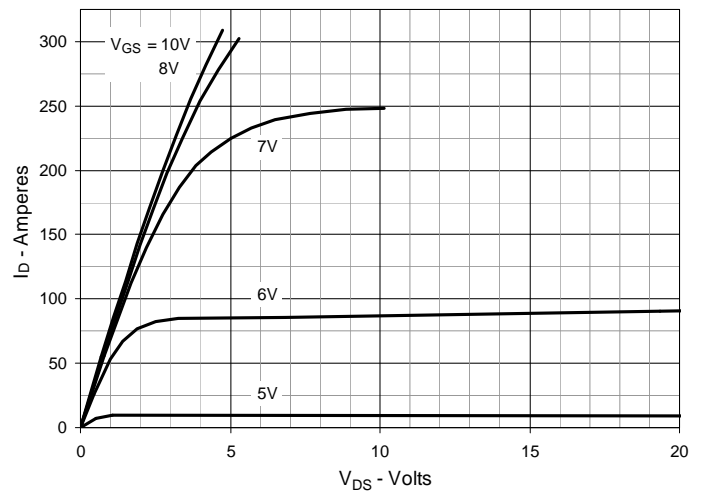
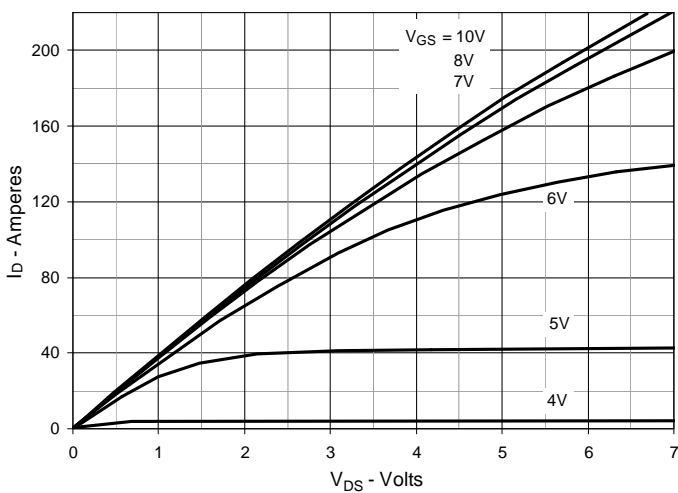
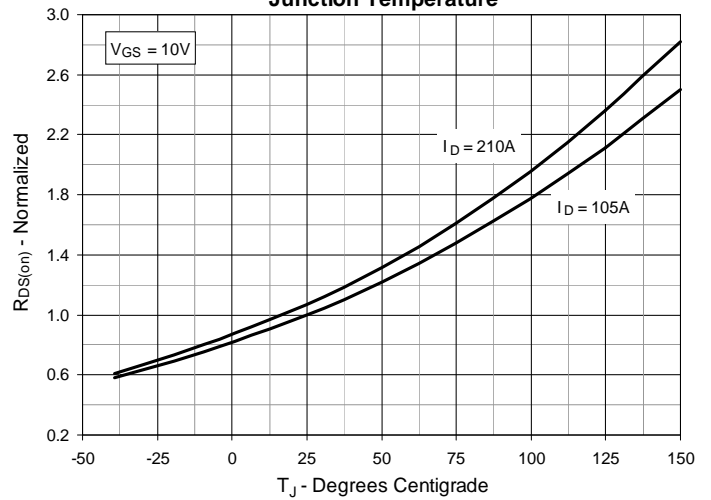
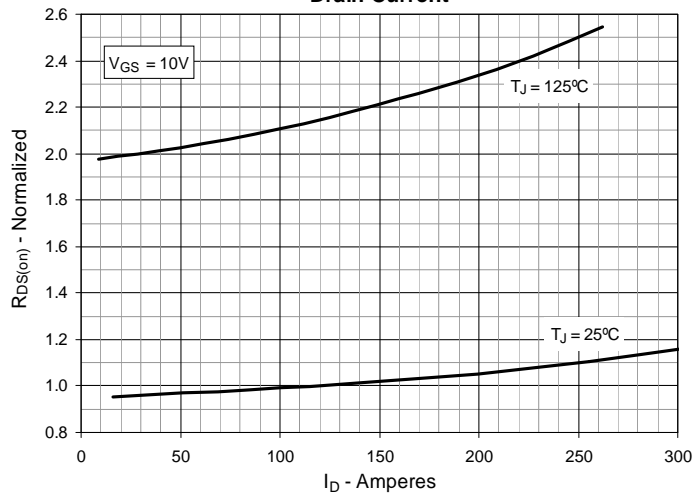
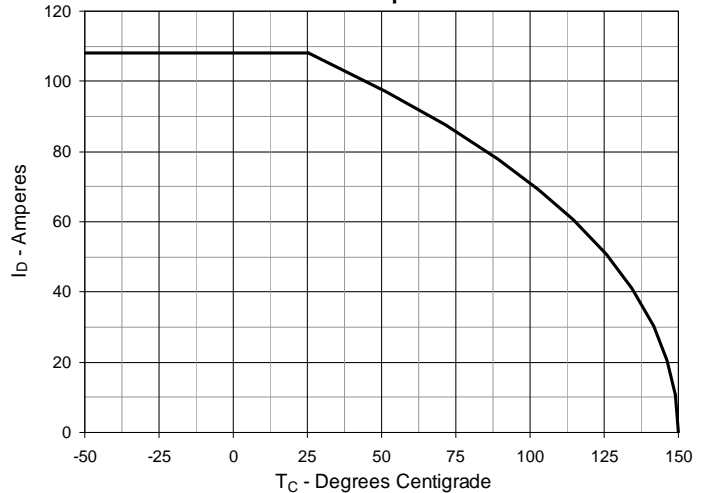
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 105\text{A}$ Value vs. Junction Temperature

Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 105\text{A}$ Value vs. Drain Current

Fig. 6. Maximum Drain Current vs. Case Temperature


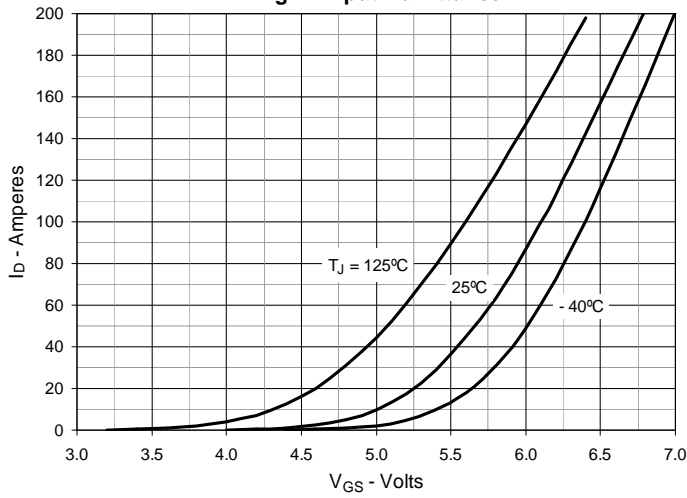
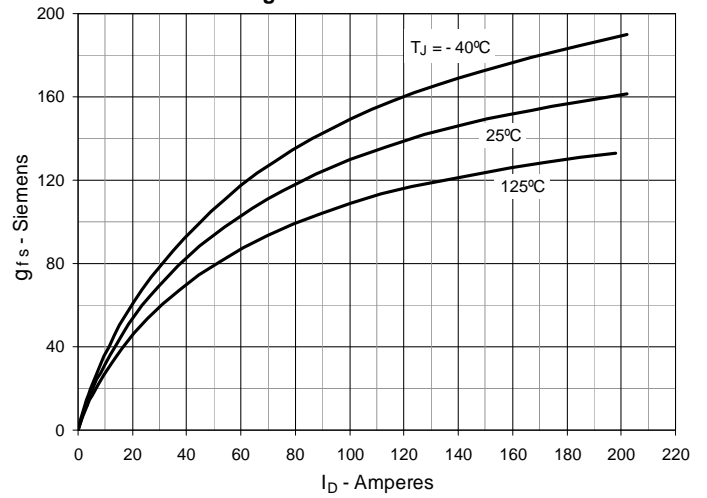
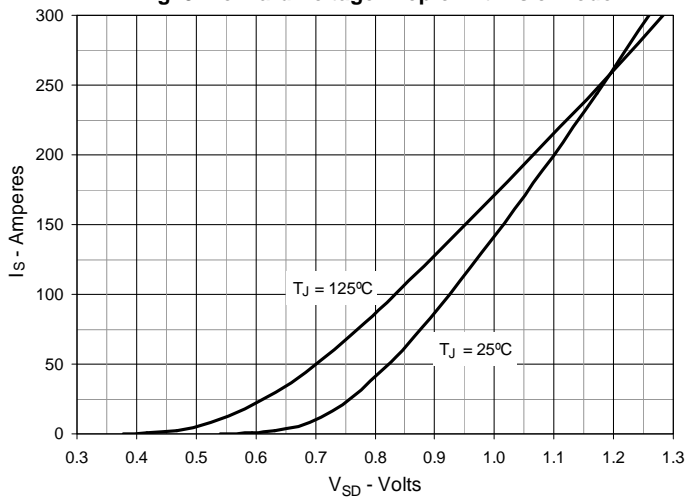
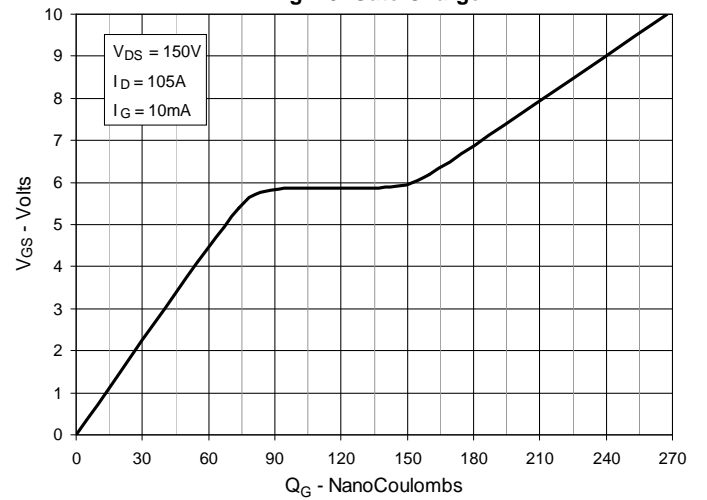
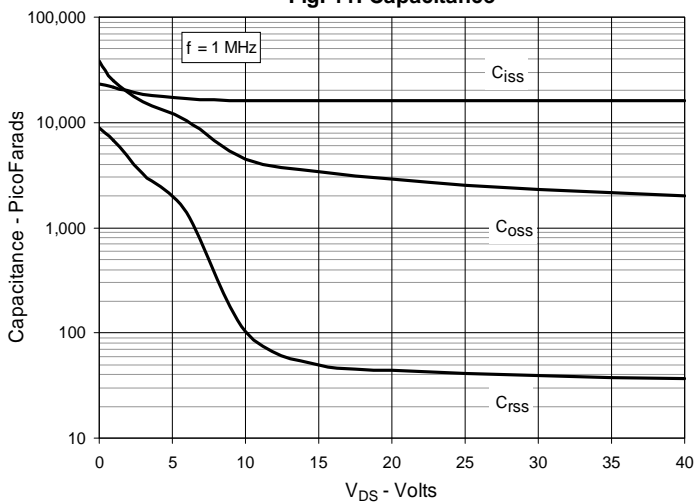
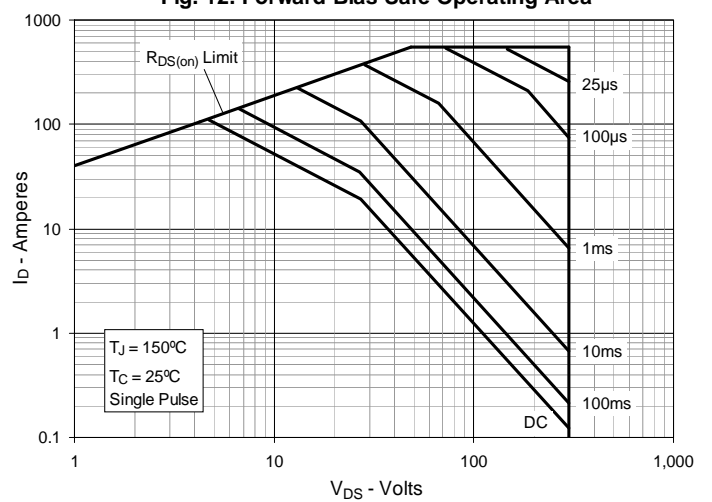
Fig. 7. Input Admittance

Fig. 8. Transconductance

Fig. 9. Forward Voltage Drop of Intrinsic Diode

Fig. 10. Gate Charge

Fig. 11. Capacitance

Fig. 12. Forward-Bias Safe Operating Area


Fig. 13. Maximum Transient Thermal Impedance

