ZL30264–ZL30267

2-APLL, 6- or 10-Output Any-to-Any Clock Multiplier and Frequency Synthesizer

Product Brief

September 2016

Features

- **Four Flexible Input Clocks**
  - One crystal/CMOS input
  - Two differential/CMOS inputs
  - One single-ended/CMOS input
  - Any input frequency from 9.72MHz to 1.25GHz (300MHz max for CMOS)
  - Activity monitors, automatic or manual switching
  - Glitchless clock switching by pin or register
- **6 or 10 Any-Frequency, Any-Format Outputs**
  - Any output frequency from 1Hz to 1045MHz
  - Two fractional-N APLLs with 0ppm error
  - **Each APLL has a fractional divider and an integer divider to make a total of four independent frequency families**
  - Output jitter from integer multiply and dividers as low as 0.17ps RMS (12kHz-20MHz)
  - Output jitter from fractional dividers is typically < 1ps RMS, many frequencies <0.5ps RMS
  - Each output has an independent divider
  - Each output configurable as LVDS, LVPECL, HCSL, 2xCMOS or HSTL
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)
  - Multiple output supply voltage banks with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry and per-output phase adjustment
  - Per-output enable/disable and glitchless start/stop (stop high or low)
- **General Features**
  - Automatic self-configuration at power-up from external (ZL30264 or 6) or internal (ZL30265 or 7) EEPROM; up to 8 configurations pin-selectable
  - External feedback for zero-delay applications
  - Numerically controlled oscillator mode
  - Spread-spectrum modulation mode
  - Easy-to-configure design requires no external VCXO or loop filter components
  - SPI or I^2C processor Interface
  - Core supply voltage options: 2.5V only, 3.3V only, 1.8V+2.5V or 1.8V+3.3V
  - Space-saving 8x8mm QFN56 (0.5mm pitch)
  - Easy-to-use evaluation/programming software

Ordering Information

ZL30264LDG1	ext. EEPROM	6 Outputs	Trays
ZL30264LDF1	ext. EEPROM	6 Outputs	Tape and Reel
ZL30265LDG1	int. EEPROM	6 Outputs	Trays
ZL30265LDF1	int. EEPROM	6 Outputs	Tape and Reel
ZL30266LDG1	ext. EEPROM	10 Outputs	Trays
ZL30266LDF1	ext. EEPROM	10 Outputs	Tape and Reel
ZL30267LDG1	int. EEPROM	10 Outputs	Trays
ZL30267LDF1	int. EEPROM	10 Outputs	Tape and Reel

Matte Tin
Package size: 8 x 8 mm, 56 Pin QFN
-40°C to +85°C

Applications

- Frequency conversion and frequency synthesis in a wide variety of equipment types

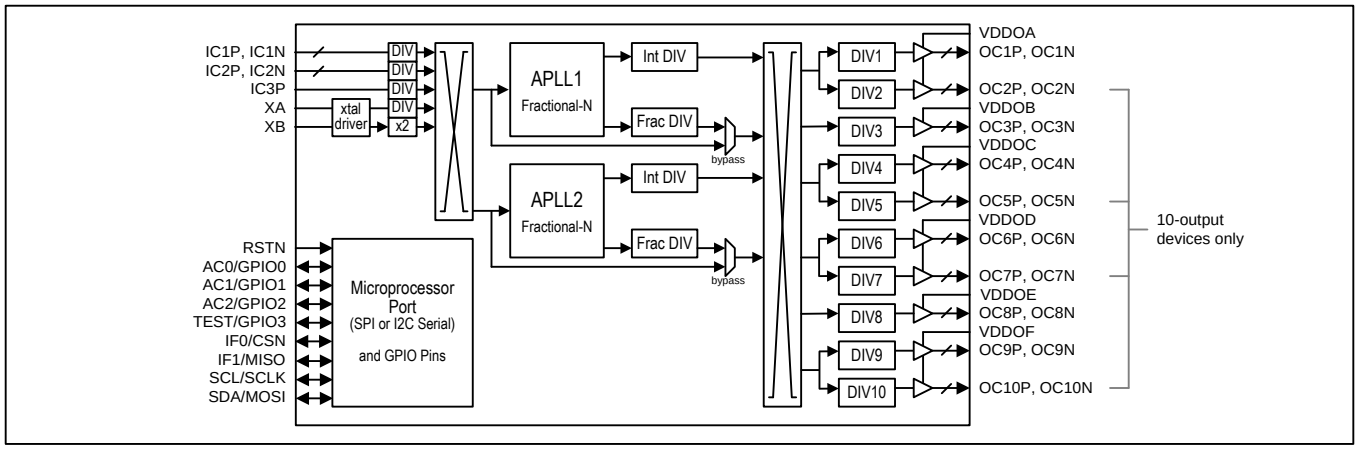


Figure 1 - Functional Block Diagram

1. Application Example

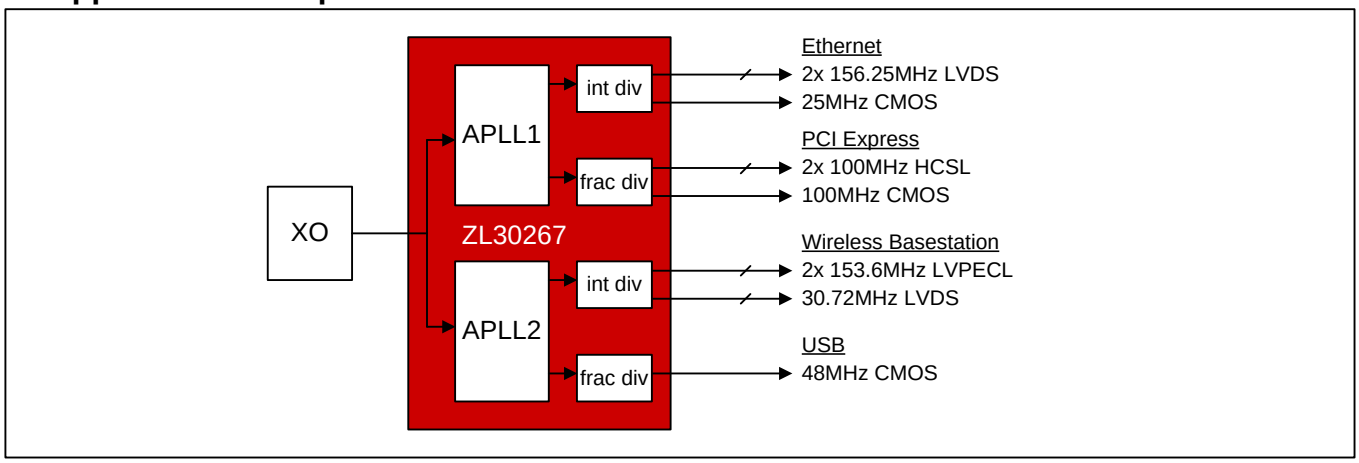


Figure 2 – Ethernet, PCIe, Wireless and USB Clocks Simultaneously

2. Detailed Features

2.1 Input Clock Features

- Four input clocks: one crystal/CMOS, two differential/CMOS, one single-ended/CMOS
- Input clocks can be any frequency from 9.72MHz to 1250MHz (differential) or 300MHz (single-ended)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Activity monitor and glitchless input switching

2.2 APLL Features

- Two APLLs with very high-resolution fractional (i.e. non-integer) frequency multiplication
- Any-to-any frequency conversion with 0ppm error
- Two output dividers per APLL: one integer divider (4 to 15 plus half divides 4.5 to 7.5) and one fractional divider to make a total of four output frequency families
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter
- Bypass mode supports system testing

2.3 Output Clock Features

- Six (ZL30264 or ZL30265) or ten (ZL30266 or ZL30267) low-jitter output clocks
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for HCSL, CMOS and HSTL)
- Output jitter from integer multiply and integer dividers as low as 0.17ps RMS (12kHz to 20MHz)
- Output jitter from fractional dividers is typically <1ps RMS, many frequencies <0.5ps RMS (12kHz to 20MHz)
- In CMOS mode, the OCxP and OCxN pins can be different divisors (Example 1: OC3P 125MHz, OC3N 25MHz; Example 2: OC3P 25MHz, OC3N 1Hz/1PPS)
- Outputs directly interface (DC coupled) with LVDS, LVPECL, HSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe clocks (PCIe gen. 1, 2 and 3)
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.4 General Features

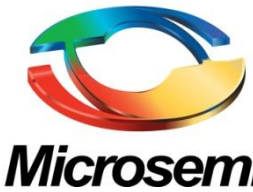
- SPI or I^2C serial microprocessor interface
- Automatic self-configuration at power-up; pin control to specify one of 8 stored configurations
  ZL30264 and ZL30266: preset configurations in ROM or user configurations in external EEPROM

ZL30265 and ZL30267: user configurations in internal EEPROM

- Numerically controlled oscillator (NCO) mode allows system software to steer DPLL frequency with resolution better than 0.01ppb
- Spread-spectrum modulation mode (meets PCI Express requirements)
- Zero-delay buffer configuration using an external feedback path
- Four general-purpose I/O pins each with many possible status and control options
- Reference can be fundamental-mode crystal, low-cost XO or clock signal from elsewhere in the system

2.5 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the ZL30264/5/6/7 quick and easy
- Generates configuration scripts to be stored in external (ZL30264/6) or internal (ZL30265/7) EEPROM
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without an evaluation board



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