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DATASHEET

Wide V_{IN} Dual Integrated Buck Regulator With 4A/4A Continuous Output Current and LDOs

ISL95901

The ISL95901 is a dual, high-efficient buck regulator capable of 4A per channel continuous output current. It integrates two LDOs and one low-impedance switch. This power management IC delivers power in portable and embedded systems. With an input range of 4.5V to 16V, it provides a high frequency power solution for a variety of point-of-load applications. Outputs are adjustable to meet system needs.

A PWM controller drives two pairs of internal switching N-channel power MOSFETs to generate output voltage. The integrated power switch is optimized for excellent thermal performance for up to 4A of output current per channel.

The ISL95901 modulator features Intersil R4™ Technology, which combines the best features of fixed-frequency and hysteretic PWMs while eliminating many of their drawbacks. Like R3™ Technology, the R4™ Technology allows variable frequency in response to load transients and maintains the benefits of current-mode hysteretic controllers. In addition, it reduces regulator output impedance and uses accurate referencing to eliminate the need for a high-gain voltage amplifier. The resulting topology can be tuned to voltage-mode hysteretic transient speed while maintaining a linear control model. This topology removes the need for compensation, which greatly simplifies regulator design for customers and reduces external component count and cost.

Protection features include overcorrect, negative overcorrect, UVLO and thermal overload. The ISL95901 is available in a 46 Ld 5mmx6mm Quad Flat (QFN) Pb-free package.

Features

- Wide input voltage range from 4.5V to 16V
- Adjustable output voltages with continuous output current up to 4A
- 1% accuracy over temperature and V_{CC} range
- Built-in low-power LDO for external µC
- Built-in compensation
- Internally set SS and OCP
- Independent enable, power-good and standby control inputs for each output
- Innovative R4™ Modulator
- Boot undervoltage detection

Applications

- General purpose, point-of-load DC/DC power conversion
- Notebook, netbook and tablet
- Embedded computing system

Related Literature

- See AN1743 "Wide V_{IN} Dual Integrated Buck Regulator With 4A/4A Continuous Output Current and LDOs"
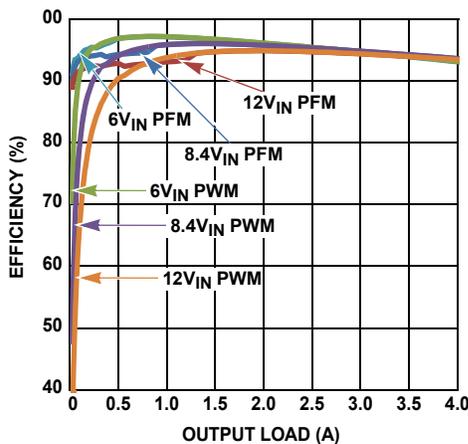

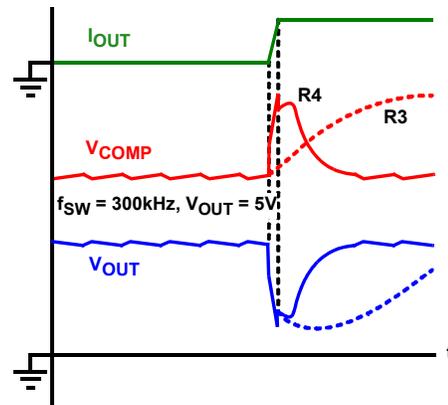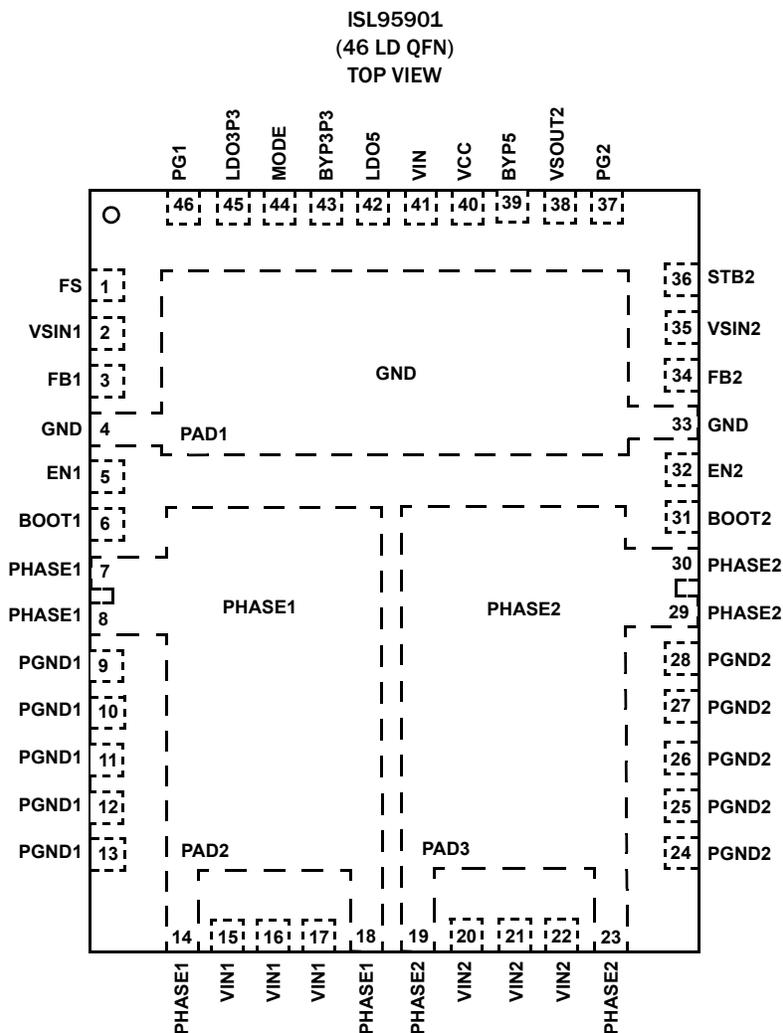FIGURE 1. EFFICIENCY vs LOAD, V_{IN} = 12V, T_A = +25°C

FIGURE 2. R3™ vs R4™ IDEALIZED TRANSIENT RESPONSE

Table of Contents

ISL95901

Pin Configuration

Pin Descriptions

PIN NUMBER	SYMBOL	PIN DESCRIPTION
1	FS	Buck switching frequency selection. Tie to high for 1MHz, float for 500kHz, tie to GND for 300kHz.
2	VSIN1	Sensing for output of Switching Mode Power Supply 1 -SMPS1. Must be connected to channel 1 output side of inductor.
3	FB1	SMPS1 feedback input. Connect FB1 to a resistive voltage divider from SVIN1 to GND1 to adjust the output from 0.8V to 5.5V.
4, 33, PAD1	GND	Analog ground for buck controllers and LDOs. Kelvin connect GND to the negative terminal of SMPS1/2. For optimal thermal performance, place as many vias as possible under PAD1 and connecting to GND plane.
5	EN1	SMPS1 controller enable input. PWM controller is held off when pin is pulled to ground. When voltage on this pin rises above 1.4V, PWM controller is enabled.
6	BOOT1	Floating bootstrap supply pin for power MOSFET gate driver. Bootstrap capacitor provides necessary charge to turn on high-side internal N-channel MOSFET of channel 1. Connect an external capacitor from this pin to PHASE1.
7, 8, 14, 18, PAD2	PHASE1	Switch node output of channel 1. Connects source of internal power MOSFETs with external output inductor. Connect exposed PAD2 as close to inductor of SMPS1 as possible.
9, 10, 11, 12, 13	PGND1	Power ground of SMPS1.

ISL95901

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	PIN DESCRIPTION
15, 16, 17	VIN1	Input supply for power stage of SMPS1 regulator and source for internal linear regulator, LDO. For decoupling, place a minimum of 10µF ceramic capacitance from VIN1 to PGND1 and close to IC.
19, 23, 29, 30, PAD3	PHASE2	Switch node output of channel 2. Connects source of internal power MOSFETs with external output inductor. Connect exposed PAD3 as close to inductor of SMPS2 as possible.
20, 21, 22	VIN2	Input supply for power stage of SMPS2 regulator. For decoupling, place a minimum of 10µF ceramic capacitance from VIN2 to PGND2 and close to the IC.
24, 25, 26, 27, 28	PGND2	Power ground of SMPS2.
31	BOOT2	Floating bootstrap supply pin for power MOSFET gate driver. Bootstrap capacitor provides necessary charge to turn on high-side internal N-channel MOSFET of channel 2. Connect an external capacitor from this pin to PHASE2.
32	EN2	SMPS2 controller enable input. PWM controller is held off when pin is pulled to ground. When voltage on this pin rises above 1.4V, PWM controller is enabled.
34	FB2	SMPS2 feedback Input. Connect FB2 to a resistive voltage divider from SVIN2 to GND2 to adjust the output from 0.8V to 5.5V.
35	VSIN2	Sensing for output of SMPS2. Must be connected to channel 2 output side of inductor.
36	STB2	Standby output 2 enable input. Standby output 2 is held off when pin is pulled to ground. When voltage on this pin rises above 1.4V, standby output 2 controller is enabled.
37	PG2	Open drain power-good of SMPS2. Pulled to ground when output voltage is below regulation limits or during soft-start interval. Contains an internal 5MΩ pull-up resistor.
38	VSOUT2	Standby output 2. There is a switch between VSIN2 and VSOUT2.
39	BYP5	Connect BYP5 to 5V buck output or external 5V source, this will allow IC to disable VCC and LDO5, then the power source will be drawn from BYP5 to minimize internal power dissipation. Tie to GND if not use.
40	VCC	Voltage bias for gate drivers as well as all other control circuitries. Power on or off by VIN. Decouple with at least 1µF of an MLCC capacitor across VCC and PAD1.
41	VIN	Input LDO3P3, LDO5 and VCC. For decoupling, place a minimum of 1µF ceramic capacitance close to IC.
42	LDO5	5V linear regulator output. Power on or off by VIN. Can provide a total of 100mA external loads. Bypass LDO5 output with a minimum of 4.7µF ceramic.
43	BYP3P3	Connect BYP3P3 to 3.3V buck output or external 3.3V source, this will allow IC to disable LDO3P3, then the power source will be drawn from BYP3P3 to minimize internal power dissipation. Tie to GND if not used.
44	MODE	Mode selection pin. Connect to logic high or VCC for PWM mode. Connect to logic low or ground for DCM mode. An internal 5MΩ pull-down resistor prevents undefined logic state in case of MODE pin float.
45	LDO3P3	3.3V linear regulator output. Power on or off by VIN. Can provide a total of 100mA external loads. Bypass LDO3P3 output with a minimum of 4.7µF ceramic.
46	PG1	Open drain power-good of SMPS1. Pulled to ground when output voltage is below regulation limits or during soft-start interval. Contains an internal 5MΩ pull-up resistor.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL95901IRZ	95901 IRZ	-40 to +85	46 Ld QFN	L46.5x6
ISL95901EVAL1Z	Evaluation Board			

NOTES:
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL95901. For more information on MSL please see Tech Brief TB363.
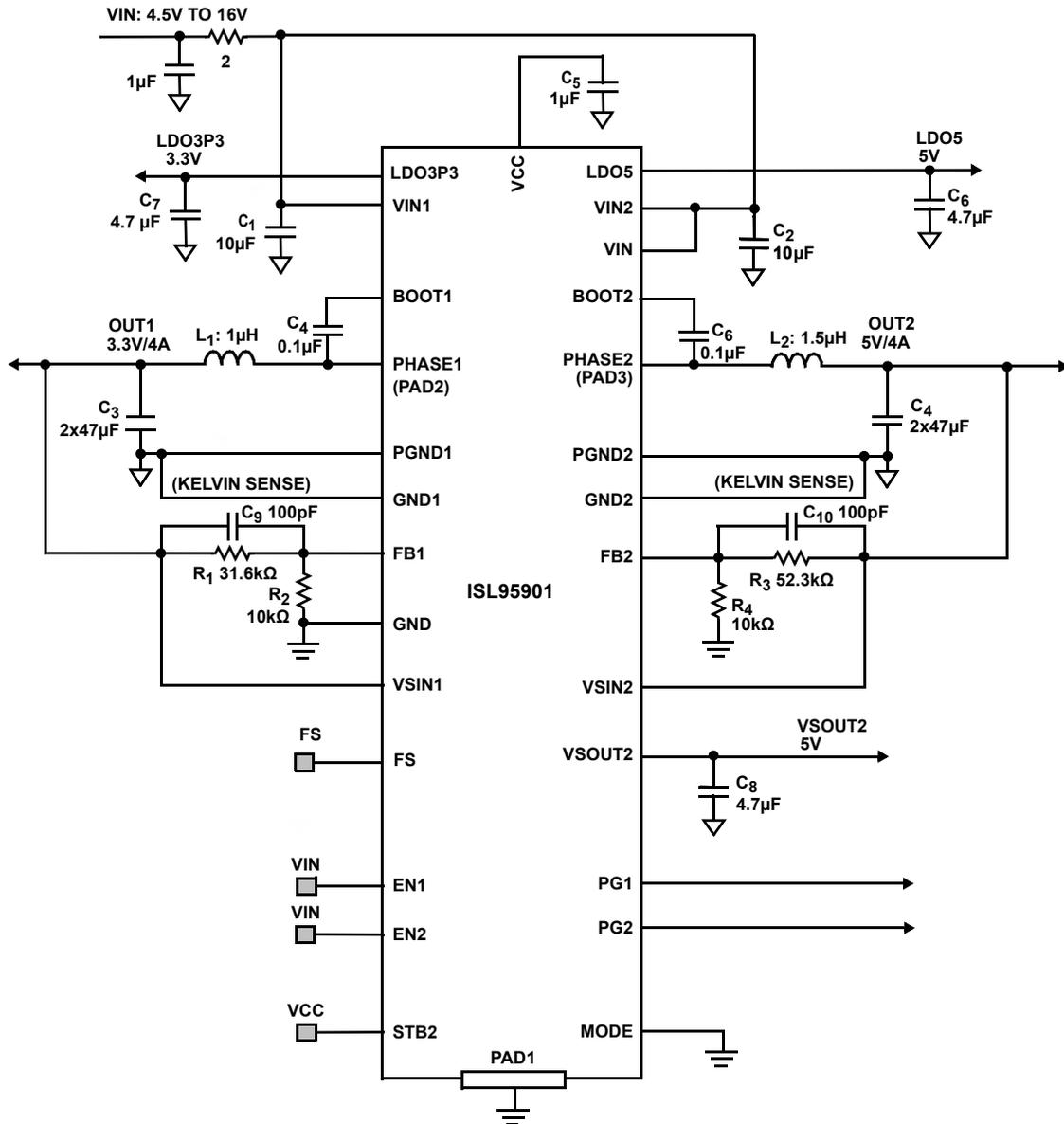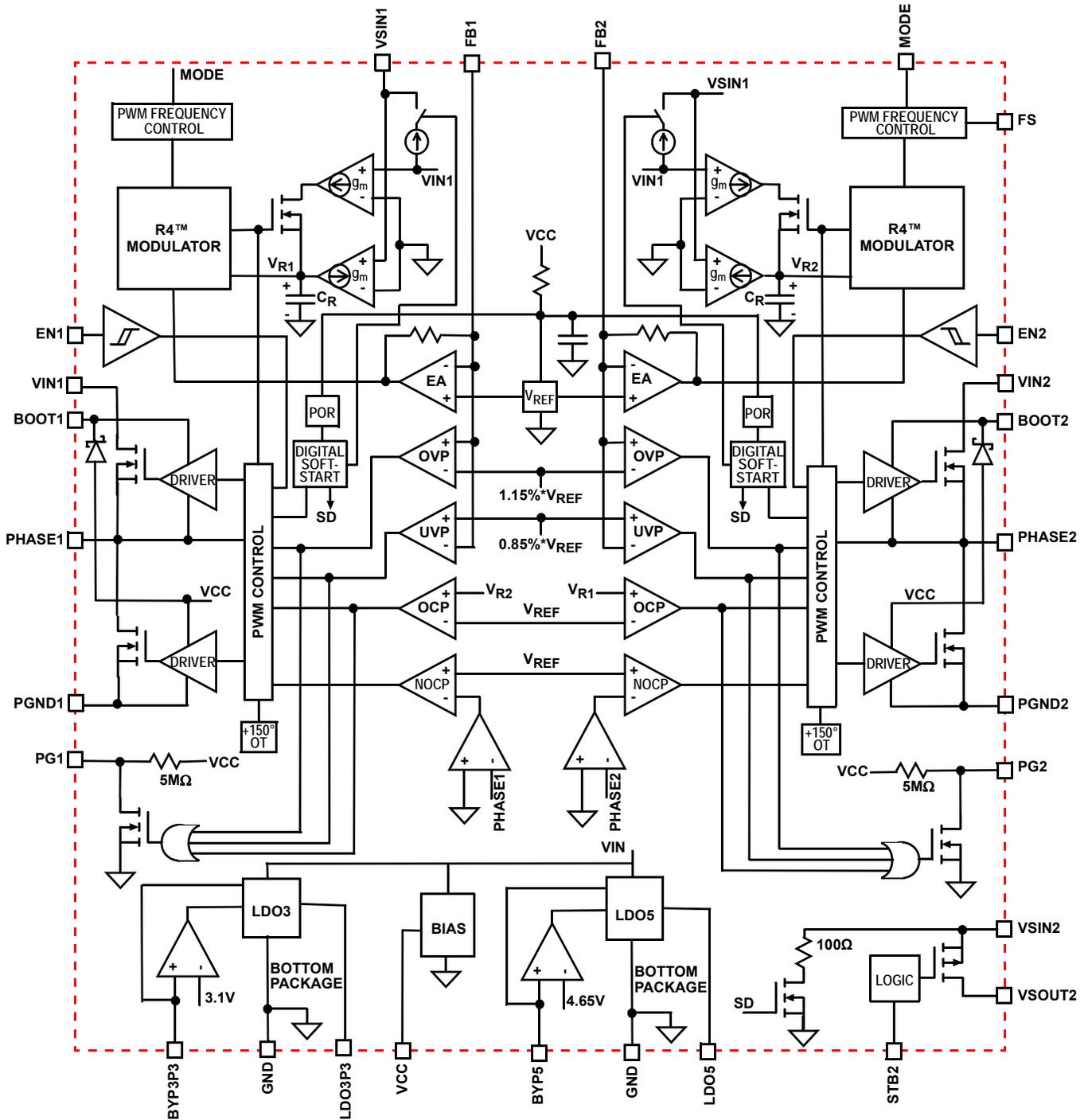
Typical Application Schematic

FIGURE 3. DUAL 4A OUTPUT AT 1MHz (V$_{IN}$ RANGE FROM 4.5V TO 16V)

Functional Block Diagram

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Absolute Maximum Ratings

VIN1/2, VIN to GND . . . . -0.3V to +17V
PHASE1/2 to PGND1/2. . . . . -0.3V to VIN1/2 + 0.3V(DC_) or
                                                                                    -2V to 19V (100ns)
BOOT1/2 to PHASE1/2 . . . . -0.3V to +5.9V
VSIN1/2, VSOUT2, to GND. . . . . -0.3V to VCC+0.3V
VCC to GND . . . . -0.3V to +5.9V
BYP5, LDO5 to GND . . . . -0.3V to VCC+0.3V
BYP3P3, LDO3P3 to GND . . . . -0.3V to VCC+0.3V
EN1/2 to GND. . . . . -0.3V to +17V
STB2, MODE, PG1/2, FS to GND. . . . . -0.3V to VCC+0.3V
FB1, FB2 to GND. . . . . -0.3V to +2.95V
ESD Rating
   Human Body Model (Tested per JESD22-A114) 2.5kV
   Charged Device Model (Tested per JESD22-C101E). 1.2kV
   Machine Model (Tested per JESD22-A115). 200V
Latch-up (Tested per JESD-78A; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance θ_{JA} (°C/W) θ_{JC} (°C/W)
   QFN Package ([Notes 4](#), [5](#)) 29.1   2
Maximum Junction Temperature (Plastic Package) . . . .+150°C
Maximum Storage Temperature Range . . . .-65°C to +150°C
Pb-Free Reflow Profile . . . . see [TB493](#)

Recommended Operating Conditions

Ambient Temperature Range . . . .-40°C to +85°C
Junction Temperature Range . . . .-40°C to +125°C
Supply Voltage . . . . .4.5V to 16V

CAUTION: *Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#) for details.

5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications V_{IN} = 4.5V to 16V, unless otherwise noted. Typical values are at T_J = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN ([Note 6](#))	TYP	MAX ([Note 6](#))	UNITS
SUPPLY VOLTAGE						
V_{IN} Voltage Range	V_{IN}		**4.5**		**16**	V
V_{IN} Quiescent Supply Current	I_Q	MODE = 0V, $I_{VSIN1/2}$ = 0A, I_{SOUT2} = 0A BYP5 = 5V		0.8		mA
		FB1/2 = 0.9V		1.2	**1.6**	mA
V_{IN} Shutdown Supply Current	I_{SD}	EN1/2 = 0V		120	**200**	µA
V_{CC} Voltage	V_{CC}	V_{IN} = 12V; I_{OUT} = 0mA, BYP5 = 0V, 6V < V_{IN} < 16V	**4.9**	5.25	**5.6**	V
LDO						
LDO5		V_{IN} = 12V, BYP5 = 0V, 0mA < ILDO5 < 100mA	**4.90**	5.0	**5.12**	V
LDO3P3		BYP3P3 = 0V, 0mA < ILDO3P3 < 100mA	**3.23**	3.32	**3.4**	V
LDO5/LDO3P3 Output Short Current	I_{OUTLDO}			150	**425**	mA
Reference Voltage	V_{REF}		**0.792**	0.8	**0.808**	V
BYP5 Threshold Voltage		Rising Edge		4.65	**4.75**	V
		Falling Edge	**4.40**	4.50		V
BYP3P3 Threshold Voltage		Rising Edge		3.1	**3.2**	V
		Falling Edge	**2.9**	3		V
BYP3P3 ON-resistance				2.2	4.2	Ω
BYP5 ON-resistance				1.2	2.2	Ω
POWER-ON RESET						
V_{CC} POR Threshold		Rising Edge		3.9	**4.25**	V
		Falling Edge	**3.25**	3.7		V
Soft-Start Ramp Time		EN1/2 = V_{IN}	**2**	3	**4**	ms

Electrical Specifications V_{IN} = 4.5V to 16V, unless otherwise noted. Typical values are at T_J = +25°C. **Boldface limits apply across the junction temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Switching Frequency	f_{SW}	FS = High	**0.8**	1.0	**1.2**	MHz
		FS = Float	**400**	500	**600**	kHz
		FS = GND	**240**	300	**360**	kHz
OUTPUT REGULATION						
FB1/2 Leakage Current			**-200**	1	**200**	nA
POWER-GOOD						
OVP PG1/2 Trip Level		Rise		115	**118**	%
		Fall	**108**	112		%
UVP PG1/2 Trip Level		Rise		90	**93**	%
		Fall	**83**	87		%
PG1/2 Propagation Delay				20		µs
PG1/2 Low Voltage		I_{SINK} = 3mA, PG1/2 = 0V		100	**300**	mV
PG1/2 Leakage Current		PG1/2 = 0V		1	**1.5**	µA
PG1/2 Leakage Current		PG1/2 = 5V		0.02	**0.6**	µA
ENABLE, MODE, STB2 and FS INPUT						
EN1/2, STB2 Leakage Current		EN1/2 = 0V/5V, STB2 = 0V/5V	**-0.2**	0.01	**0.2**	µA
MODE Leakage Current		MODE = 0V	**-0.2**	0.01	**0.2**	µA
		MODE = 5V	**0.8**	1	**1.2**	µA
EN1/2, MODE, STB2 Input Threshold Voltage		Low Level			**0.40**	V
		High Level	**1.40**			V
FS Voltage Threshold		Low Level	**0.84**	0.92	**1**	V
		Float Level	**1.14**	1.2	**1.26**	V
		High Level	**1.76**	1.81	**1.86**	V
FAULT PROTECTION						
Thermal Shutdown Temperature	T_{SD}	Rising Threshold		150		°C
	T_{HYS}	Hysteresis		20		°C
Overcurrent Protection Threshold		Valley $V_{IN1/2}$ to $I_{PHASE1/2}$ (6 cycles delay)	**4.8**	7.8	**12**	A
Zero Cross Threshold				350		mA
Negative Current Limit	INLIMIT	$I_{PHASE1/2}$ to PGND1/2	**-10.5**	-6.2	**-2.8**	A
Standby Overcurrent Protection Threshold		IVS_{OUT2}		2		A
POWER MOSFET						
Highside	R_{HDS}	$I_{PHASE1/2}$ = 100mA		41	**55**	mΩ
Lowside	R_{LDS}	$I_{PHASE1/2}$ = 100mA		9	**14**	mΩ
PHASE Leakage Current (Note 7)		EN1/2 = PHASE1/2 = 0V		0.01	**2.5**	µA
PHASE Rise Time (Note 7)	t_{RISE}	V_{IN} = 16V		10		ns
VS_{OUT2} Standby Power MOSFET		IVS_{OUT2} = 100mA, VS_{IN1} = 5V		70		mΩ

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

7. Care must be taken not to exceed the phase node max voltage rating.

Typical Performance Curves

Circuit of [Figure 3]. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5, I_{OUT1} = 4A, I_{OUT2} = 4A, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.
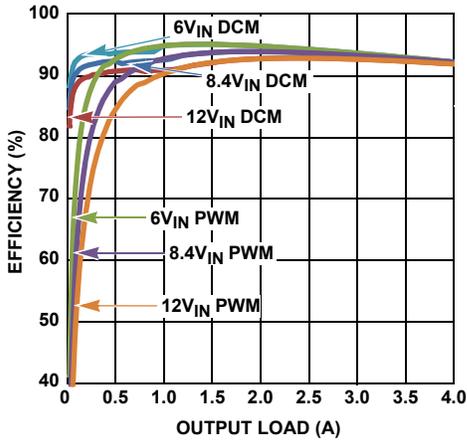
FIGURE 4. EFFICIENCY vs LOAD (300kHz, 3.3V$_{OUT}$)
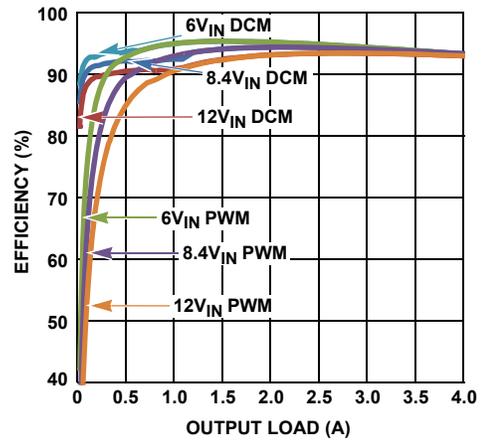
FIGURE 5. EFFICIENCY vs LOAD (500kHz, 3.3V$_{OUT}$)
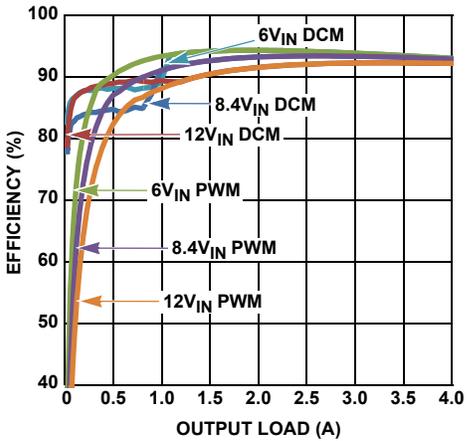
FIGURE 6. EFFICIENCY vs LOAD (1MHz, 3.3V$_{OUT}$)
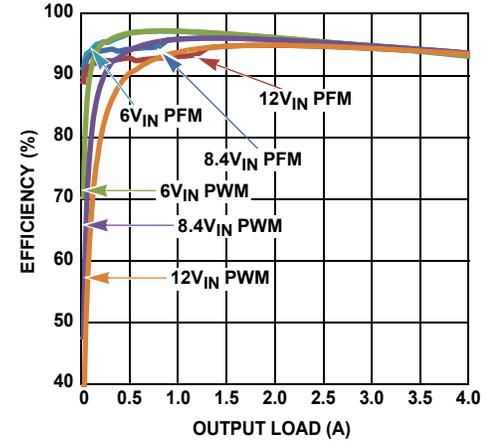
FIGURE 7. EFFICIENCY vs LOAD (300kHz, 5V$_{OUT}$)
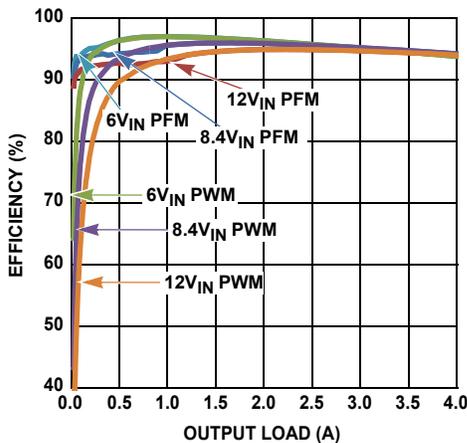
FIGURE 8. EFFICIENCY vs LOAD (500kHz, 5V$_{OUT}$)
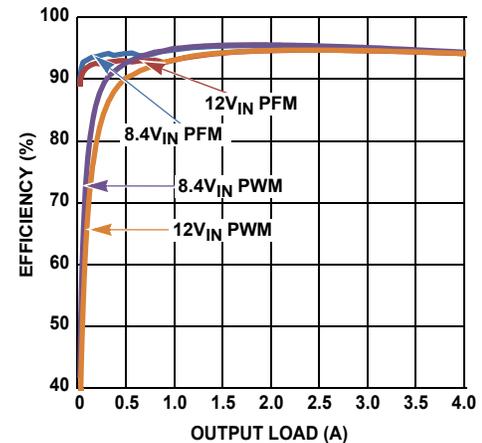
FIGURE 9. EFFICIENCY vs LOAD (1MHz, 5V$_{OUT}$)

Typical Performance Curves

Circuit of Figure 3. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5, I_{OUT1} = 4A, I_{OUT2} = 4A, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**
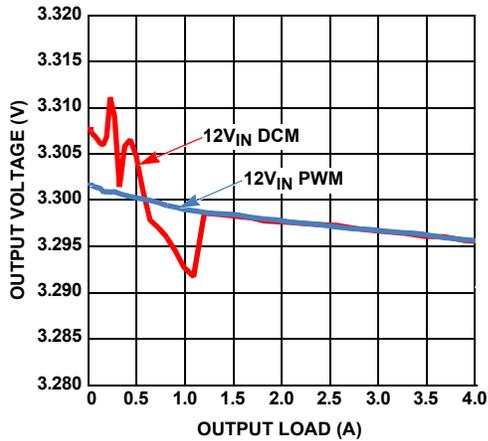
FIGURE 10. V_{OUT} REGULATION vs LOAD (300kHz 3.3V_{OUT})
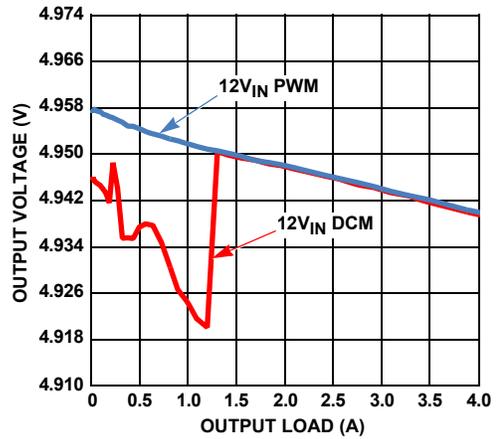
FIGURE 11. V_{OUT} REGULATION vs LOAD (300kHz 5V_{OUT})
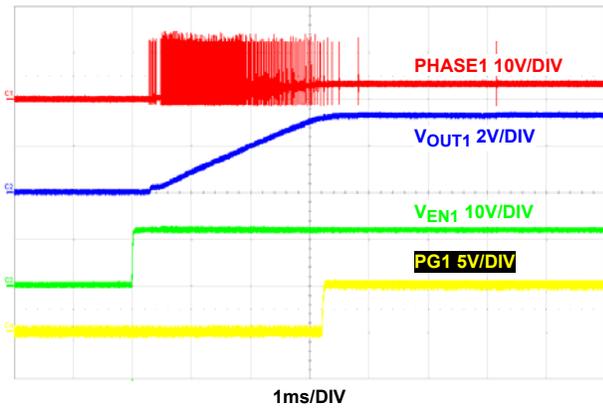
FIGURE 12. CH1 START-UP AT NO LOAD (PFM)
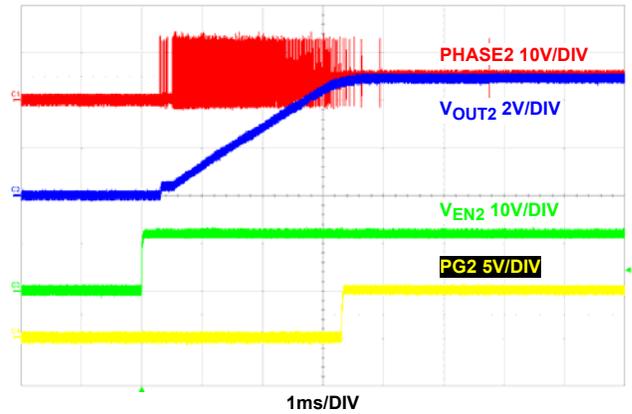
FIGURE 13. CH2 START-UP AT NO LOAD (PFM)
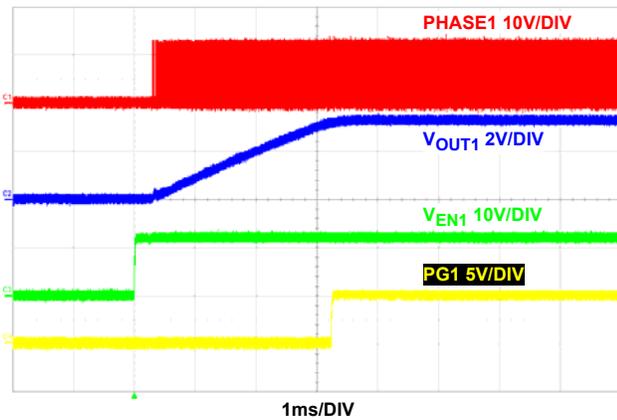
FIGURE 14. CH1 START-UP AT NO LOAD (PWM)
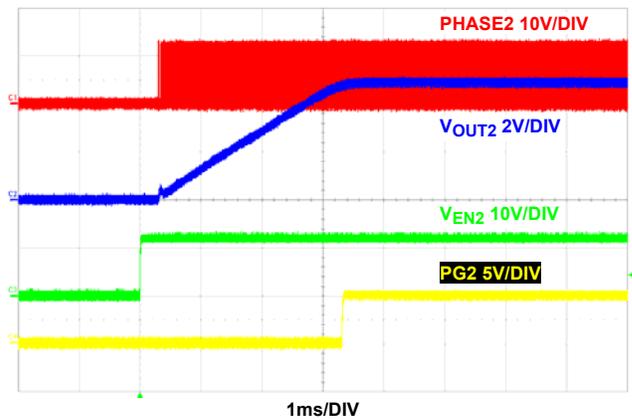
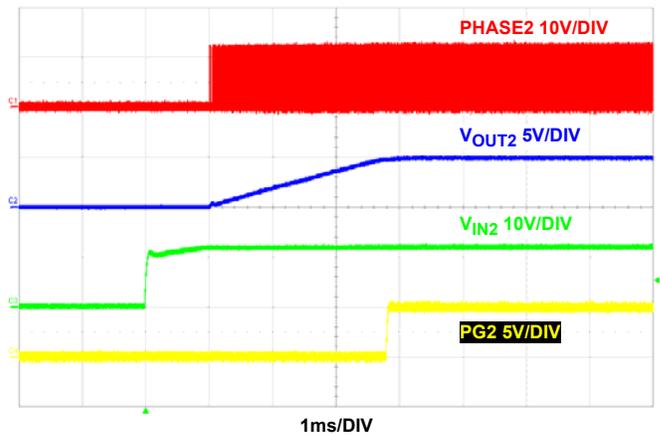FIGURE 15. CH2 START-UP AT NO LOAD (PWM)

Typical Performance Curves

Circuit of Figure 3. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5, I_{OUT1} = 4A, I_{OUT2} = 4A, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**
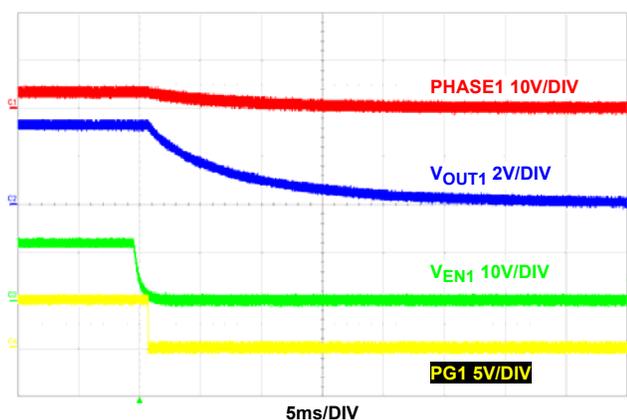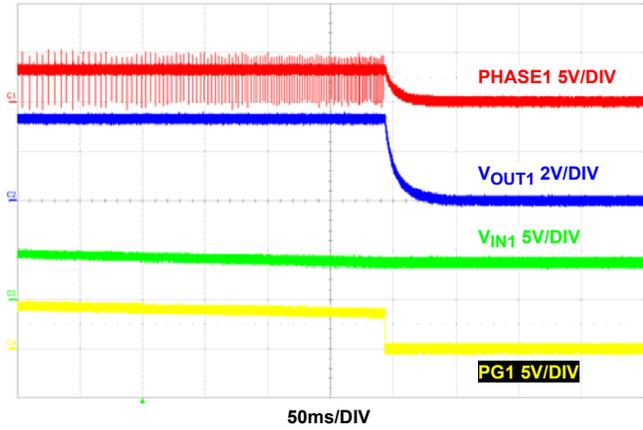

FIGURE 16. CH1 SHUTDOWN AT NO LOAD (PFM)
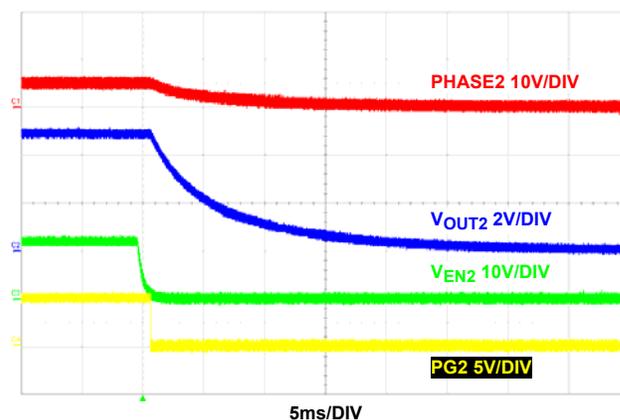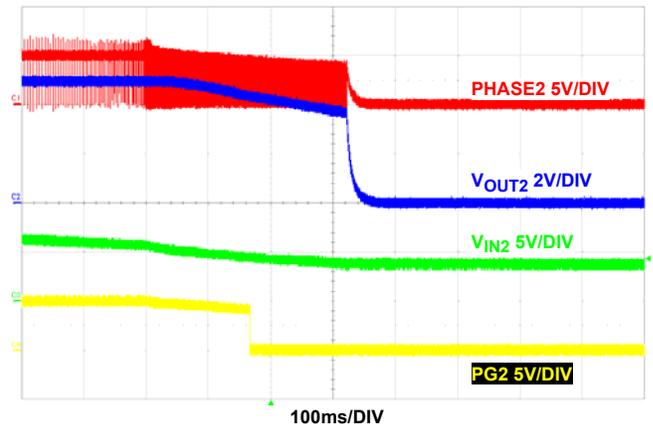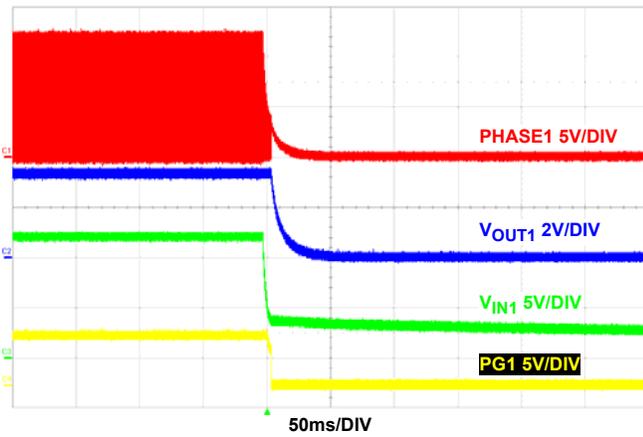

FIGURE 17. CH2 SHUTDOWN AT NO LOAD (PFM)
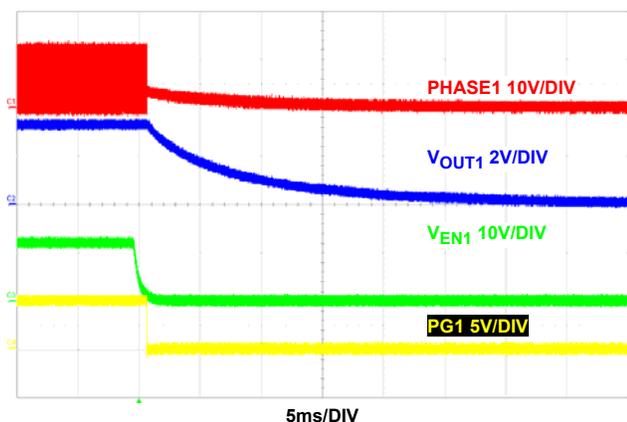
FIGURE 18. CH1 SHUTDOWN AT NO LOAD (PWM)
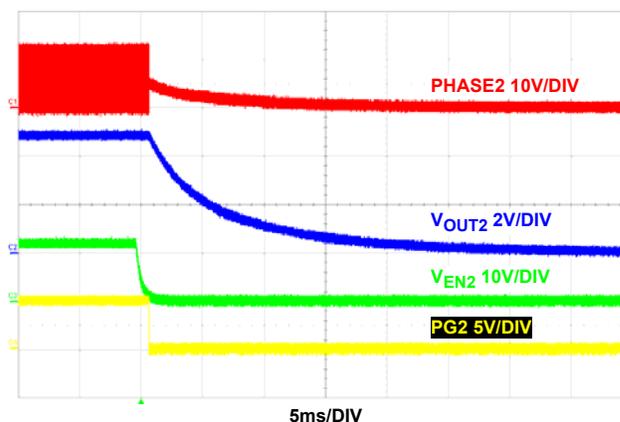
FIGURE 19. CH2 SHUTDOWN AT NO LOAD (PWM)
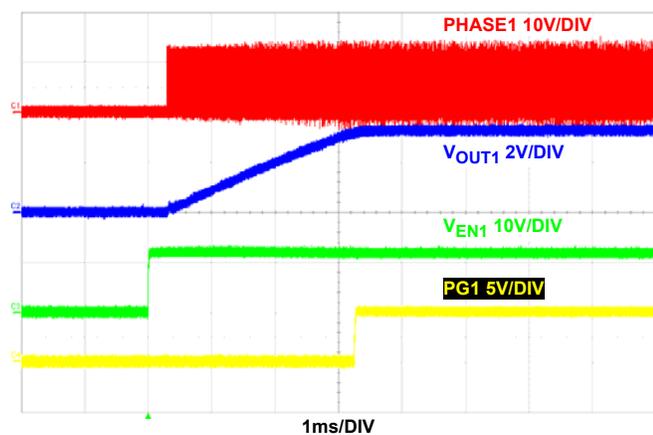
FIGURE 20. CH1 START-UP AT 4A LOAD (PWM)
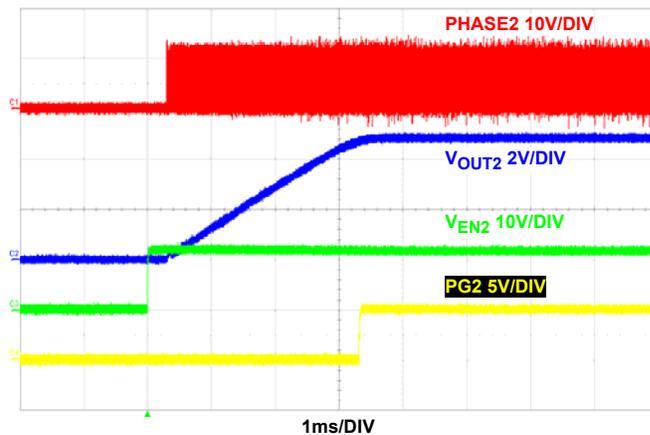
FIGURE 21. CH2 START-UP AT 4A LOAD (PWM)

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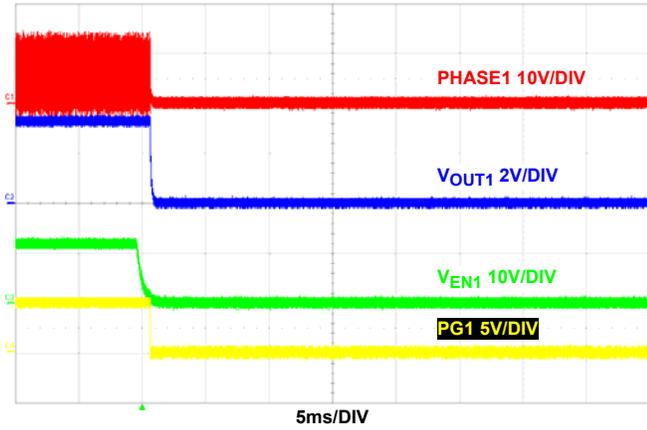
FIGURE 22. CH1 SHUTDOWN AT 4A LOAD (PWM)
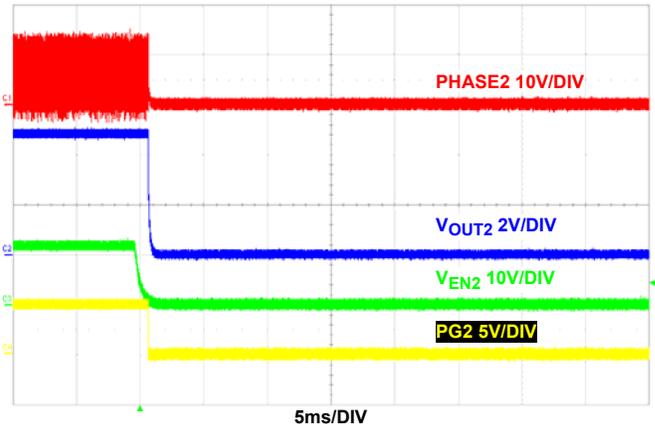
FIGURE 23. CH2 SHUTDOWN AT 4A LOAD (PWM)
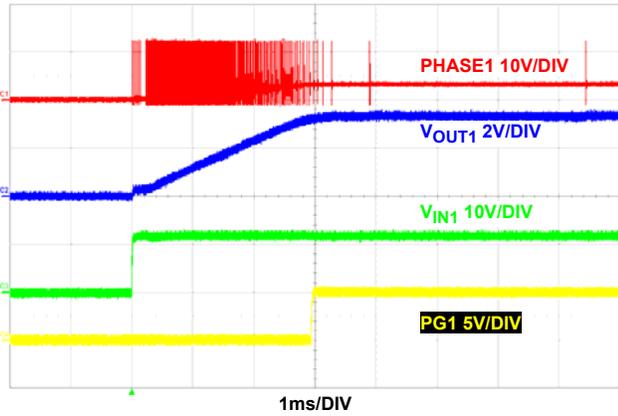
FIGURE 24. CH1 START-UP V_{IN} AT NO LOAD (PFM)
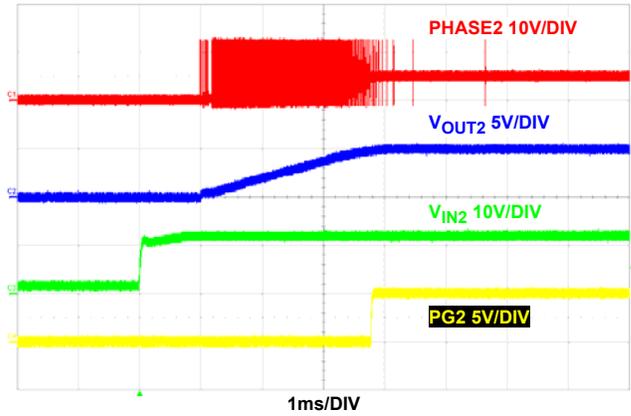
FIGURE 25. CH2 START-UP V_{IN} AT NO LOAD (PFM)
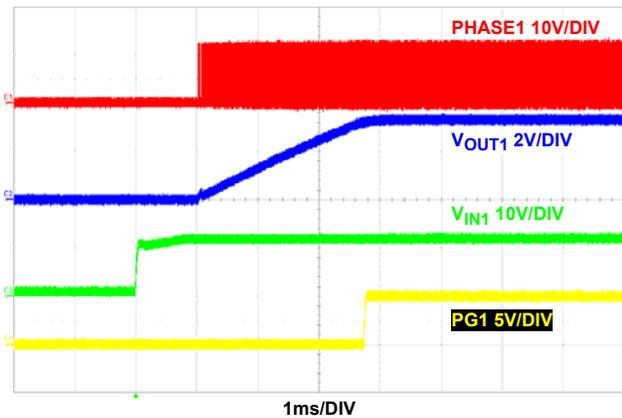
FIGURE 26. CH1 START-UP V_{IN} AT NO LOAD (PWM)

FIGURE 27. CH2 START-UP V_{IN} AT NO LOAD (PWM)

ISL95901

Typical Performance Curves   Circuit of Figure 3. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5, I_{OUT1} = 4A, I_{OUT2} = 4A, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

FIGURE 28. CH1 SHUTDOWN V_{IN} AT NO LOAD (PFM)

FIGURE 29. CH2 SHUTDOWN V_{IN} AT NO LOAD (PFM)

FIGURE 30. CH1 SHUTDOWN V_{IN} AT NO LOAD (PWM)
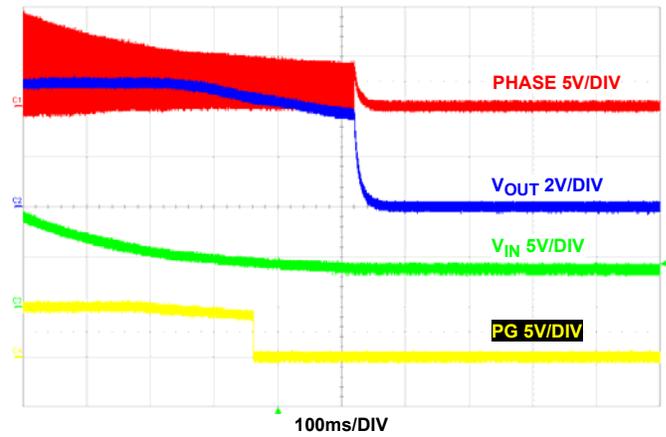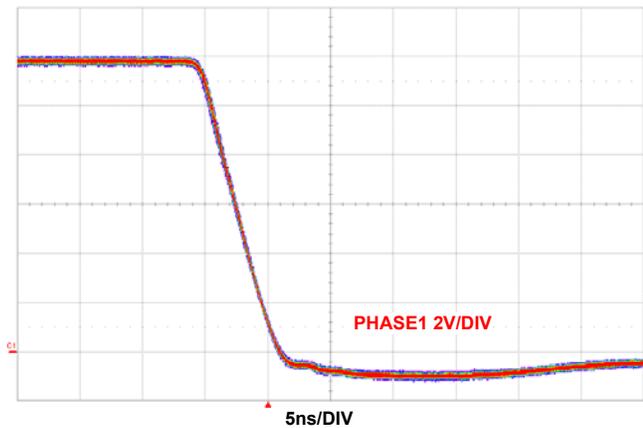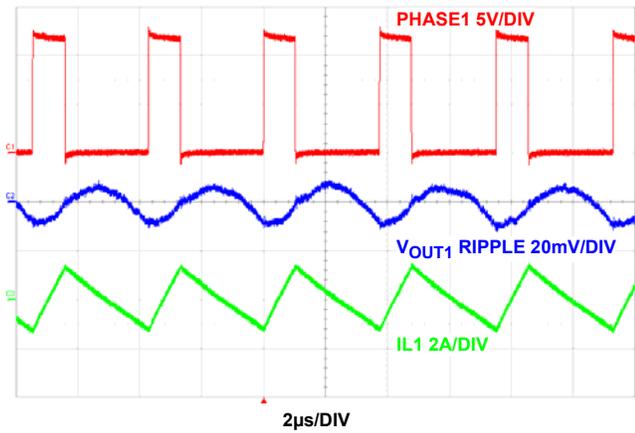

FIGURE 31. CH2 SHUTDOWN V_{IN} AT NO LOAD (PWM)

FIGURE 32. CH1 JITTER AT NO LOAD PWM
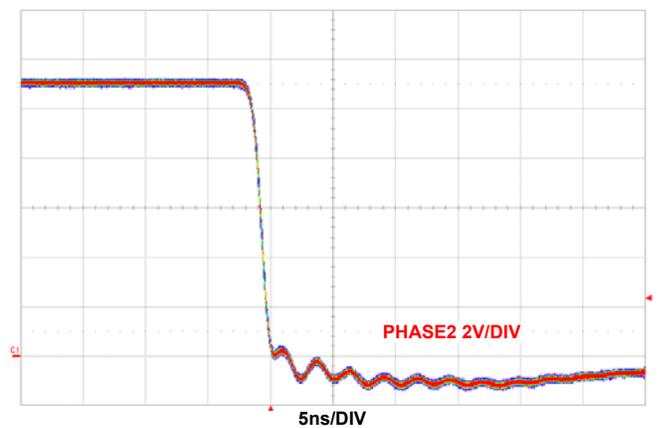
FIGURE 33. CH1 JITTER AT FULL LOAD PWM

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PHASE1 5V/DIV

V_{OUT1} RIPPLE 20mV/DIV

IL1 2A/DIV

2µs/DIV

FIGURE 34. CH1 STEADY STATE AT NO LOAD PWM

PHASE2 5V/DIV

V_{OUT2} RIPPLE 20mV/DIV

IL2 1A/DIV

2µs/DIV
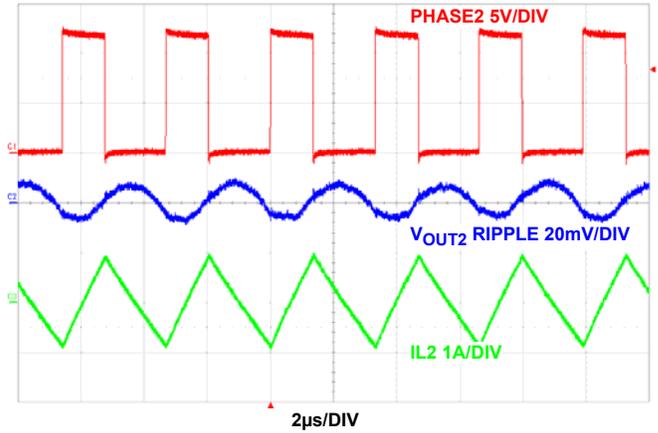
FIGURE 35. CH2 STEADY STATE AT NO LOAD PWM

PHASE1 5V/DIV

V_{OUT1} RIPPLE 50mV/DIV

IL1 2A/DIV

10ms/DIV
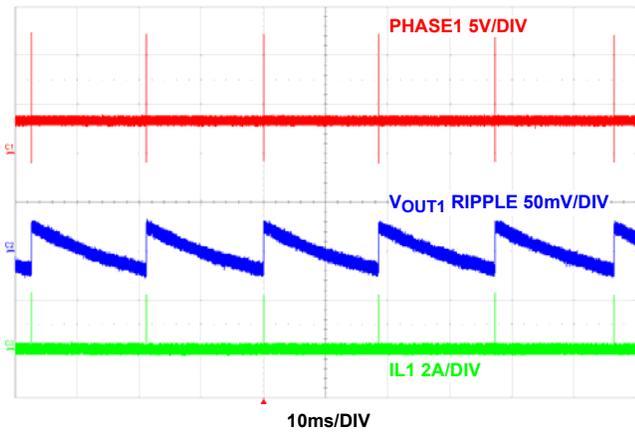
FIGURE 36. CH1 STEADY STATE AT NO LOAD PFM

PHASE2 5V/DIV

V_{OUT2} RIPPLE 50mV/DIV

IL2 1A/DIV

5ms/DIV
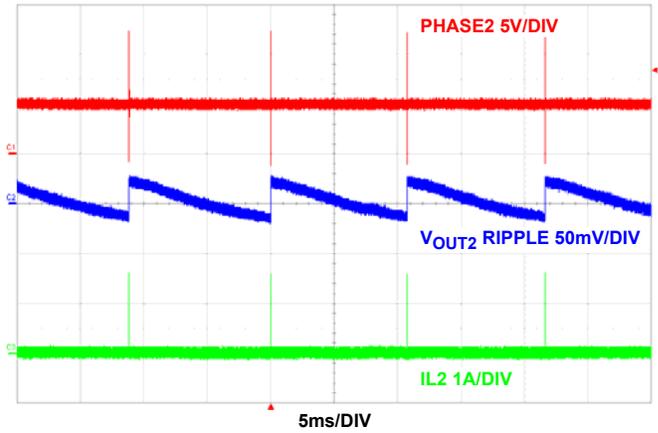
FIGURE 37. CH2 STEADY STATE AT NO LOAD PFM

PHASE1 5V/DIV

V_{OUT1} RIPPLE 50mV/DIV

IL2 2A/DIV

2µs/DIV
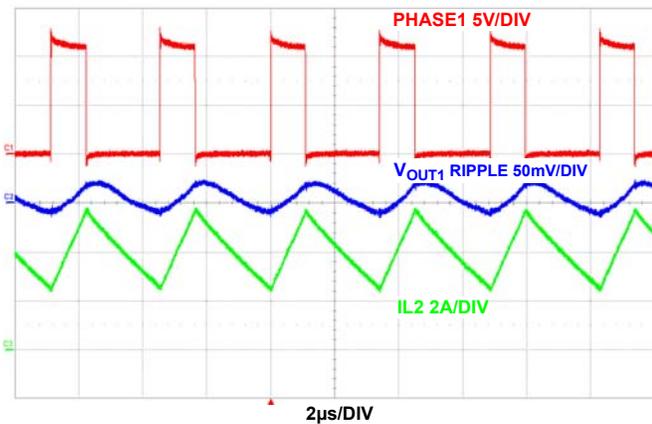
FIGURE 38. CH1 STEADY STATE AT 4A LOAD PWM

PHASE2 5V/DIV

V_{OUT2} RIPPLE 50mV/DIV

IL2 2A/DIV

2µs/DIV

FIGURE 39. CH2 STEADY STATE AT 4A LOAD PWM

ISL95901

Typical Performance Curves
Circuit of Figure 3. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5, I_{OUT1} = 4A, I_{OUT2} = 4A, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

FIGURE 40. STEADY STATE AT NO LOAD PWM ON BOTH CHANNELS
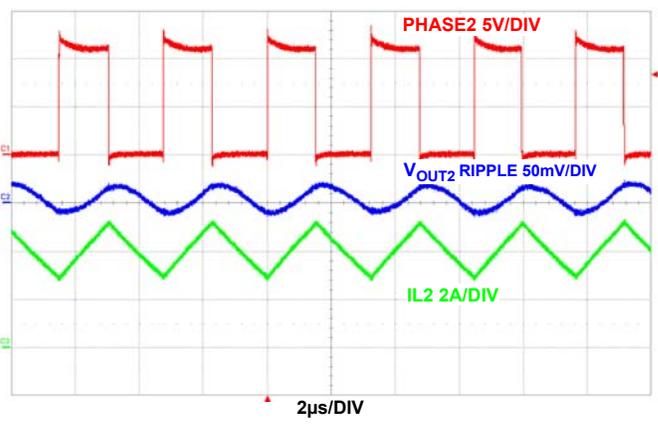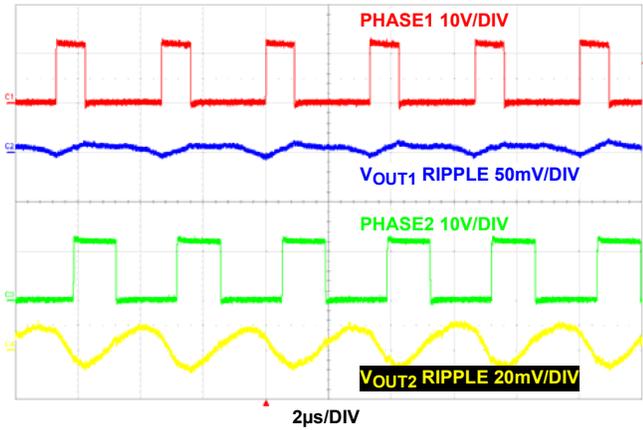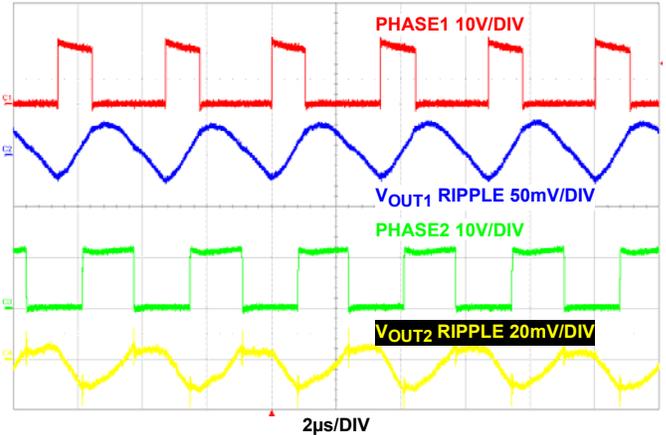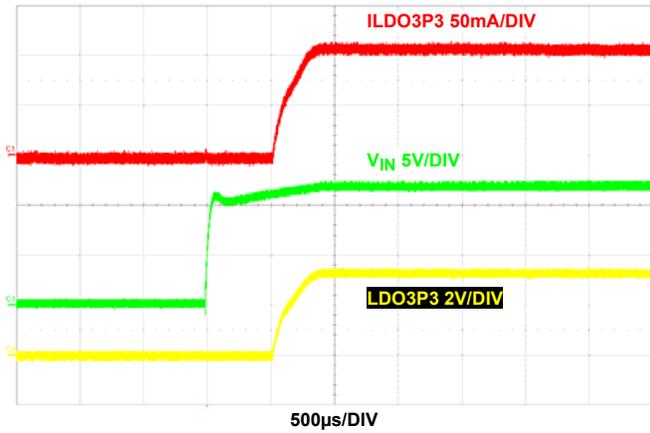

FIGURE 41. STEADY STATE AT 4A LOAD PWM ON BOTH CHANNELS
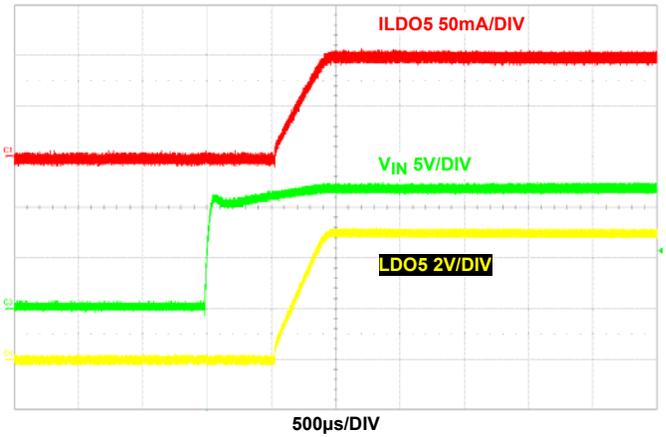

FIGURE 42. LDO3P3 START-UP V_{IN} AT 100mA

FIGURE 43. LDO5 START-UP V_{IN} AT 100mA
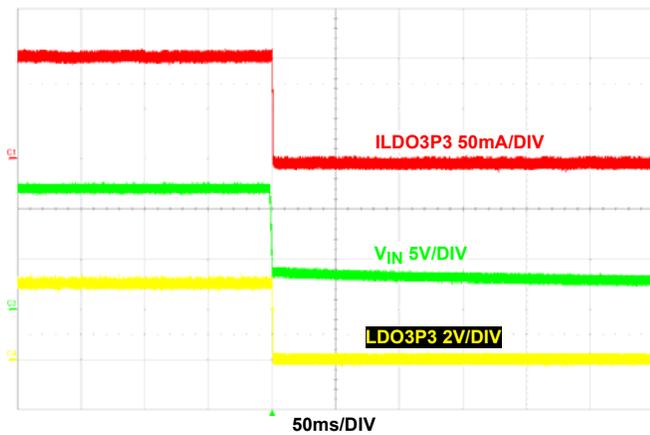

FIGURE 44. LDO3P3 SHUTDOWN V_{IN} AT 100mA
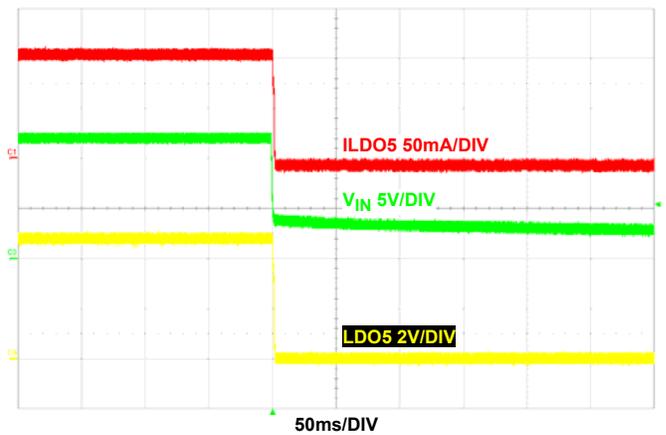
FIGURE 45. LDO5 SHUTDOWN V_{IN} AT 100mA

ISL95901

Typical Performance Curves Circuit of Figure 3. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5, I_{OUT1} = 4A, I_{OUT2} = 4A, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**
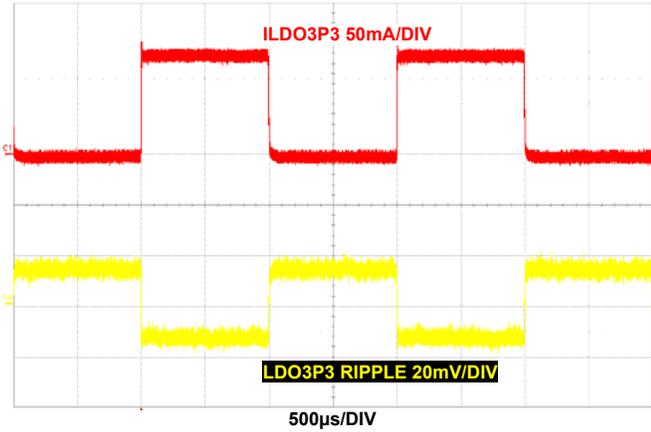
FIGURE 46. LDO3P3 LOAD TRANSIENT
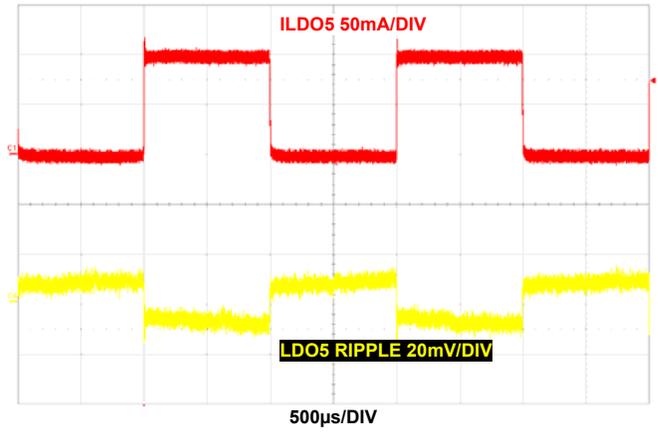
FIGURE 47. LDO5 LOAD TRANSIENT
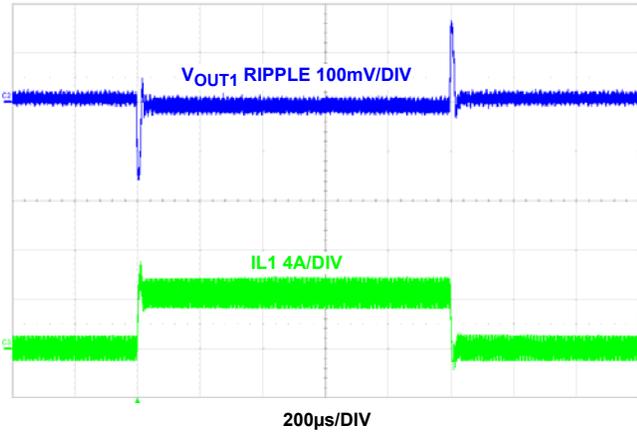
FIGURE 48. CH1 LOAD TRANSIENT (PWM)
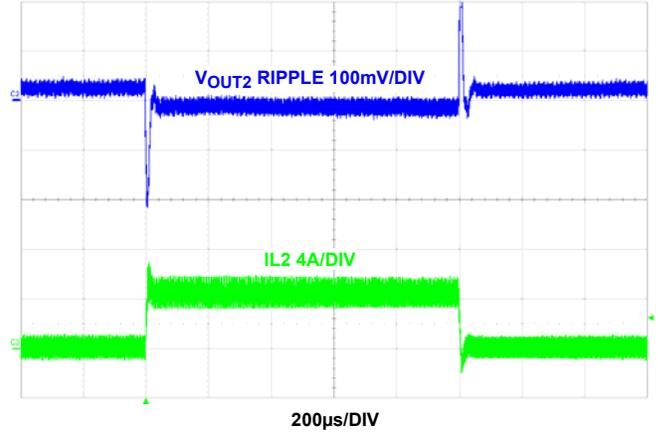
FIGURE 49. CH2 LOAD TRANSIENT (PWM)
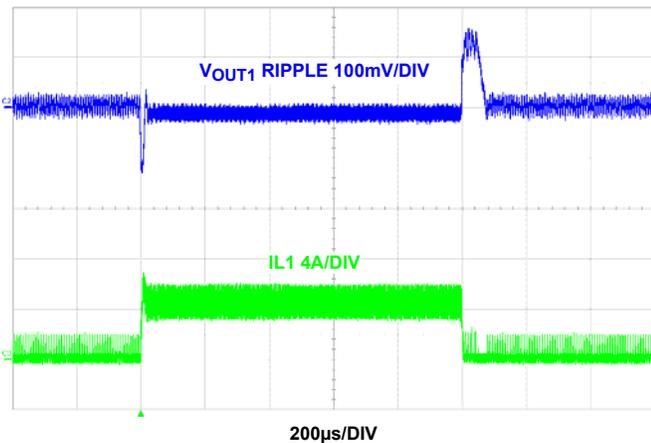
FIGURE 50. CH1 LOAD TRANSIENT (PFM)
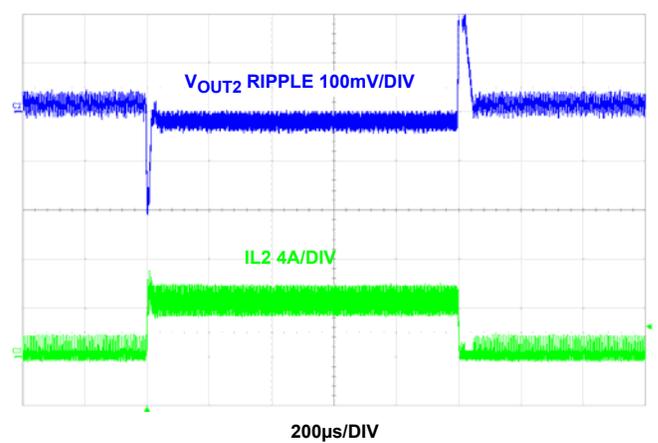
FIGURE 51. CH2 LOAD TRANSIENT (PFM)

ISL95901
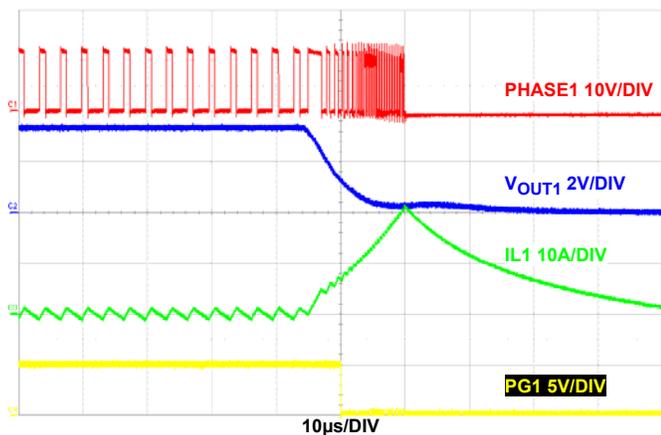
FIGURE 52. CH1 OUTPUT SHORT CIRCUIT
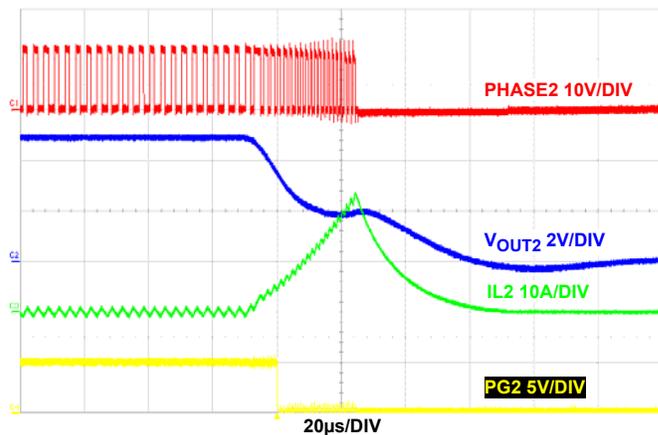
FIGURE 53. CH2 OUTPUT SHORT CIRCUIT
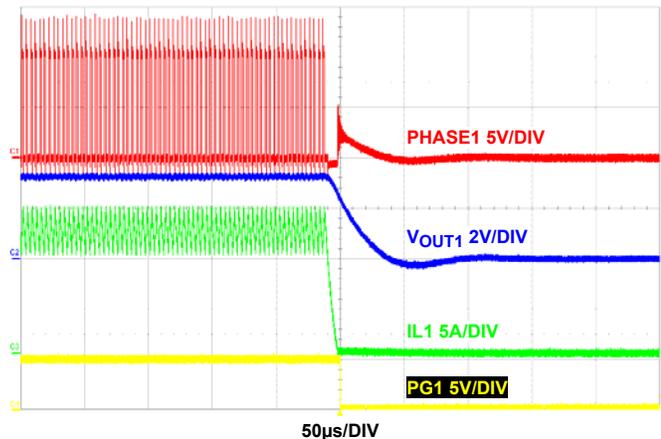
FIGURE 54. CH1 OCP
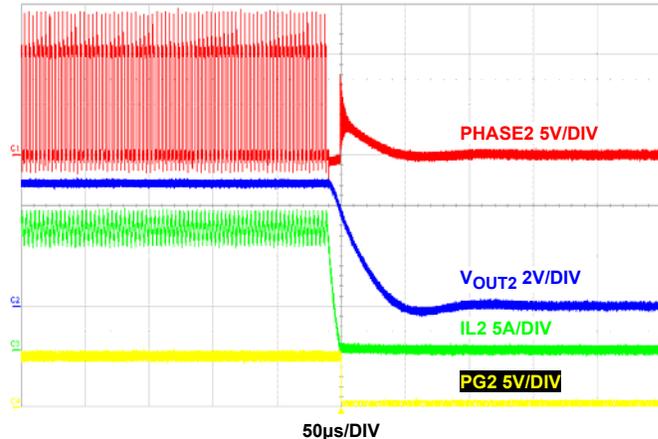
FIGURE 55. CH2 OCP
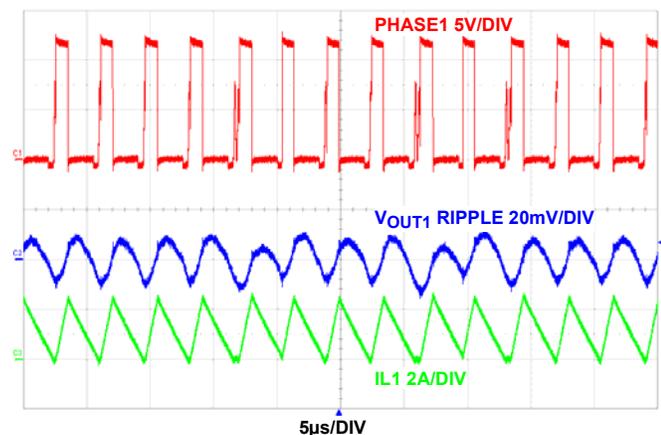
FIGURE 56. CH1 PFM TO PWM TRANSITION
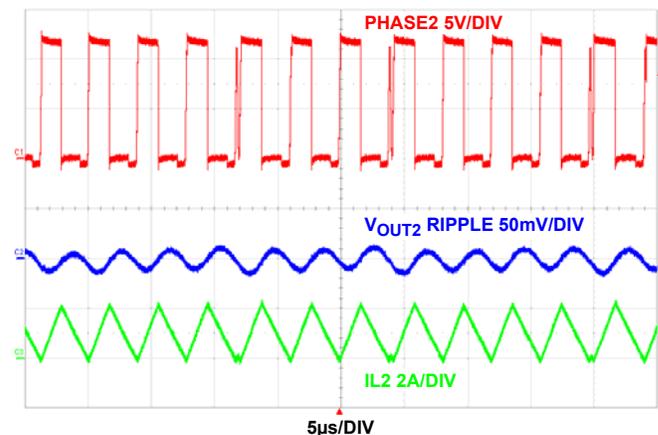
FIGURE 57. CH2 PFM TO PWM TRANSITION

ISL95901

Typical Performance Curves
Circuit of Figure 3. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5, I_{OUT1} = 4A, I_{OUT2} = 4A, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**
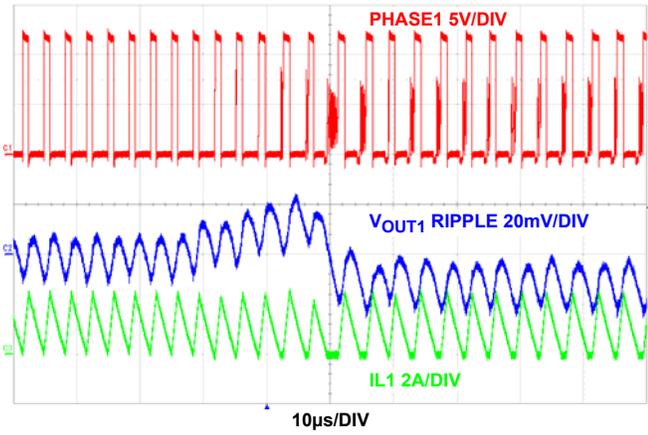
**FIGURE 58. CH1 PWM TO PFM TRANSITION**
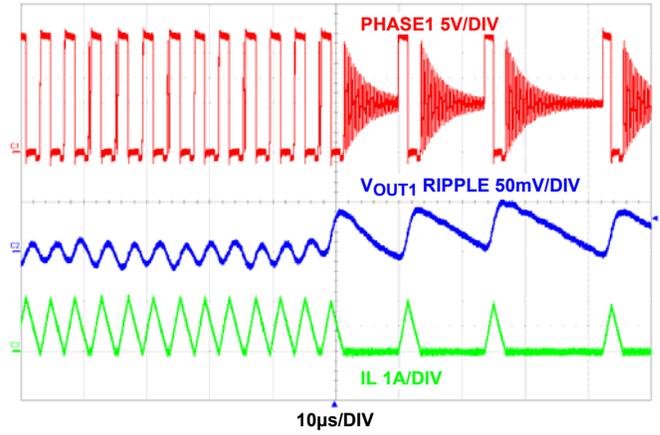
FIGURE 59. CH2 PWM TO PFM TRANSITION
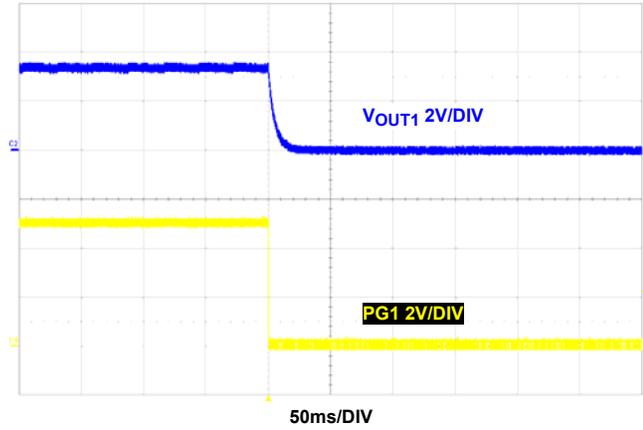
FIGURE 60. CH1 OTP

FIGURE 61. CH2 OTP

intersil
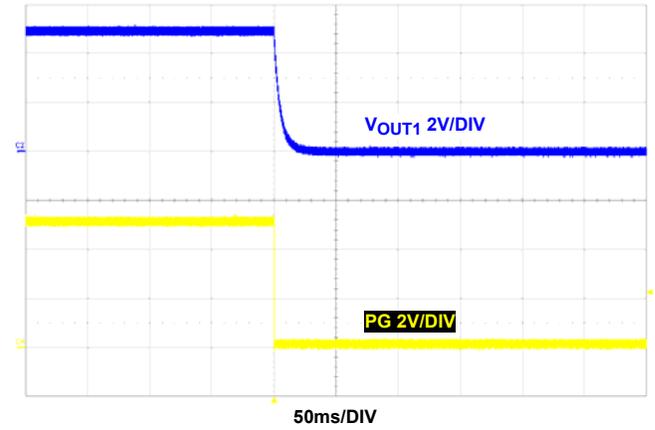
Detailed Description

The ISL95901 combines a dual PWM controller with two pairs of integrated switching MOSFETs. The synchronous controller drives the internal N-channel MOSFETs to deliver load current up to 4A per channel. The buck regulator can operate from an unregulated DC source such as a battery, with a voltage ranging from +4.5V to +16V. The converter output can be regulated to as low as 0.8V. These features make the ISL95901 ideally suited for FPGA, set-top boxes, LCD panels, DVD drives, netbook, laptop and wireless chipset power applications.

R4™ Modulator Technology

The ISL95901 modulator features Intersil R4™ Modulator Technology. The R4™ modulator is an evolutionary step in R3™ Technology. Like R3™, the R4™ Modulator allows variable frequency in response to load transients and maintains the benefits of current-mode hysteretic controllers. In addition, the R4™ Modulator reduces regulator output impedance and uses accurate referencing to eliminate the need for a high-gain voltage amplifier. The result is a topology that can be tuned to voltage-mode hysteretic transient speed while maintaining a linear control model and removing the need for any compensation. This greatly simplifies regulator design for customers and reduces external component count and cost.

R4™ Technology employs an innovative modulator that synthesizes an AC ripple voltage signal, V_R, analogous to the output inductor ripple current. The AC signal enters a window comparator where the lower threshold is the error amplifier output, V_{COMP} and the upper threshold is a programmable voltage reference, V_W, resulting in generation of the PWM signal. The voltage reference, V_W, sets the steady-state PWM frequency. Both edges of the PWM can be modulated in response to input voltage transients and output load transients much faster than conventional fixed-frequency PWM controllers. Unlike a conventional hysteretic converter, each channel of the ISL95901 has an error amplifier that provides ±1% voltage regulation at the FB pin.

To minimize solution size, the error amplifier internally integrates all necessary poles and zeroes, thus eliminating the need for compensation.

Stability

Removal of compensation derives from the R4™ Modulator's lack of need for high DC gain. In traditional architectures, high DC gain is achieved with an integrator in the voltage loop. The integrator introduces a pole in the open-loop transfer function at low frequencies. This pole, combined with the double-pole from the output L/C filter, creates a three-pole system that must be compensated to maintain stability.

Classic control theory requires a single-pole transition through unity gain to ensure a stable system. Current-mode architectures (includes peak, peak-through, current-mode hysteretic, R3™ and R4™) generate a zero at or near the L/C resonant point, effectively canceling one of the system's poles. The system still contains two poles, one of which must be cancelled with a zero before unity gain crossover to achieve stability. Compensation components are added to introduce the necessary zero.
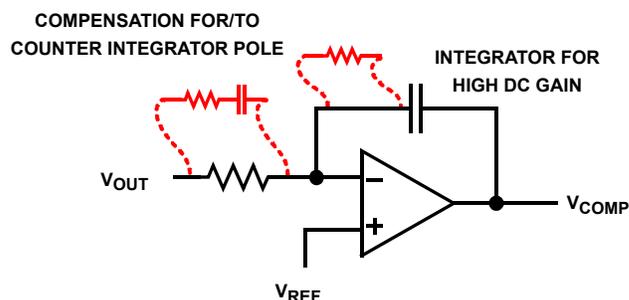
FIGURE 62. INTEGRATOR ERROR-AMPLIFIER CONFIGURATION

Figure 62 illustrates the classic integrator configuration for a voltage loop error-amplifier. While the integrator provides the high DC gain required for accurate regulation in traditional technologies, it also introduces a low-frequency pole into the control loop. Figure 63 shows the open-loop response that results from the addition of an integrating capacitor in the voltage loop. The compensation components found in Figure 62 are necessary to achieve stability.
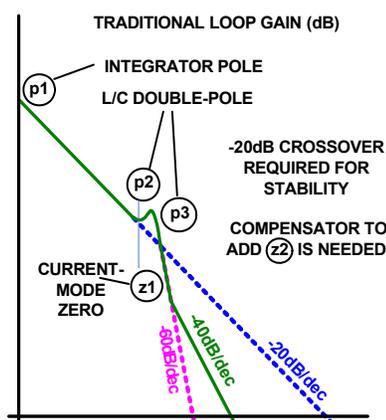
FIGURE 63. UNCOMPENSATED INTEGRATOR OPEN-LOOP RESPONSE

Because R4™ does not require a high-gain voltage loop, the integrator can be removed, reducing the number of inherent poles in the loop to two. The current-mode zero continues to cancel one of the poles, ensuring a single-pole crossover for a wide range of output filter choices. The result is a stable system with no need for compensation components or complex equations to properly tune the stability.

Figure 64 shows the R4™ error-amplifier that does not require an integrator for high DC gain to achieve accurate regulation. The result to the open loop response can be seen in Figure 65.
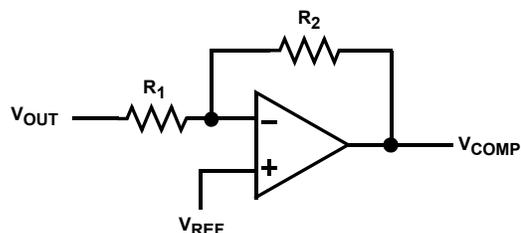
FIGURE 64. NON-INTEGRATED R4™ ERROR-AMPLIFIER CONFIGURATION
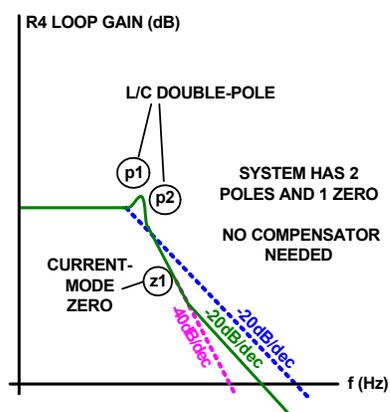
FIGURE 65. UNCOMPENSATED R4™ OPEN-LOOP RESPONSE

Transient Response

In addition to requiring a compensation zero, the integrator in traditional architectures slows system response to transient conditions. The change in COMP voltage is slow in response to a rapid change in output voltage. If the integrating capacitor is removed, COMP moves as quickly as V_{OUT} and the modulator immediately increases or decreases switching frequency to recover the output voltage.

The dotted red and blue lines in Figure 66 represent the time delayed behavior of V_{OUT} and V_{COMP} in response to a load transient when an integrator is used. The solid red and blue lines illustrate the increased response of R4™ in the absence of the integrator capacitor.
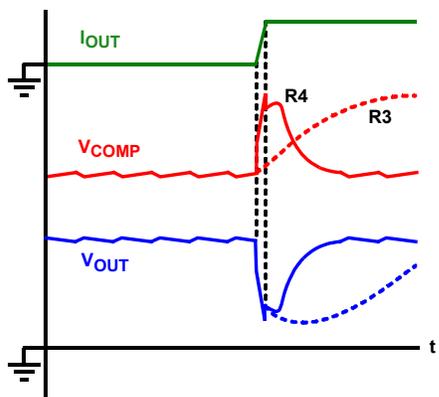
FIGURE 66. R3™ vs R4™ IDEALIZED TRANSIENT RESPONSE

Discontinuous Conduction Modes

The ISL95901 supports two power-saving modes of operation during light load conditions. If MODE is asserted HIGH, the regulator remains in continuous conduction mode (CCM), which offers the best transient response and the most stable operating frequency.

If the MODE pin is pulled to ground potential, the regulator operates in full discontinuous conduction mode (DCM). In this mode, the inductor current is monitored and is prohibited from going negative. When the inductor current reaches zero, both internal power MOSFETs are turned off. The output voltage then

decays solely as a function of load. The power FETs remain off until the output voltage droops enough to trigger a PWM on pulse. Because the rate of decay of V_{OUT} scales proportionally with load, so does the switching frequency. This increases efficiency as the relatively fixed power loss associated with switching the power FETs is averaged over the switching period.

Like R3™, the R4™ architecture seamlessly enters and exits all power saving modes to ensure accurate regulation.

Operation Initialization

The power-on reset circuitry and enable inputs prevent false start-up of the PWM regulator output. When all input criteria are met, the controller soft-starts the output voltage to the programmed level.

Power-on Reset

The ISL95901 automatically initializes upon receipt of input power supply. The power-on reset (POR) function continuously monitors VCC voltage. While below the POR threshold, the controller inhibits switching of the internal power MOSFET. When exceeded, the controller initializes the internal soft-start circuitry. If VCC supply drops below its falling POR threshold during soft-start or operation, the buck regulator is disabled until the input voltage returns.

Enable and Disable

When EN1/2 are pulled low, the device enters shutdown mode, and the supply current drops to a typical value of 120µA. All internal power devices are held in a high-impedance state while in shutdown mode.

The EN pin enables the ISL95901 controller. When the voltage on the EN pin exceeds its logic rising threshold, the controller initiates the 2ms soft-start function for the regulator. If the voltage on the EN pin drops below the falling threshold, the buck regulator shuts down.

Discharge Mode (Soft-stop)

When a transition to shutdown mode occurs or when the VCC POR is set, the outputs discharge to GND through an internal 50Ω switch.

Power-good

PG1/2 are the open-drain outputs of a window comparator that continuously monitors the buck regulator output voltage via the FB1/2 pin. PG1/2 is actively held low when EN1/2 is low and during the buck regulator soft-start period. After the soft-start period terminates, PG becomes high impedance as long as the output voltage (monitored on the FB1/2 pin) is between 90% and 105% of the nominal regulation voltage set by FB1/2. When V_{OUT} drops 10% below the nominal regulation voltage, the ISL95901 pulls PG1/2 low. Any fault condition forces PG1/2 low until the fault condition is cleared by attempts to soft-start. There is an internal 5MΩ internal pull-up resistor tied to PG1/2.

Output Voltage Selection

The regulator output voltage is easily programmed using an external resistor divider to scale VSIN1/2 relative to the internal reference voltage. The scaled voltage is applied to the inverting input of the error amplifier (see Figure 67).

The output voltage programming resistor, R_2, depends on the value chosen for the feedback resistor, R_3, and the desired output voltage, VSIN1/2, of the regulator. Equation 1 describes the relationship between resistor values. R_3 is often chosen to be in the 10kΩ to 100kΩ range.

$$R_2 = (VSIN1/2\text{-}0.8) \bullet R_3 / 0.8 \qquad \text{(EQ. 1)}$$

If the desired output voltage is 0.8V, then R_3 is left unpopulated, and R_2 is 0Ω.
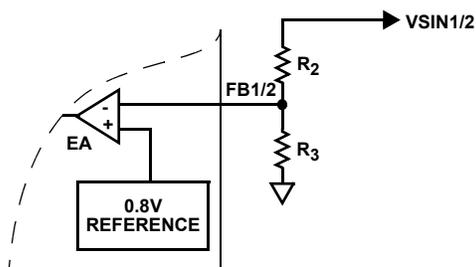

FIGURE 67. EXTERNAL RESISTOR DIVIDER

Protection Features

The ISL95901 limits the current in all on-chip power devices. Overcurrent protection limits the current on the LDO5, LDO3P3, V_{CC}, the two buck regulators and the standby outputs.

Buck Regulator Overcurrent Protection

If the current draw from the load becomes too high during operation, the IC protects itself and the load by latching off. The overcurrent mechanism is implemented as a two-fold protection scheme.

The ISL95901 continuously monitors the lower N-channel MOSFET current. It stores the valley of the inductor current each cycle and compares it against the lower overcurrent protection (OCP) threshold of 7.8A nominally. If the OCP threshold is achieved for 6 consecutive PWM cycles, an overcurrent fault is detected and buck is latched off. In this event, the power-good monitor flags PG1/2 low and the high-side switching power MOSFET is turned off. Inductor valley current is used to ensure the minimum OCP threshold is above the ISL95901 normal maximum load of 4A, regardless of chosen inductor value, the IC remains latched off until POR or EN1/2 is toggled.

Buck Negative Current Protection

Similar to overcurrent protection, negative current protection is realized by monitoring the current across the low-side N-FET, as shown in . When the valley point of the inductor current reaches -6.2A, both P-FET and N-FET are off. Boot undervoltage engages when the condition exists for a long time and the voltage difference between BOOT and PHASE drops below 2.5V. The buck controller begins to switch again when output is back to regulation.

Standby Output Overcurrent Protection

The standby output (VSOUT2) current limit is 2A. Upon reaching these threshold, the internal MOSFET is latched off to prevent damage. Toggle EN2 or STB2 to reset faulty condition.

Thermal Overload Protection

Thermal overload protection limits maximum junction temperature in the ISL95901. When the junction temperature (T_J) exceeds +150°C, a thermal sensor sends a signal to the fault monitor.

The fault monitor commands the buck regulator and LDOs to shutdown. When the junction temperature has decreased by +20°C, the regulators and LDOs attempt a normal soft-start sequence and returns to normal operation. For continuous operation, the +125°C junction temperature rating should not be exceeded.

BOOT Undervoltage Protection

If the BOOT capacitor voltage falls below 2.5V, the BOOT undervoltage protection circuit pulls the phase pin low for 400ns to recharge the capacitor. This operation may arise during long periods of no switching, as in no-load situations at PFM.

Application Guidelines

Output Inductor Selection

The inductor value determines the converter's ripple current. Choosing an inductor current requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% of total load current. The inductor value can then be calculated using Equation 2:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \qquad \text{(EQ. 2)}$$

Increasing the value of inductance reduces the ripple current and thus ripple voltage. However, the larger inductance value may reduce the converter's response time to a load transient. The inductor current rating should be such that it does not saturate in overcurrent conditions.

Buck Regulator Output Capacitor Selection

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are two critical factors when considering output capacitance choice. The current mode control loop allows low ESR ceramic capacitors to be used and results in smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturer data sheet to determine actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction generally suffices. The result of these considerations can easily result in an effective capacitance that is 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

The following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For ceramic capacitors (low ESR) (Equation 3):

$$V_{OUTripple} = \frac{\Delta I}{8*f_{SW}*C_{OUT}}$$ (EQ. 3)

where ΔI is the inductor's peak-to-peak ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitor.

If using electrolytic capacitors (Equation 4):

$$V_{OUTripple} = \Delta I*ESR$$ (EQ. 4)

Input Capacitor Selection

To reduce the resulting input voltage ripple and to minimize EMI by forcing the very high frequency switching current into a tight local loop, an input capacitor is required. The input capacitor must have an adequate ripple current rating, which can be approximated by the Equation 5.

$$\frac{I_{RMS}}{I_O} = \sqrt{D - D^2}$$ (EQ. 5)

where $D = V_O/V_{IN}$

If capacitors other than MLCC are used, attention must be paid to ripple and surge current ratings.

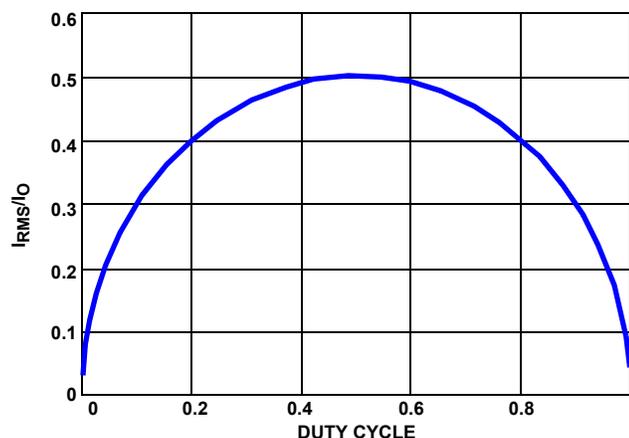The input ripple current is graphically represented in Figure 68 for each SMPS.

FIGURE 68. I_{RMS}/I_O vs DUTY CYCLE

A minimum of 10µF ceramic capacitance is required on each VIN pin. The capacitors must be as close to the IC as physically possible. Additional capacitance may be used.

Power Derating Characteristics

To prevent the ISL95901 from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 6:

$$T_{RISE} = (PD)(\theta_{JA})$$ (EQ. 6)

Where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by Equation 7:

$$T_J = (T_A + T_{RISE})$$ (EQ. 7)

where T_A is the ambient temperature. For the QFN package, θ_{JA} is +29°C/W.

The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C.

The ISL95901 outputs current level depends on whether the thermal impedance from the thermal pad maintains the junction temperature below +125°C. This depends on the input voltage/output voltage combination and the switching frequency. The device power dissipation must be reduced otherwise, thermal shutdown will occur.

Layout Considerations

Layout is very important in high frequency switching converter design. With power devices switching efficiently between 100kHz and 2MHz, the resulting current transitions from one device to another cause voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit board design minimize these voltage spikes.

As an example, consider the turn-off transition of the upper MOSFET. Prior to turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is picked up by the body diode of the low-side MOSFET. Any parasitic inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection; tight layout of the critical components; and short, wide traces minimize the magnitude of voltage spikes.

There are two sets of critical components in the ISL95901 switching converter. The switching components are the most critical because they switch large amounts of energy and therefore tend to generate large amounts of noise. Next, are the small signal components, which connect to sensitive nodes or supply critical bypass current and signal coupling.

A multi-layer printed circuit board is recommended. Figure 64 shows the connections of the critical components in the converter. Note that capacitors C_{IN} and C_{OUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually a middle layer of the PC board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminals to the output inductor short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

To dissipate heat generated by the internal LDO and MOSFET, the pads should be connected to the PCB planes through at least eight vias. These allow heat to move away from the IC and also tie PAD1 to the ground plane through a low impedance path.

The switching components should be placed close to the ISL95901 first. Minimize the length of connections between the input capacitors, C_{IN}, and the power switches by placing them nearby. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible. Position the output inductor and output capacitors between PHASE1 (or PHASE2) and the load.

The critical small-signal components include any bypass capacitors, feedback components and compensation components. Feedback resistors should be located as close as possible to the FB pins with vias tied straight to the ground plane as required.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
January 22, 2015	FN7893.1	Updated datasheet by changing the continuous output current from 6A to 4A throughout document. Added Eval board to ordering information table on page 4. Updated datasheet with all Intersil standards.
Dec. 17, 2014	FN7893.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

L46.5x6

46 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 6/11

TOP VIEW

5.00

6.00

6̸

PIN 1
INDEX AREA

A

B

(4X) ⌒ 0.15

BOTTOM VIEW

3.50

3.60

42x 0.40

1.275

2.85

0.60

4.50

6̸

PIN #1 INDEX AREA

46x 0.40

2x 1.575

3.50

b

46X0.20 ⊕ 0.10 Ⓜ C A B

TYPICAL RECOMMENDED LAND PATTERN

3.50
(4.80)
(3.60)

(5.80)
(4.50)

1.275

0.60

2.85

(42X 0.40)

(46X 0.20)

(46X 0.60)

2x 1.575

3.50

SIDE VIEW

0.70

0.90±0.1

0.203 ⊢ 0.035

SEE DETAIL "X"

// 0.10 C

BASE PLANE C
SEATING PLANE
⌒ 0.08 C

DETAIL "X"

C ⌐ 0.2 REF

5̸

0.00 MIN
0.05 MAX
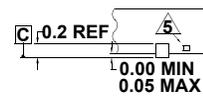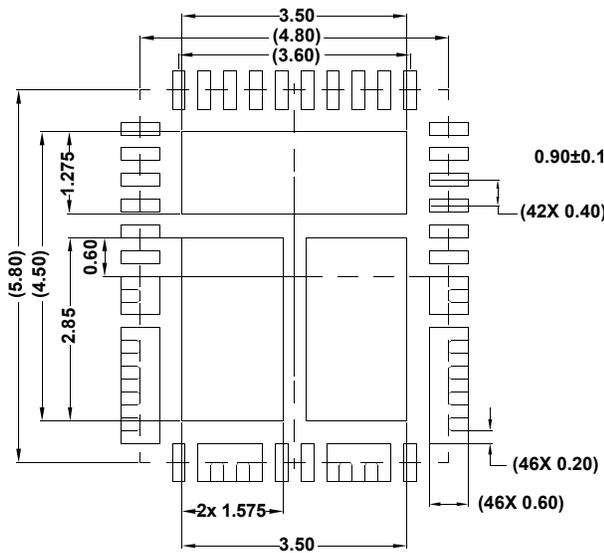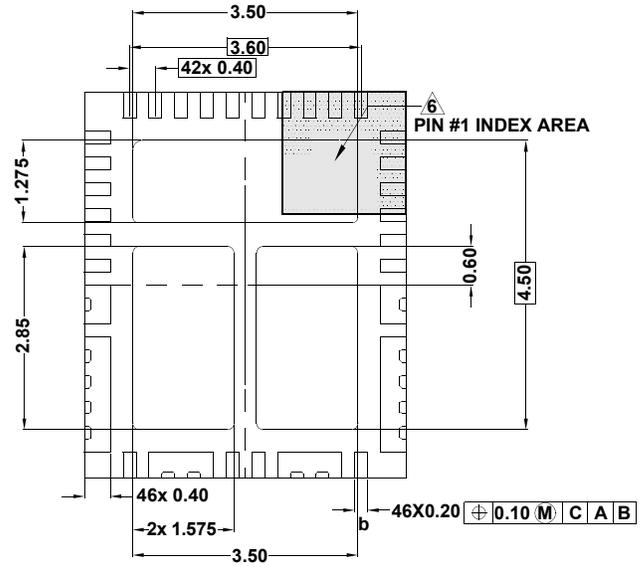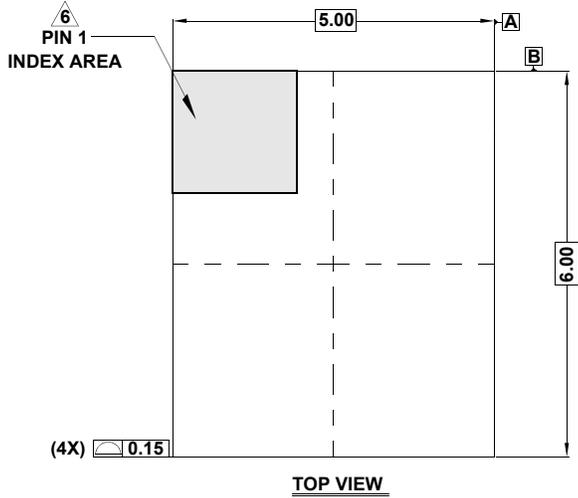
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.

2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.

3. Unless otherwise specified, tolerance : Decimal ± 0.05

4. Dimension b applies to the metallized terminal and is measured
   between 0.15mm and 0.25mm from the terminal tip.

5̸. Tiebar shown (if present) is a non-functional feature.

6̸. The configuration of the pin #1 identifier is optional, but must be
   located within the zone indicated. The pin #1 identifier may be
   either a mold or mark feature.