

Double channel high side driver

Features

| Type | $R_{DS(on)}$ | I_{lim} | V_{CC} |
|-------------|-----------------------------|-----------|----------|
| VND600PEP-E | 30m Ω ⁽¹⁾ | 25A | 36V |

1. Per each channel

- DC short circuit current: 25A
- CMOS compatible inputs
- Proportional load current sense
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Current limitation
- Very low standby power dissipation
- Protection against: loss of ground and loss of V_{CC}
- Reverse battery protection (see [Application schematic on page 13](#))
- In compliance with the 2002/95/ec european directive



Description

The VND600PEP-E is a monolithic device made using STMicroelectronics VIPower™ M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table).

This device has two channels in high side configuration; each channel has an analog sense output on which the sensing current is proportional (according to a known ratio) to the corresponding load current. Built-in thermal shutdown and outputs current limitation protect the chip from over temperature and short circuit. Device turns off in case of ground pin disconnection.

Table 1. Device summary

| Package | Order codes | |
|-------------|-------------|---------------|
| | Tube | Tape and reel |
| PowerSSO-24 | VND600PEP-E | VND600PEPTR-E |

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1 Block diagram and pin description

Figure 1. Block diagram

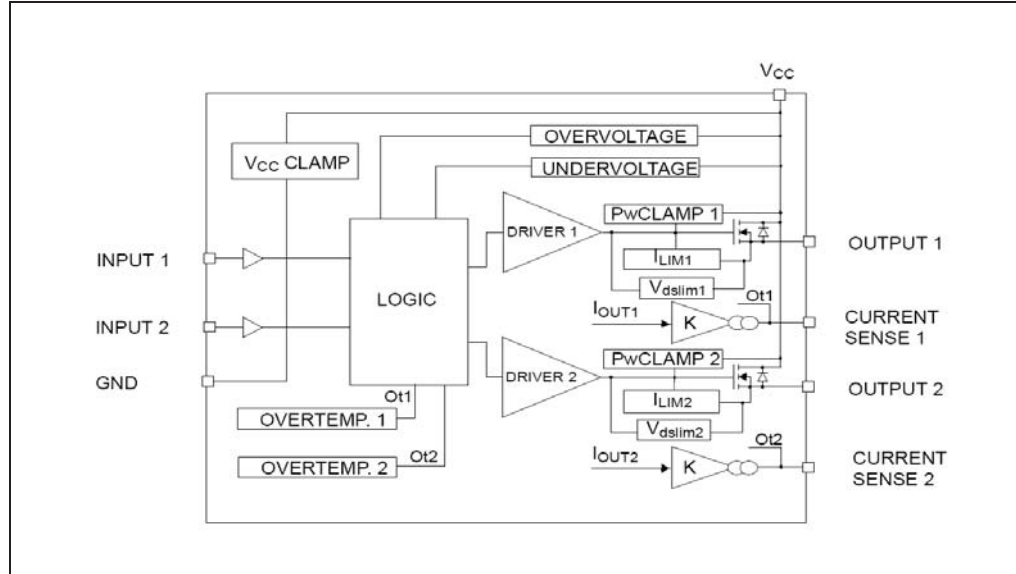


Figure 2. Configuration diagram (top view)

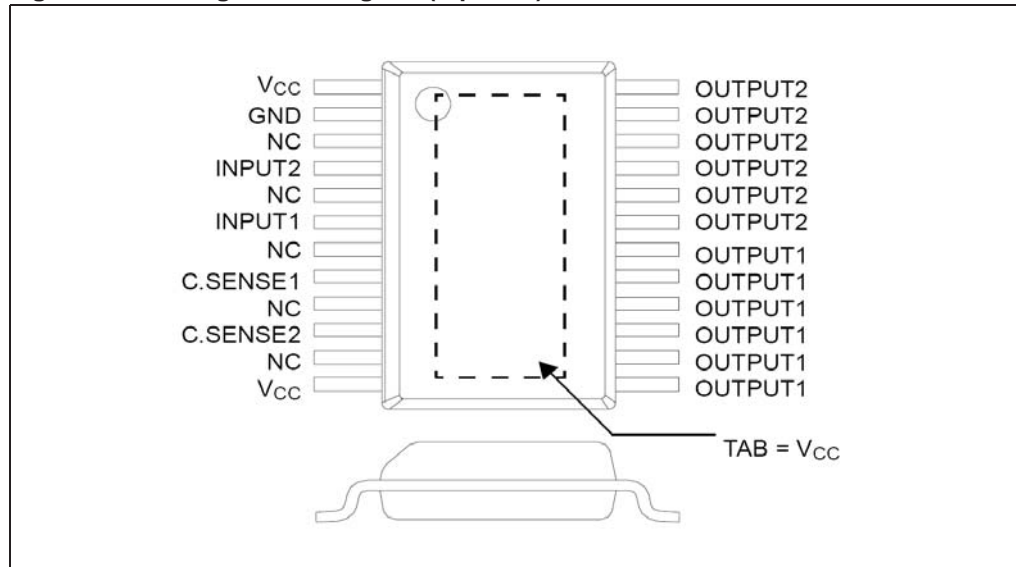
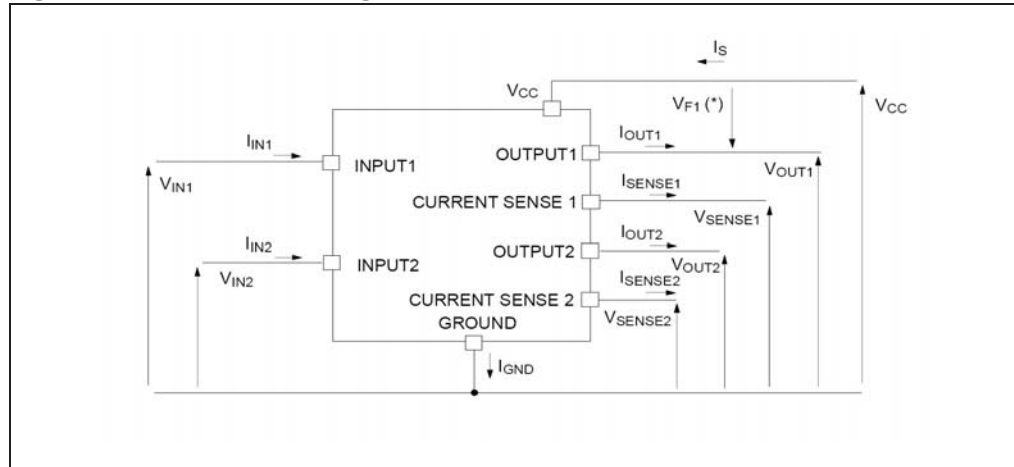


Table 2. Suggested connections for unused and not connected pins

| Connection / pin | Current sense | N.C. | Output | Input |
|------------------|-----------------------|------|-------------|------------------------|
| Floating | | X | X | X |
| To ground | Through 1 kΩ resistor | X | Not allowed | Through 10 kΩ resistor |

2 Electrical specifications

Figure 3. Current and voltage conventions



Note: $V_{Fn} = V_{CCn} - V_{OUTn}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 3. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------|-------------------------------|--------------------|--------|
| V_{CC} | DC supply voltage | 41 | V |
| $-V_{CC}$ | Reverse supply voltage | -0.3 | V |
| $-I_{GND}$ | DC reverse ground pin current | -200 | mA |
| I_{OUT} | Output current | Internally limited | A |
| I_R | Reverse output current | -21 | A |
| I_{IN} | Input current | +/-10 | mA |
| V_{CSENSE} | Current sense maximum voltage | -3 +15 | V V |

Table 3. Absolute maximum ratings (continued)

| Symbol | Parameter | Value | Unit |
|------------------|---|--------------------|------|
| V_{ESD} | Electrostatic discharge (human body model: R=1.5K Ω ; C=100pF) | | |
| | – Input | 4000 | V |
| | – Current sense | 2000 | V |
| | – Output | 5000 | V |
| | – V_{CC} | 5000 | V |
| E_{MAX} | Maximum switching energy (L=0.13mH; R _L =0 Ω ; V _{bat} =13.5V; T _{jstart} =150°C; I _L =40A) | 146 | mJ |
| P_{tot} | Power dissipation at T _c =25°C | 96 | W |
| T _j | Junction operating temperature | Internally limited | °C |
| T _c | Case operating temperature | -40 to 150 | °C |
| T _{STG} | Storage temperature | -55 to 150 | °C |

2.2 Thermal data

Table 4. Thermal data

| Symbol | Parameter | Value | | Unit |
|--------------------------------------|---|-------------------|-------------------|------|
| R _{thj-case} ⁽¹⁾ | Thermal resistance junction-case (max) | 1.8 | | °C/W |
| R _{thj-case} ⁽²⁾ | Thermal resistance junction-case (max) | 1.3 | | °C/W |
| R _{thj-amb} | Thermal resistance junction-ambient (max) | 54 ⁽³⁾ | 39 ⁽⁴⁾ | °C/W |

1. one channel ON

2. two channels ON

3. When mounted on a standard single-sided FR-4 board with 0.5cm² of Cu (at least 35 μ m thick).

4. When mounted on a standard single-sided FR-4 board with 8cm² of Cu (at least 35 μ m thick).

2.3 Electrical characteristics

8V < V_{CC} < 36V; -40°C < T_j < 150°C unless otherwise specified.

Per each channel

Table 5. Power

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------------------------|--------------------------|-----------------|------|------|------|------|
| V _{CC} ⁽¹⁾ | Operating supply voltage | | 5.5 | 13 | 36 | V |
| V _{USD} ⁽¹⁾ | Undervoltage shutdown | | 3 | 4 | 5.5 | V |
| V _{OV} ⁽¹⁾ | Overvoltage shutdown | | 36 | | | V |

Table 5. Power (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------------------|--------------------------|---|------|------|------|------|
| R _{ON} | On-state resistance | I _{OUT} =5A; T _j =25°C | | | 30 | mΩ |
| | | I _{OUT} =5A; T _j =150°C | | | 60 | mΩ |
| | | I _{OUT} =3A; V _{CC} =6V | | | 100 | mΩ |
| V _{clamp} | Clamp Voltage | I _{CC} =20mA ⁽²⁾ | 41 | 48 | 55 | V |
| I _S ⁽¹⁾ | Supply current | Off-state; V _{CC} =13V; V _{IN} =V _{OUT} =0V | | 12 | 40 | μA |
| | | Off-state; V _{CC} =13V; V _{IN} =V _{OUT} =0V; T _j =25°C | | 12 | 25 | μA |
| | | On-state; V _{IN} =5V; V _{CC} =13V; I _{OUT} =0A; R _{SENSE} =3.9kΩ | | | 6 | mA |
| I _{L(off1)} | Off-state Output Current | V _{IN} =V _{OUT} =V _{SENSE} =0V | 0 | | 50 | μA |
| I _{L(off3)} | Off-state Output Current | V _{IN} =V _{OUT} =V _{SENSE} =0V; V _{CC} =13V; T _j =125°C | | | 5 | μA |
| I _{L(off4)} | Off-state Output Current | V _{IN} =V _{OUT} =V _{SENSE} =0V; V _{CC} =13V; T _j =25°C | | | 3 | μA |

1. Per device.

2. V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

Table 6. Switching (V_{CC} =13V)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--|------------------------|---|------|----------------------|------|------|
| t _{d(on)} | Turn-on delay time | R _L =2.6Ω (see <i>Figure 4</i>) | - | 30 | - | μs |
| t _{d(off)} | Turn-on delay time | R _L =2.6Ω (see <i>Figure 4</i>) | - | 30 | - | μs |
| (dV _{OUT} /dt) _{on} | Turn-on voltage slope | R _L =2.6Ω (see <i>Figure 4</i>) | - | See relative diagram | - | V/μs |
| (dV _{OUT} /dt) _{off} | Turn-off voltage slope | R _L =2.6Ω (see <i>Figure 4</i>) | - | See relative diagram | - | V/μs |

Table 7. V_{CC} - output diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|--------------------|--|------|------|------|------|
| V _F | Forward on Voltage | -I _{OUT} =2.6A; T _j =150°C | | | 0.6 | V |

Table 8. Logic input (channels 1, 2)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|--------------------------|------------------------|------|------|------|------|
| V _{IL} | Input low level voltage | | | | 1.25 | V |
| I _{IL} | Low level input current | V _{IN} =1.25V | 20 | 65 | | μA |
| V _{IH} | Input high level voltage | | 3.25 | | | V |
| I _{IH} | High level input current | V _{IN} =3.25V | | | 10 | μA |

Table 8. Logic input (channels 1, 2) (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--------------------------|-------------------------------|------|-------------|------|--------|
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.5 | | | V |
| V_{ICL} | Input clamp voltage | $I_{IN}=1mA$ $I_{IN}=-1mA$ | 6 | 6.8 -0.7 | 8 | V V |

Table 9. Current sense ($9V \leq V_{CC} \leq 16V$)⁽¹⁾

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|---|---|--------------|--------------|--------------|----------|
| K_1 | I_{OUT}/I_{SENSE} | I_{OUT1} or $I_{OUT2}=0.5A$; $V_{SENSE}=0.5V$; other channels open; $T_j=40^\circ C \dots 150^\circ C$ | 3300 | 4400 | 6000 | |
| dK_1/K_1 | Current sense ratio drift | I_{OUT1} or $I_{OUT2}=0.5A$; $V_{SENSE}=0.5V$; other channels open; $T_j=40^\circ C \dots 150^\circ C$ | -10 | | +10 | % |
| K_2 | I_{OUT}/I_{SENSE} | I_{OUT1} or $I_{OUT2}=5A$; $V_{SENSE}=4V$; other channels open; $T_j=-40^\circ C$ $T_j=25^\circ C \dots 150^\circ C$ | 3800 3950 | 4400 4400 | 5400 5200 | |
| dK_2/K_2 | Current sense ratio drift | I_{OUT1} or $I_{OUT2}=5A$; $V_{SENSE}=4V$; other channels open; $T_j=-40^\circ C \dots 150^\circ C$ | -6 | | +6 | % |
| K_3 | I_{OUT}/I_{SENSE} | I_{OUT1} or $I_{OUT2}=15A$; $V_{SENSE}=4V$; other channels open; $T_j=-40^\circ C$ $T_j=25^\circ C \dots 150^\circ C$ | 3800 3950 | 4400 4400 | 4900 4700 | |
| dK_3/K_3 | Current sense ratio drift | I_{OUT1} or $I_{OUT2}=15A$; $V_{SENSE}=4V$; other channels open; $T_j=-40^\circ C \dots 150^\circ C$ | -6 | | +6 | % |
| $V_{SENSE1,2}$ | Max analog sense output voltage | $V_{CC}=5.5V$; $I_{OUT1,2}=2.5A$; $R_{SENSE}=10k\Omega$ $V_{CC}>8V$; $I_{OUT1,2}=5A$; $R_{SENSE}=10k\Omega$ | 2 4 | | | V V |
| V_{SENSEH} | Analog sense output voltage in over temperature condition | $V_{CC}=13V$; $R_{SENSE}=3.9k\Omega$ | | 5.5 | | V |
| $R_{VSENSEH}$ | Analog sense output impedance in over temperature condition | $V_{CC}=13V$; $T_j > TTSD$; All channels open | | 400 | | Ω |
| t_{DSENSE} | Current sense delay response | to 90% I_{SENSE} ⁽²⁾ | | | 500 | μs |

1. See [Figure 7](#).

2. Current sense signal delay after positive input slope

Table 10. Protections (1)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|--------------------------------|---|-------------|-------------|-------------|------|
| I_{lim} | DC short circuit current | $V_{CC}=13V$ $5.5V < V_{CC} < 36V$ | 25 | 40 | 70 70 | A A |
| T_{TSD} | Thermal shutdown temperature | | 150 | 175 | 200 | °C |
| T_R | Thermal reset temperature | | 135 | | | °C |
| T_{HYST} | Thermal hysteresis | | 7 | 15 | | °C |
| V_{demag} | Turn-off output voltage clamp | $I_{OUT}=2A$; $V_{IN}=0V$; $L=6mH$ | $V_{CC}-41$ | $V_{CC}-48$ | $V_{CC}-55$ | V |
| V_{ON} | Output voltage drop limitation | $I_{OUT}=0.5A$; $T_j = -40^{\circ}C \dots +150^{\circ}C$ | | 50 | | mV |

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Figure 4. Switching characteristics (resistive load $R_L=2.6$)

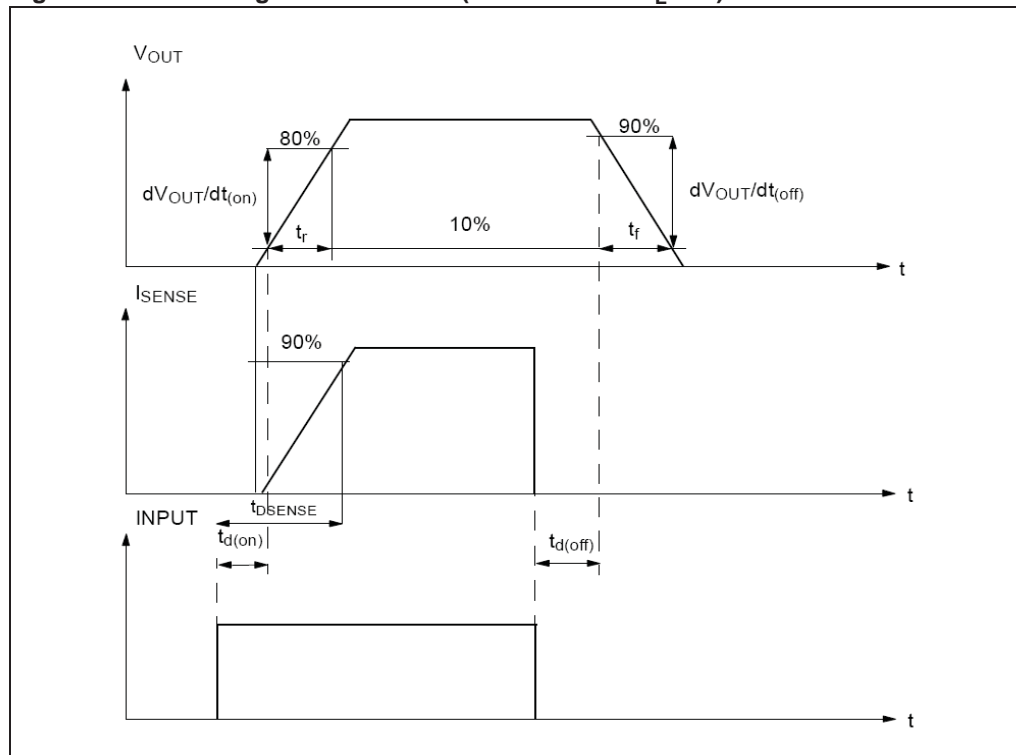


Table 11. Truth table (per channel)

| Conditions | Input | Output | Sense |
|-------------------------------|-------|--------|-----------------------|
| Normal operation | L | L | 0 |
| | H | H | Nominal |
| Over temperature | L | L | 0 |
| | H | L | V_{SENSEH} |
| Undervoltage | L | L | 0 |
| | H | L | 0 |
| Overvoltage | L | L | 0 |
| | H | L | 0 |
| Short circuit to GND | L | L | 0 ($T_j < T_{TSD}$) |
| | H | L | 0 ($T_j > T_{TSD}$) |
| | H | L | V_{SENSEH} |
| Short circuit to VXX | L | H | 0 |
| | H | H | < Nominal |
| Negative output voltage clamp | L | L | 0 |

Table 12. Electrical transient requirements (part 1/3)

| ISO T/R 7637/1 Test Pulse | Test levels | | | | Delays and Impedance |
|------------------------------|-------------|---------|---------|---------|-------------------------|
| | I | II | III | IV | |
| 1 | -25 V | -50 V | -75 V | -100 V | 2 ms 10 Ω |
| 2 | +25 V | +50 V | +75 V | +100 V | 0.2 ms 10 Ω |
| 3a | -25 V | -50 V | -100 V | -150 V | 0.1 μ s 50 Ω |
| 3b | +25 V | +50 V | +75 V | +100 V | 0.1 μ s 50 Ω |
| 4 | -4 V | -5 V | -6 V | -7 V | 100 ms, 0.01 Ω |
| 5 | +26.5 V | +46.5 V | +66.5 V | +86.5 V | 400 ms, 2 Ω |

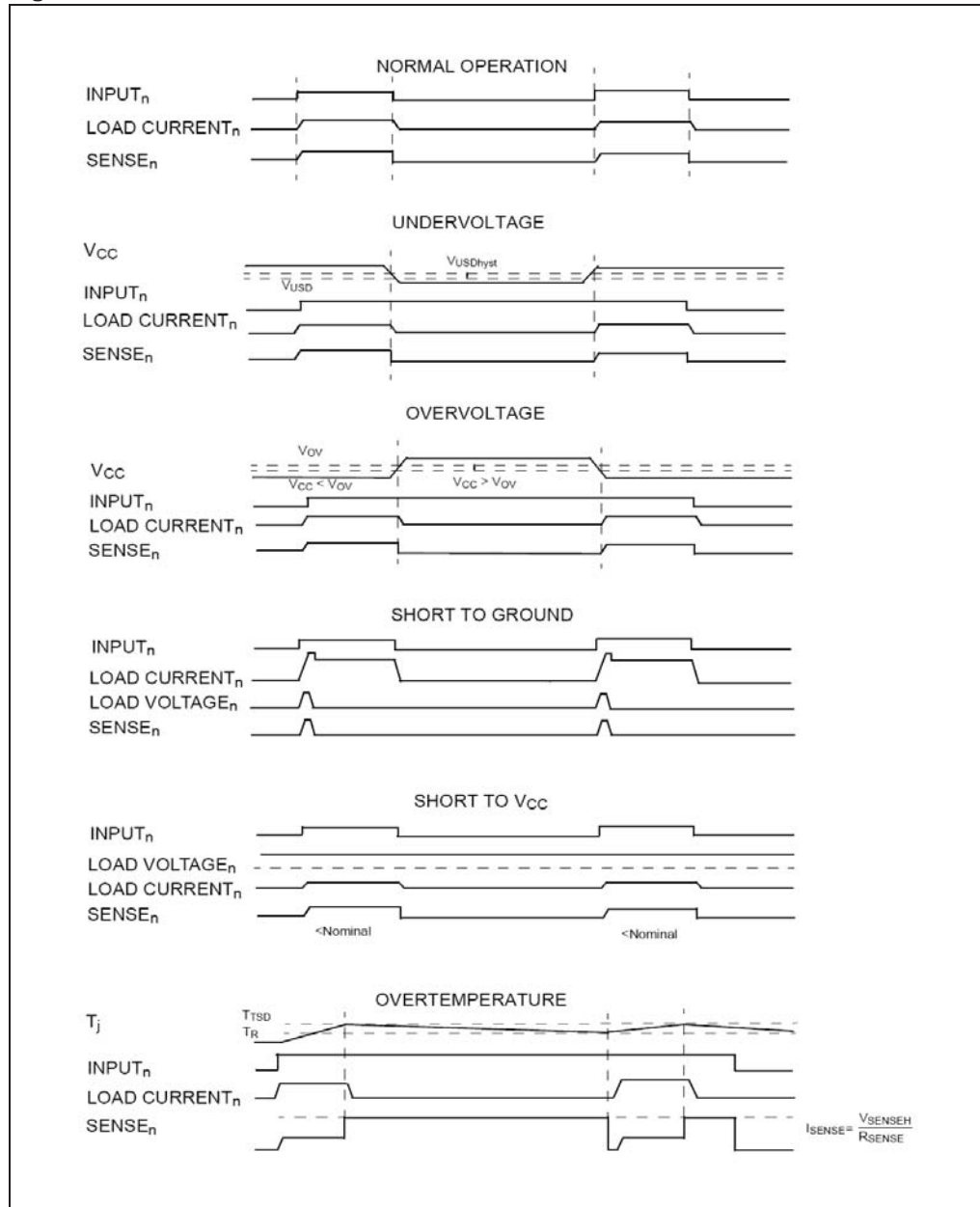
Table 13. Electrical transient requirements (part 2/3)

| ISO T/R 7637/1 Test Pulse | Test levels results | | | |
|------------------------------|---------------------|----|-----|----|
| | I | II | III | IV |
| 1 | C | C | C | C |
| 2 | C | C | C | C |
| 3a | C | C | C | C |
| 3b | C | C | C | C |
| 4 | C | C | C | C |
| 5 | C | E | E | E |

Table 14. Electrical transient requirements (part 3/3)

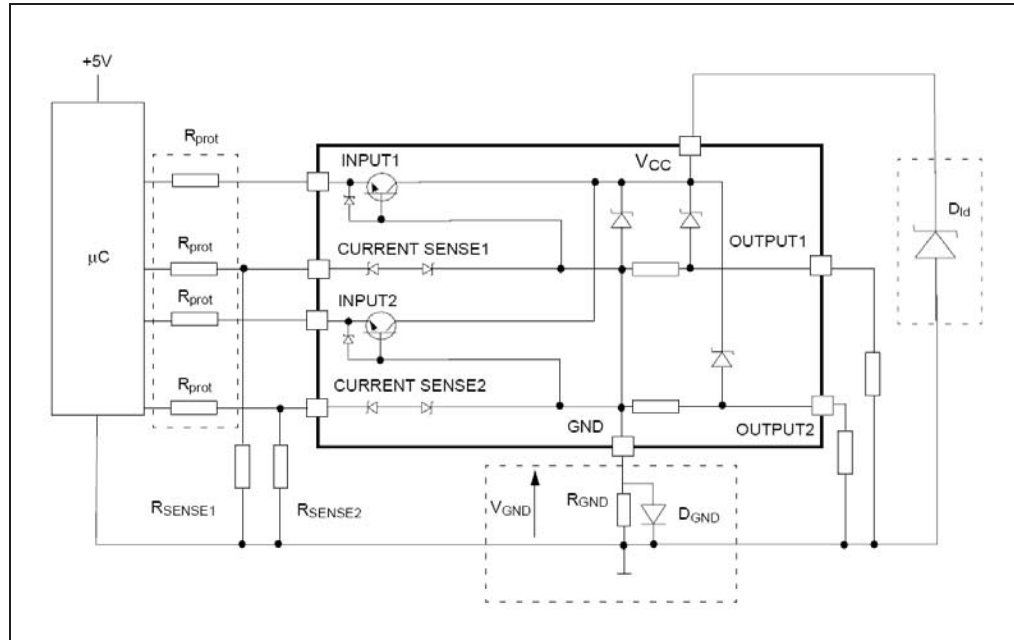
| Class | Contents |
|-------|---|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

Figure 5. Waveforms



3 Application information

Figure 6. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This solution can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\text{mV} / (I_{S(on)max})$
2. $R_{GND} \geq (V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet. Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are on in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor ($R_{GND}=1k\Omega$) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift ($\approx 600mV$) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

Series resistor in input line is also required to prevent that, during battery voltage transient, the current exceeds the absolute maximum rating.

Safest configuration for unused input pin is to leave it unconnected, while unused sense pin has to be connected to ground pin.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

3.3 Microcontroller I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of μC I/Os.

$$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

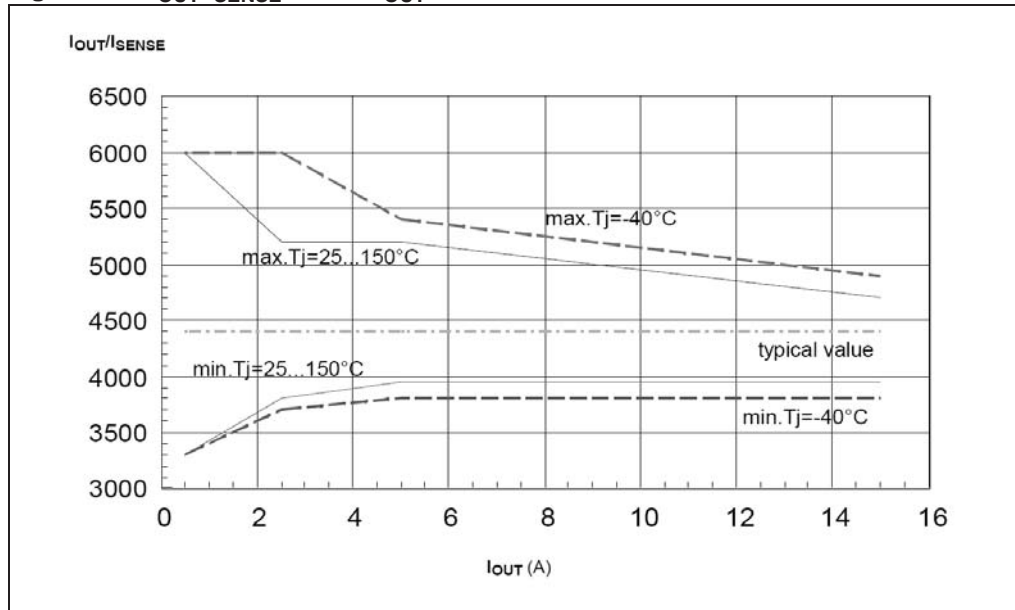
Calculation example:

$$\text{For } V_{CCpeak} = -100V \text{ and } I_{latchup} \geq 20mA; V_{OH\mu C} \geq 4.5V$$

$$5k\Omega \leq R_{prot} \leq 65k\Omega.$$

Recommended R_{prot} value is $10k\Omega$.

Figure 7. I_{OUT}/I_{SENSE} versus I_{OUT}



3.4 Electrical characteristics curves

Figure 8. Off-state output current

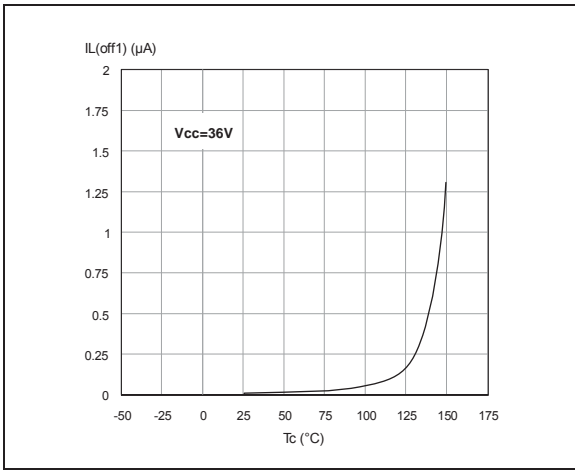


Figure 9. High level input current

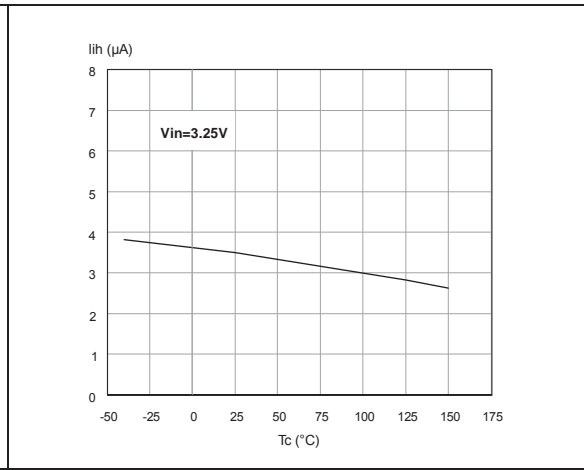


Figure 10. Input clamp voltage

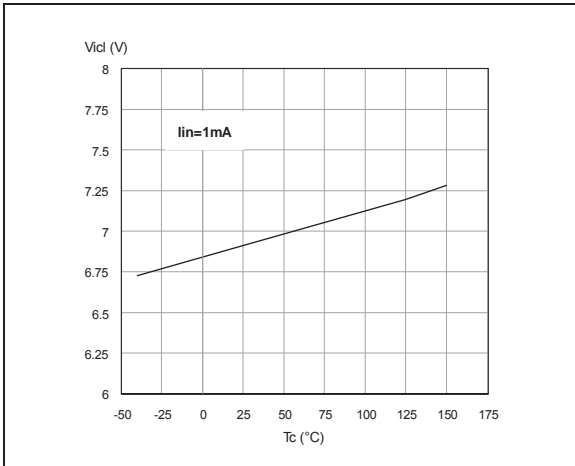


Figure 11. Input high level voltage

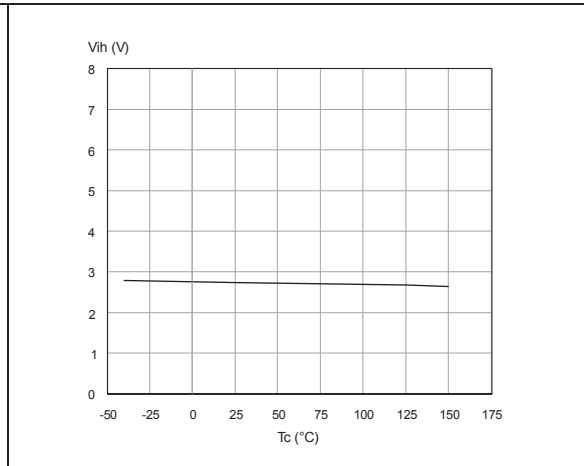


Figure 12. Input low level voltage

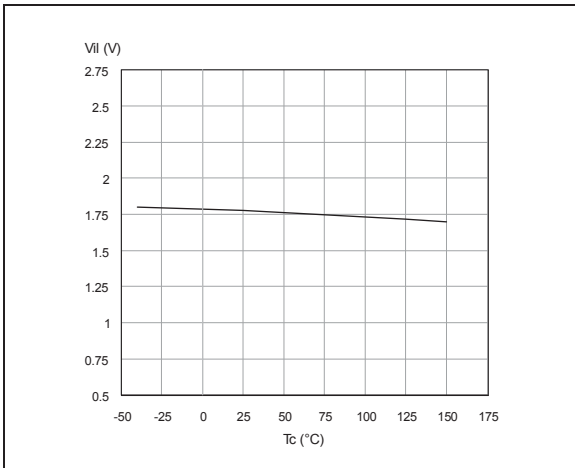


Figure 13. Input hysteresis voltage

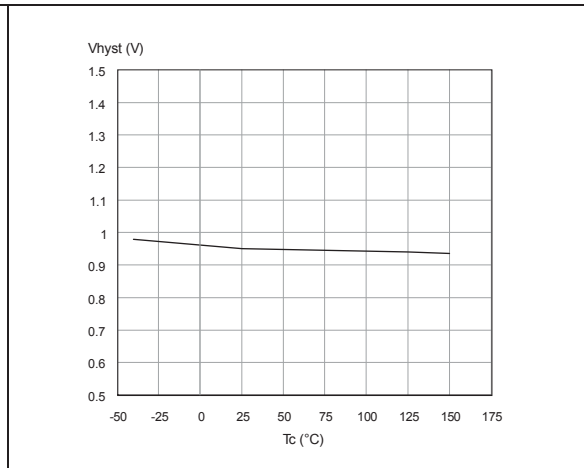


Figure 14. Overvoltage shutdown

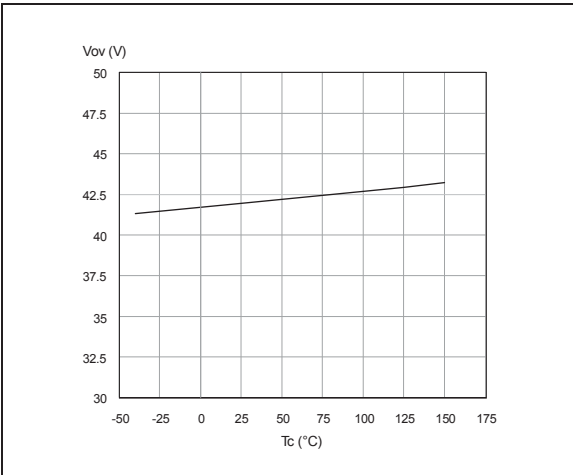


Figure 15. I_{LIM} vs T_{case}

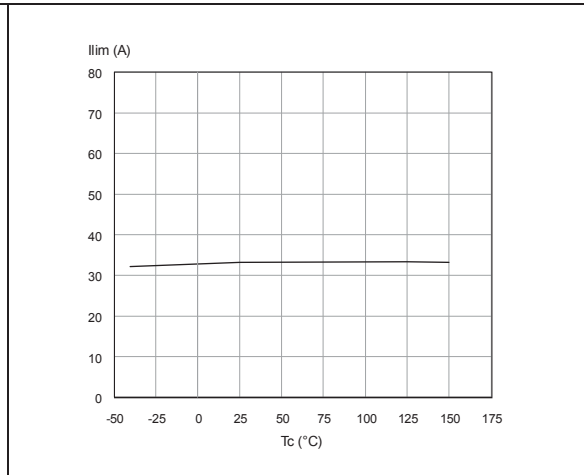


Figure 16. Turn-on voltage slope

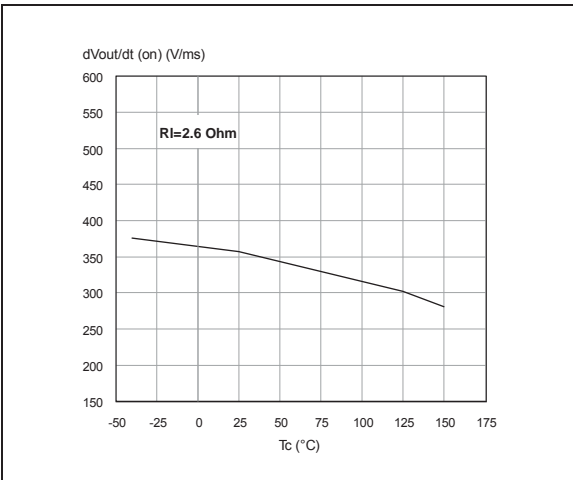


Figure 17. Turn-off voltage slope

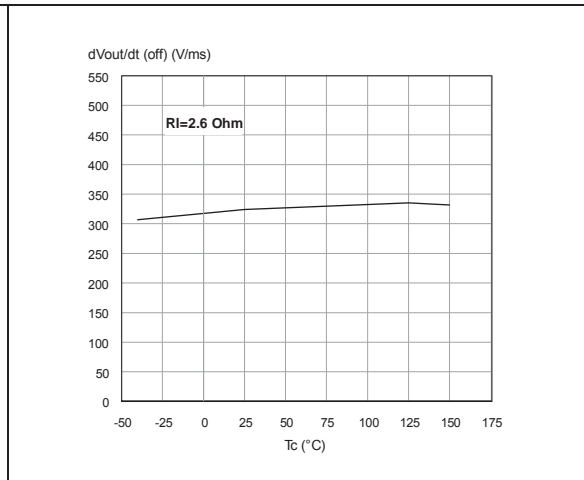


Figure 18. On-state resistance vs T_{case}

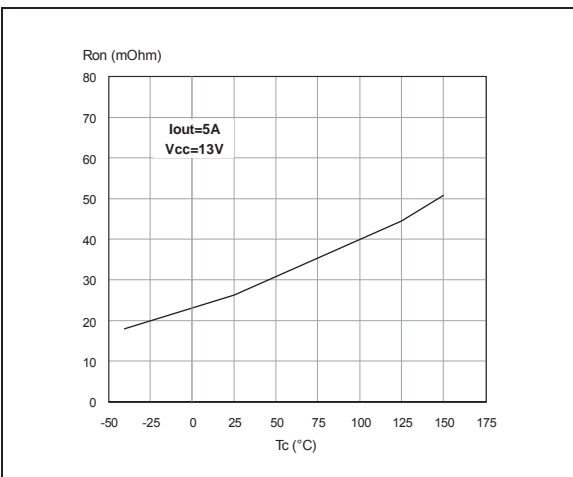
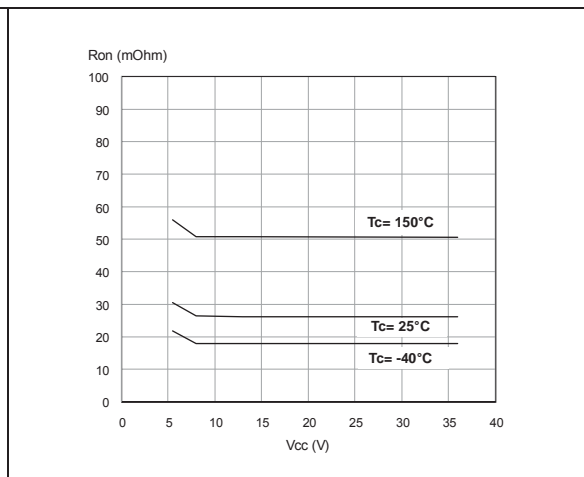


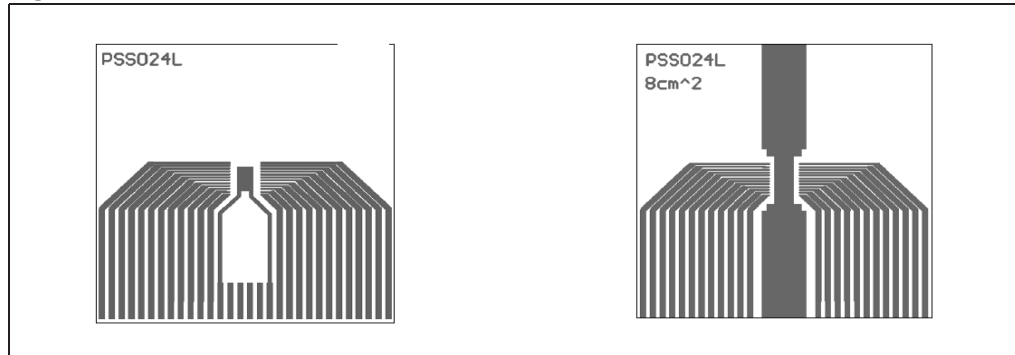
Figure 19. On-state resistance vs V_{CC}



4 Package and PC board thermal data

4.1 PowerSSO-24 thermal data

Figure 20. PowerSSO-24 PC board



Note: *Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70mm (front and back side), Copper areas: from minimum pad lay-out to 8cm²).*

Figure 21. $R_{thj-amb}$ vs PCB copper area in open box free air condition

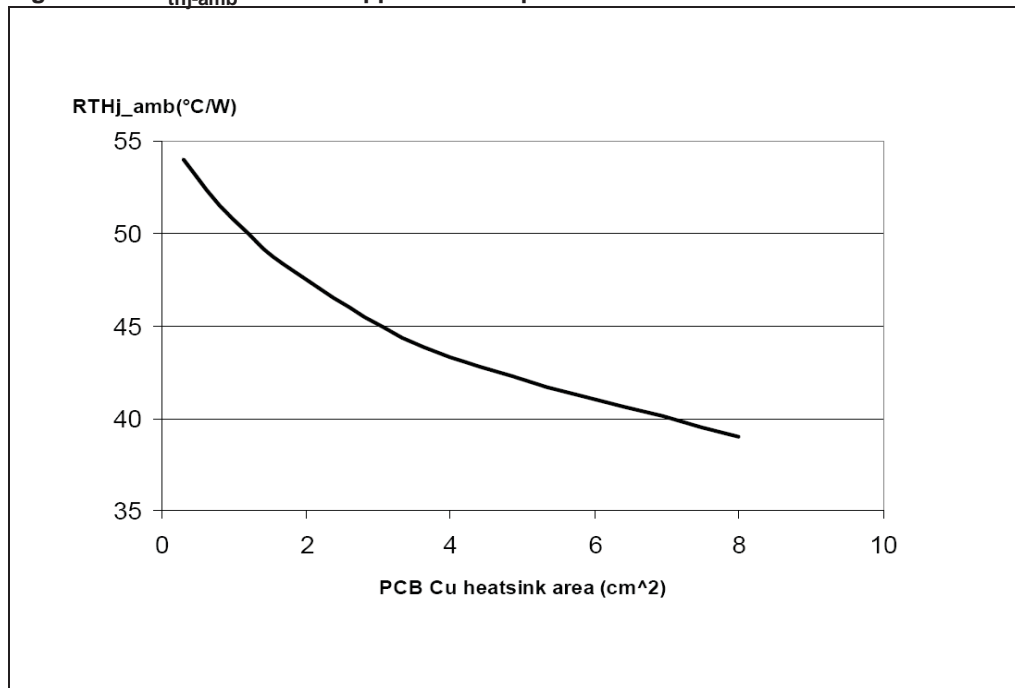
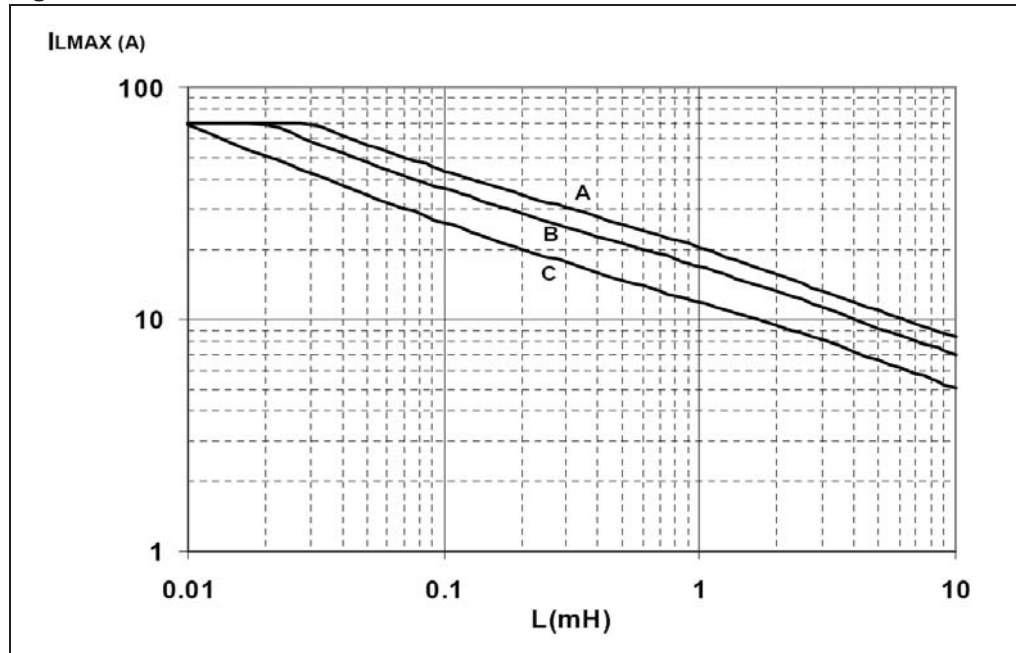


Figure 22. Maximum turn-off current versus load inductance



Legend

A = Single Pulse at $T_{Jstart} = 150^{\circ}\text{C}$

B = Repetitive pulse at $T_{Jstart} = 100^{\circ}\text{C}$

C = Repetitive Pulse at $T_{Jstart} = 125^{\circ}\text{C}$

Conditions:

$V_{CC} = 13.5\text{V}$

Values are generated with $R_L = 0\Omega$. In case of repetitive pulses, T_{Jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves B and C.

Figure 23. Demagnetization

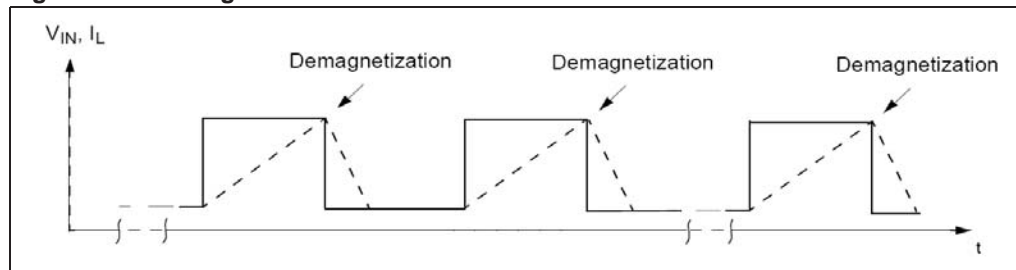


Figure 24. PowerSSO-24 thermal impedance junction ambient single pulse

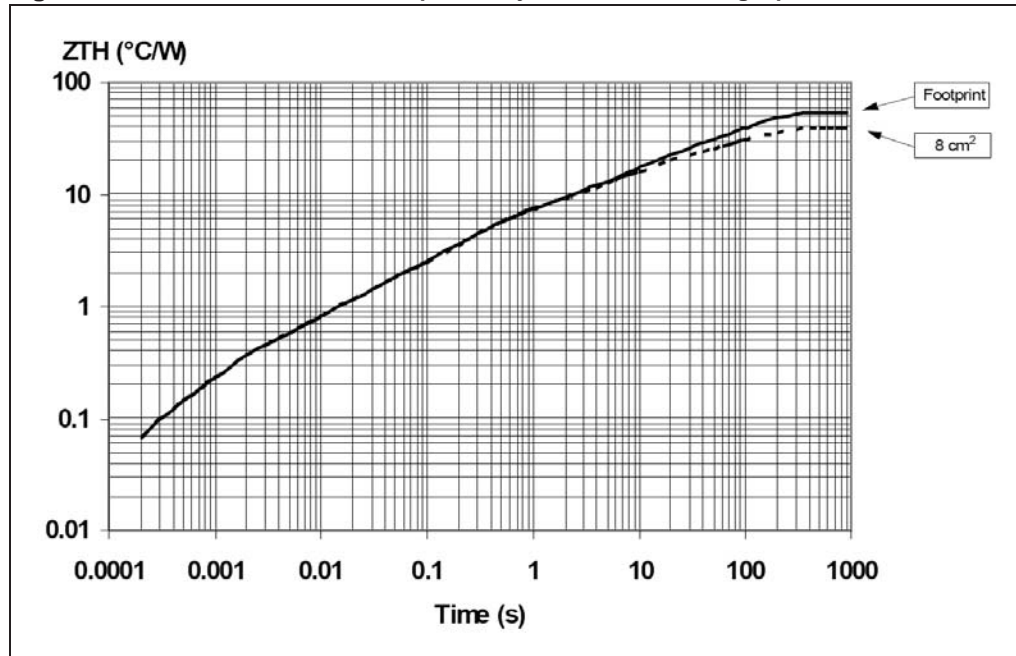
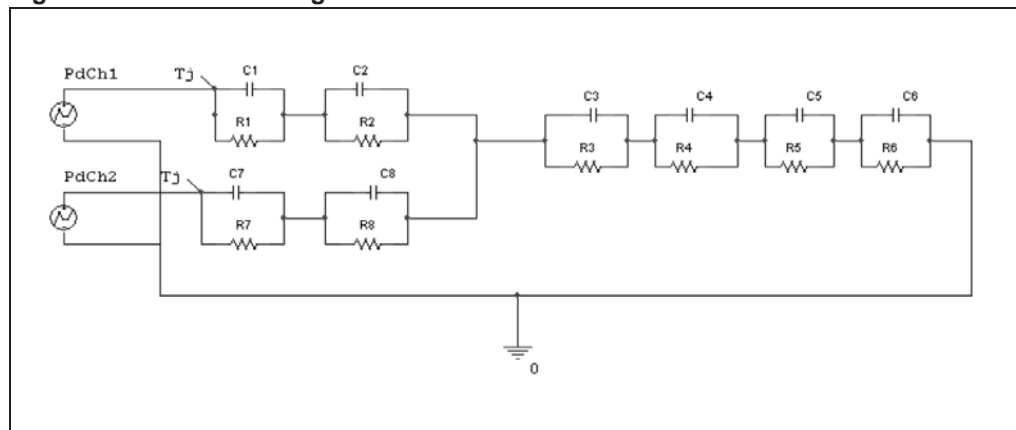


Figure 25. Thermal fitting model of a double channel HSD in PowerSSO-24



Equation 1: pulse calculation formula:

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p/T$

Table 15. Thermal parameters

| Area/island (cm ²) | Footprint | 8 |
|--------------------------------|-----------|---|
| R1 = R7 (°C/W) | 0.5 | |
| R2 = R8 (°C/W) | 0.3 | |
| R3 (°C/W) | 0.9 | |

Table 15. Thermal parameters (continued)

| Area/island (cm ²) | Footprint | 8 |
|--------------------------------|-----------|----|
| R4 (°C/W) | 5 | |
| R5 (°C/W) | 13.5 | 8 |
| R6 (°C/W) | 37 | 22 |
| C1 = C7 (W.s/°C) | 0.001 | |
| C2 = C8 (W.s/°C) | 0.005 | |
| C3 (W.s/°C) | 0.025 | |
| C4 (W.s/°C) | 0.08 | |
| C5 (W.s/°C) | 0.7 | |
| C6 (W.s/°C) | 3 | 5 |

5 Package and packing information

5.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com.

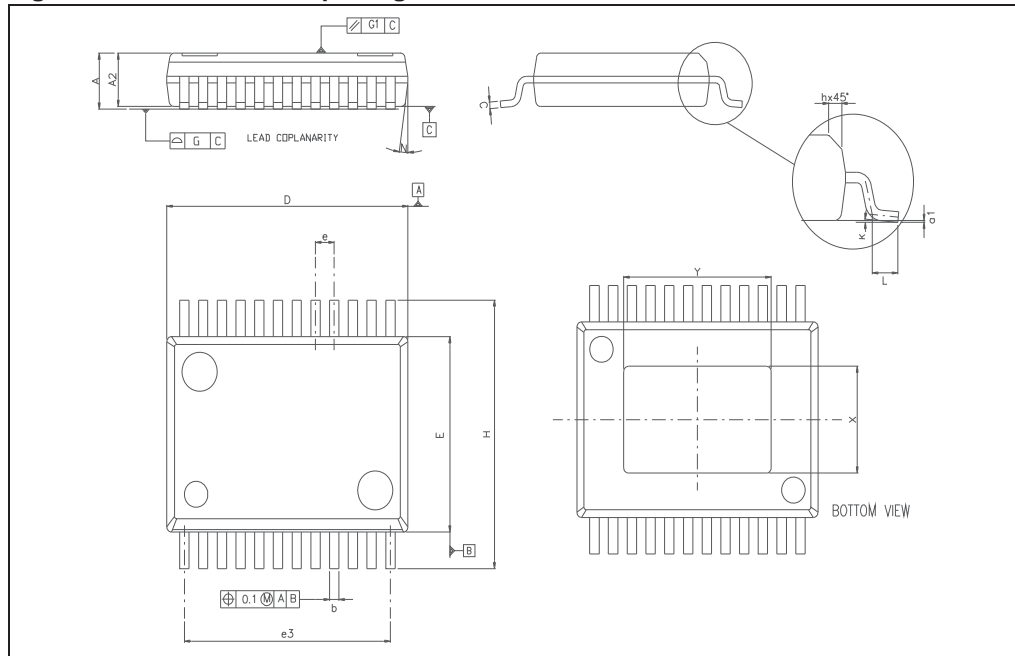
ECOPACK[®] is an ST trademark.

5.2 PowerSSO-24 mechanical data

Table 16. PowerSSO-24 mechanical data

| Symbol | millimeters | | |
|--------|-------------|-----|-------|
| | Min | Typ | Max |
| A | | | 2.45 |
| A2 | 2.15 | | 2.35 |
| a1 | 0 | | 0.1 |
| b | 0.33 | | 0.51 |
| c | 0.23 | | 0.32 |
| D | 10.10 | | 10.50 |
| E | 7.4 | | 7.6 |
| e | | 0.8 | |
| e3 | | 8.8 | |
| F | | 2.3 | |
| G | | | 0.1 |
| G1 | | | 0.06 |
| H | 10.1 | | 10.5 |
| h | | | 0.4 |
| k | 0° | | 8° |
| L | 0.55 | | 0.85 |
| N | | | 10deg |
| X | 4.1 | | 4.7 |
| Y | 6.5 | | 7.1 |

Figure 26. PowerSSO-24 package dimensions



5.3 Packing information

Figure 27. PowerSSO-24 tube shipment (no suffix)

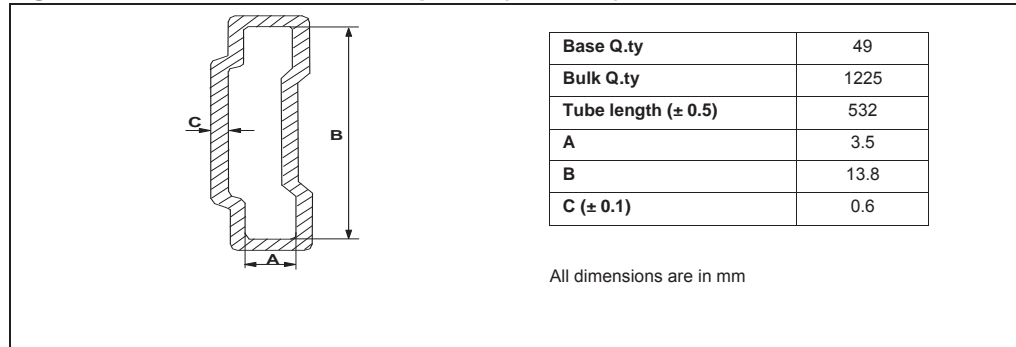
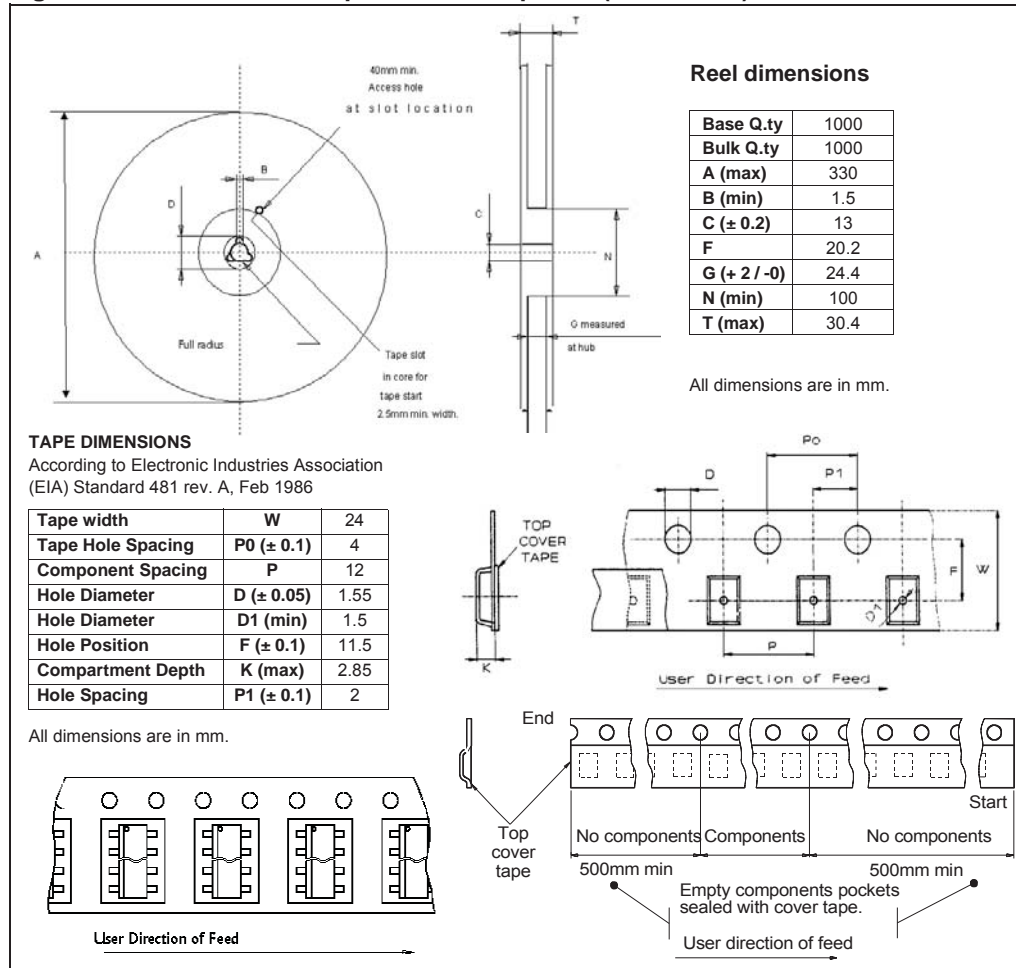


Figure 28. PowerSSO-24 tape and reel shipment (suffix “TR”)



6 Revision history

Table 17. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 04-Nov-2004 | 1 | Initial release. |
| 01-Dec-2004 | 2 | $I_{L(off2)}$ removal. |
| 01-Mar-2005 | 3 | <p><i>Table 3: Absolute maximum ratings:</i></p> <ul style="list-style-type: none"> – Added maximum switching energy. <p>Added <i>Section 2.2: Thermal data.</i></p> <p>Added <i>Figure 22: Maximum turn-off current versus load inductance.</i> -</p> <p>Added <i>Figure 24: PowerSSO-24 thermal impedance junction ambient single pulse.</i></p> |
| 01-Apr-2005 | 4 | <p>Modified <i>Figure 2: Configuration diagram (top view)</i></p> <p>Inserted <i>Section 5.3: Packing information</i></p> |
| 13-May-2005 | 5 | Minor changes |
| 24-Jun-2009 | 6 | <p><i>Table 16: PowerSSO-24 mechanical data:</i></p> <ul style="list-style-type: none"> – Deleted A (min) value – Changed A (max) value from 2.47 to 2.45 – Changed A2 (max) value from 2.40 to 2.35 – Changed a1 (max) value from 0.075 to 0.1 – Added F and k rows |
| 23-Sep-2013 | 7 | Updated Disclaimer. |

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